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Reverse-Current Phenomenon in Synchronous Rectifiers

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Synchronous rectification (SR) is used in low-voltage high-current dc-dc converters to achieve higher efficiency and to increase power density. When a diode is replaced with MOSFETs for rectification, one important difference between the diode and MOSFET is that the diode is a unidirectional device whereas the MOSFET is a bidirectional device. A diode has unidirectional current flow from the anode to the cathode whereas a MOSFET has bidirectional current from drain to source and from source to drain. In any event, no matter how the converter operates, the diode can block the reverse current while the MOSFET cannot.

Synchronous rectification can force continuous current in the output choke and current becomes negative under no-load and light-load conditions. The reverse current, apart from reducing efficiency at light load, can cause hard failure in a power supply. So this reverse-current phenomenon must be controlled to avoid hard failure when synchronous rectification is used. This is true in nonisolated buck converters as well as isolated dc-dc converters where synchronous rectification is employed on the secondary side. Fig. 1 shows simplified schematics of isolated and nonisolated dc-dc converters configured for synchronous rectification.

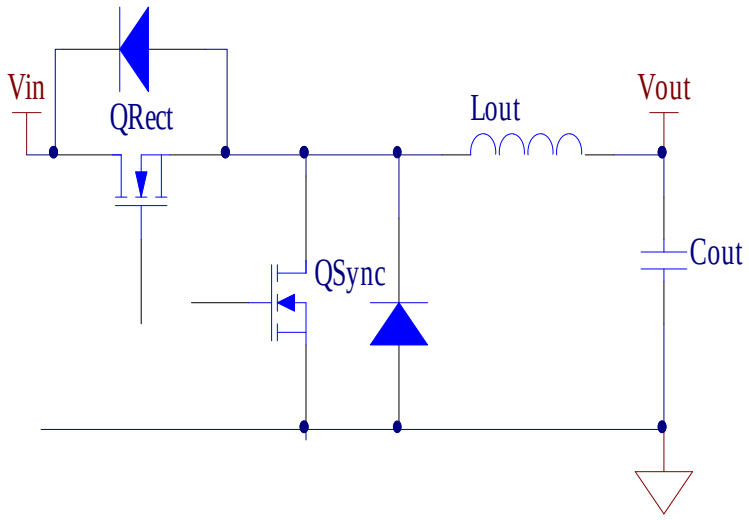

Fig. 1a. Nonisolated buck converter configured for synchronous rectification.

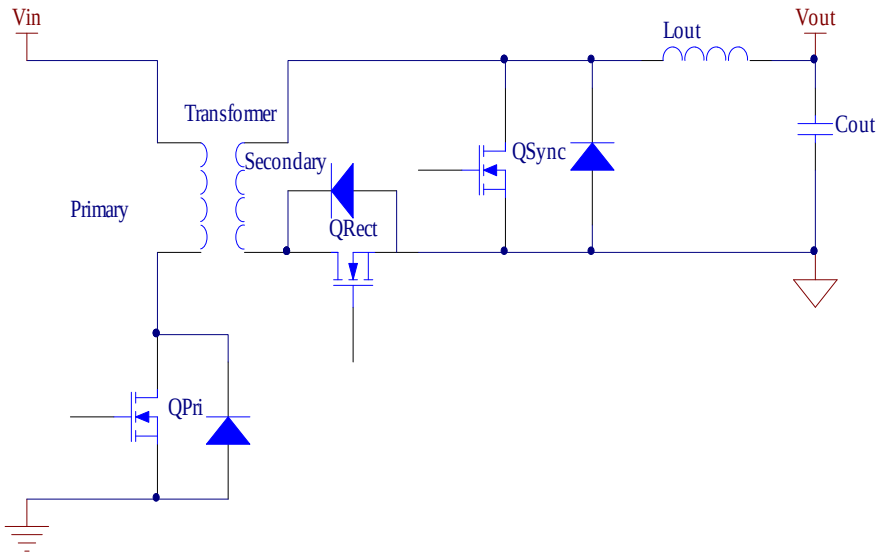

Fig.1b. Isolated dc-dc converter configured for synchronous rectification. (Note: Diodes shown are the built-in body diodes of the MOSFETs.)

There are many ways of driving the gates of the MOSFETs in synchronous rectifiers. One of the popular methods is to use complimentary pulses to drive the rectifier MOSFET (QRect) and the synchronous MOSFET (QSync) with dead time between pulses to prevent simultaneous conduction of top and bottom MOSFETs. Fig.2a and Fig.2b show gate-drive timings optimized for efficiency by avoiding cross conduction in a nonisolated buck converter.

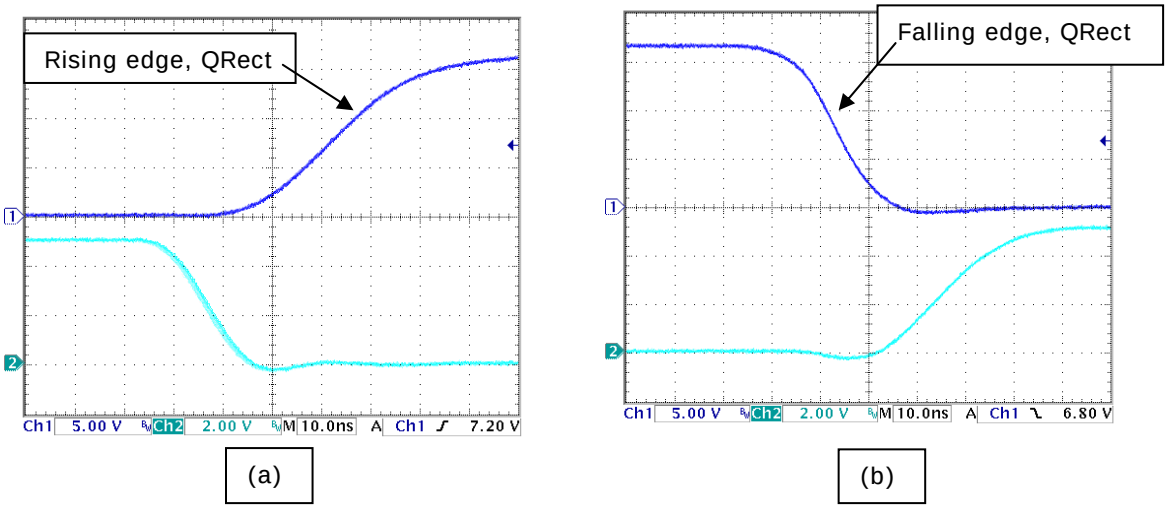

Fig. 2. Gate-drive signals for top MOSFET (QRect) (waveform on Ch1) and bottom MOSFET (QSync) (waveform on Ch2) in the nonisolated buck converter shown in Fig. 1a.

A reverse current can occur in synchronous rectifiers in various situations. Reverse current can occur during turn off of the power supply with no-load or light-load condition, pre-bias turn on, shutting down of the power supply during an overvoltage protection (OVP) or overcurrent (OCP) condition or during dynamic load change from full load to no load or light load and during sudden load removal. The reverse-current issue is attributed to the difference in characteristics between diodes and MOSFETs. Wherever the SR converter is used, the reverse current must be controlled carefully, or the reverse current can cause an abnormal turn on/turn off condition and may damage the MOSFET.

To avoid voltage stress and failure due to reverse current, PWM controllers used with synchronous rectification should have controlled start up and shutdown features for normal as well as pre-bias conditions. Figs. 3 through 5 show various waveforms for a nonisolated synchronous buck converter operating with no load. Fig. 3 waveforms were taken under normal operation, while Fig. 4 waveforms were taken during turn-on of the

converter, and Fig. 5 waveforms were taken during turn-off of the converter. These waveforms were obtained from a 12-V input 1.1-V output buck converter operating at 500 kHz. The converter is based on International Rectifier's IR3710 synchronous buck controller IC. Fig. 6. shows turn-off waveforms for an isolated buck converter.

In Fig. 3, the inductor current goes negative at no-load and light-load conditions. During turn off at no-load or light-load condition, when the inductor current is negative, if both MOSFETs are turned off, this negative current can only find a way through the body diode of Qrect to the input dc source. In an isolated converter, this produces voltage stress on the MOSFET as this current cannot find an immediate path for the current to continue to flow. The result is higher voltage stress on the devices. This reverse current eventually charges up the MOSFET output capacitance and then this reverse current can get reflected to primary side and can cause voltage stress on the primary-side MOSFET, eventually leading to its failure.

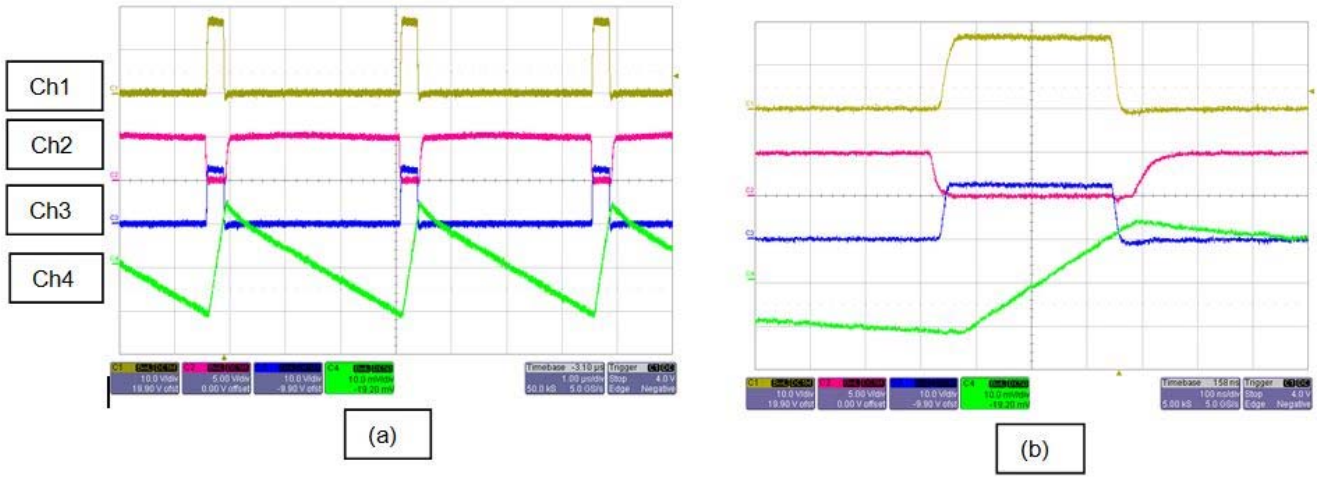

Fig. 3. Normal operating waveforms of a nonisolated buck converter at no load are shown in (a) with an expanded view in (b). Vin = 12 V and Vout = 1.1 V. Waveforms include top MOSFET gate voltage (Ch1), bottom MOSFET gate voltage (Ch2), phase voltage (Ch3), and inductor current (2 A/div.) (Ch4).

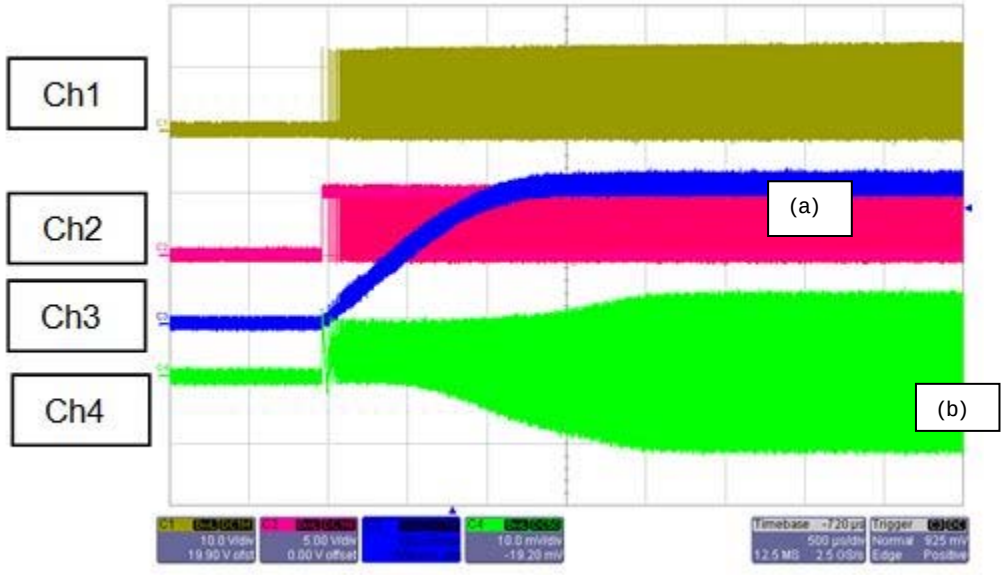

Fig. 4. Turn-on waveforms of a nonisolated buck converter at no load. Vin = 12 V and Vout = 1.1 V. Waveforms include top MOSFET gate voltage (Ch1), bottom MOSFET gate voltage (Ch2), Vout (Ch3), and inductor current (2 A/div.) (Ch4).

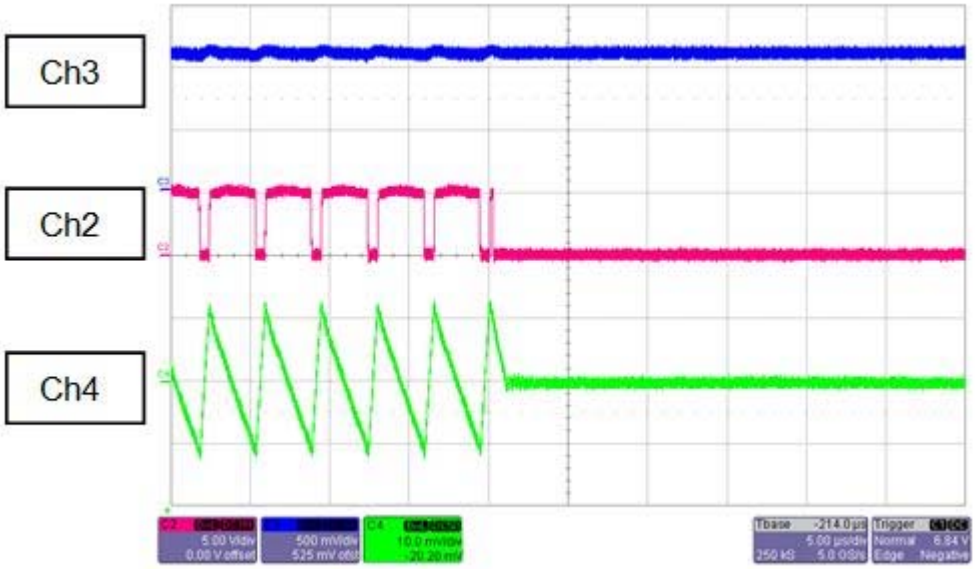

Fig. 5. Turn-off waveforms of a nonisolated buck converter at no load. Vin = 12 V and Vout = 1.1 V. Waveforms include top MOSFET gate voltage (Ch1), bottom MOSFET gate voltage (Ch2), Vout (Ch3), and inductor current (2 A/div.) (Ch4).

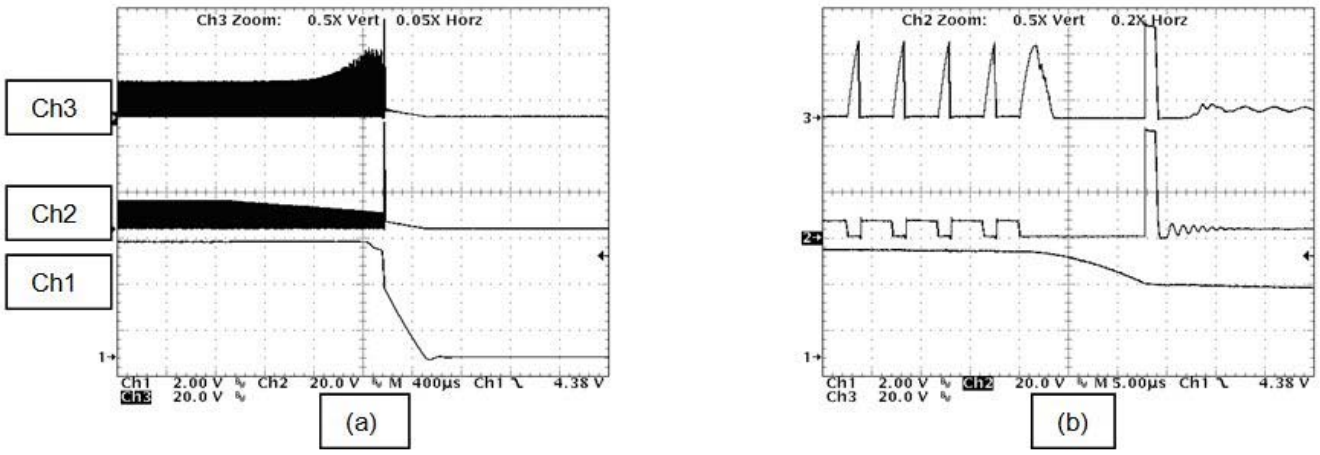

Fig. 6. Turn-off waveforms of an isolated buck converter are shown in (a) and with an expanded view in (b). Waveforms include Vout (Ch1), Qsync MOSFET drain voltage (Ch2), and Qrect MOSFET drain voltage (Ch3).

During turn on, if the synchronous MOSFET Qsync is on, then any pre-bias voltage present at the output will be discharged into it. This produces reverse-current build up in the output inductor and can cause the output voltage to dip.

Figure 7 shows pre-bias turn on without any issue. Figure 8 shows reverse current build up and output voltage dip when no pre-bias fix is implemented. The bottom MOSFET remains on for a certain amount of time and the inductor current goes negative to a big value. A large reverse current from the output causes output voltage to dip. This is not acceptable.

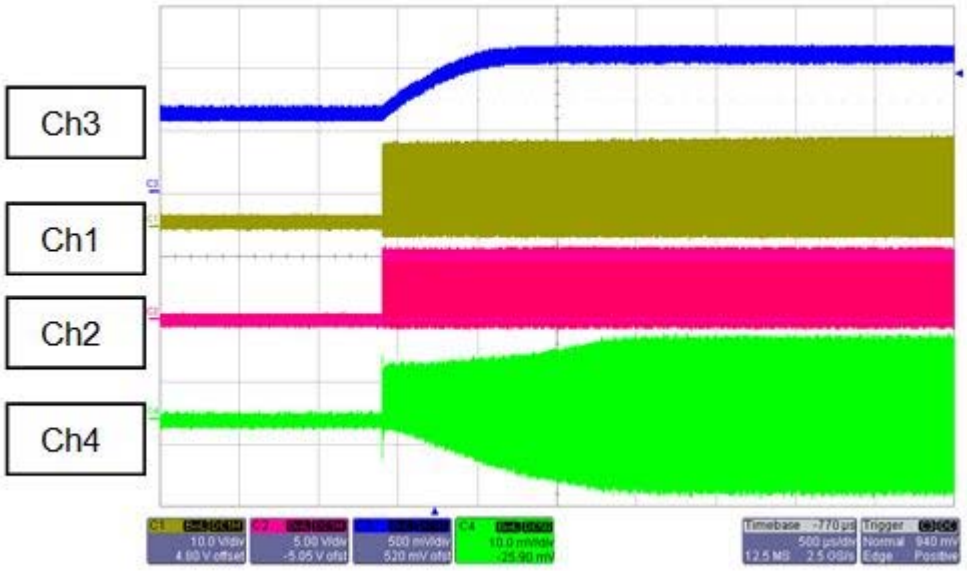

Fig 7. Pre-bias turn on waveforms for a nonisolated buck converter. Vin = 12 V and Vout = 1.1 V. Waveforms include top MOSFET gate voltage (Ch1), bottom MOSFET gate voltage (Ch2), Vout (Ch3), and inductor current (2 A/div.) (Ch4).

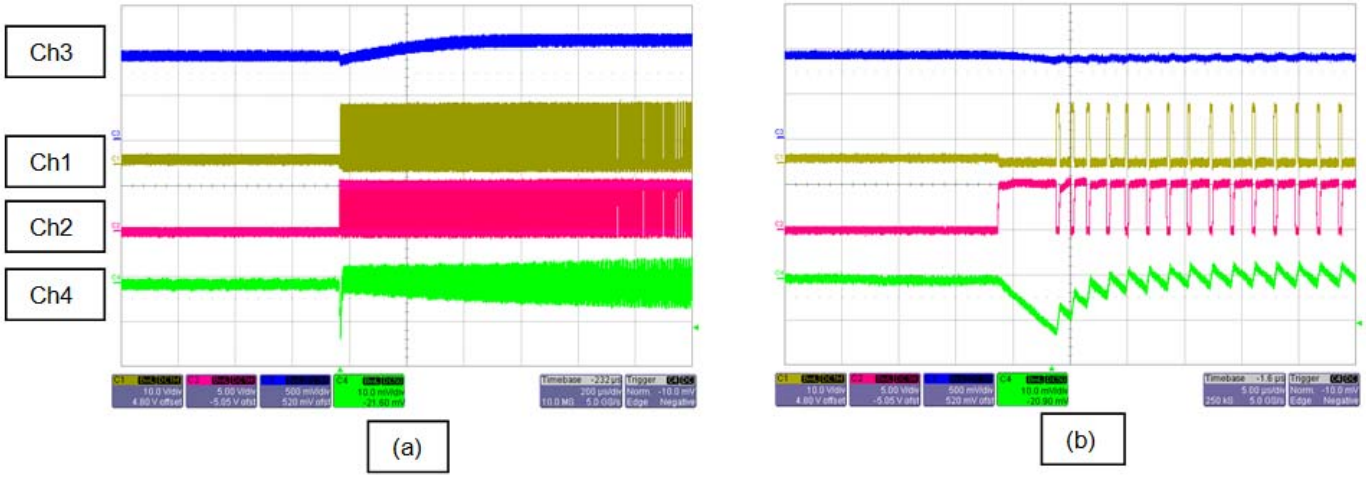

Fig. 8. Pre-bias turn-on waveforms for a nonisolated buck converter with an issue are shown in (a) and with an expanded view in (b). Vin = 12 V and Vout = 1.1 V. Waveforms include top MOSFET gate voltage (Ch1), bottom MOSFET gate voltage (Ch2), Vout (Ch3), and inductor current (2 A/div.)(Ch4).

To avoid this situation, synchronous MOSFETs should be kept off during turn on to achieve pre-bias turn on. Different methods are available to achieve pre-bias turn on with synchronous rectifiers. A comparator can be used to keep the synchronous MOSFET off during turn on until the output voltage reaches around 60% to 70% of its final. The drawback is that, until the synchronous MOSFET is turned on, its body diode is conducting and may be very lossy. After that, the synchronous MOSFET is released so that it can start switching. Under no-load and light-load conditions, until the synchronous MOSFET is turned on, the IR3710 PWM IC will be operating in a pulse-skipping mode.

In some pre-bias arrangement schemes, soft start is provided for a synchronous MOSFET gate drive, so that the on time of the synchronous MOSFET is gradually increased. The IC starts in an asynchronous mode and keeps the synchronous MOSFET off until the first gate signal for the top MOSFET is generated. The synchronous MOSFET always starts with a narrow pulse width and gradually increases its pulse width with a step of 25%, 50%, 75% and 100% until it reaches steady-state value. This will insure that reverse current does not build up in the output choke.

Sensing inductor current and turning off the synchronous MOSFET when current crosses zero is another method to implement a controlled turn on. Another way is to monitor the pulse width of QRect and then turn on the QSync MOSFET only when the pulse width of QRect reaches a certain pre-defined width. This can also prevent the synchronous MOSFET from operating with a higher duty cycle during turn on.

Care should be taken to ensure that the output rise is monotonic and does not produce any glitches on the output when QSync turns on. Monotonic startup provides safe start up into a pre-biased output, whereas conventional stepdown regulators without this fix can discharge the output capacitor, creating a voltage dip at the output that may damage a sensitive load.

Fig 9 shows a nonisolated buck converter where the load is fully removed from 100% to no load. The result is that the inductor current can go to a very large negative value.

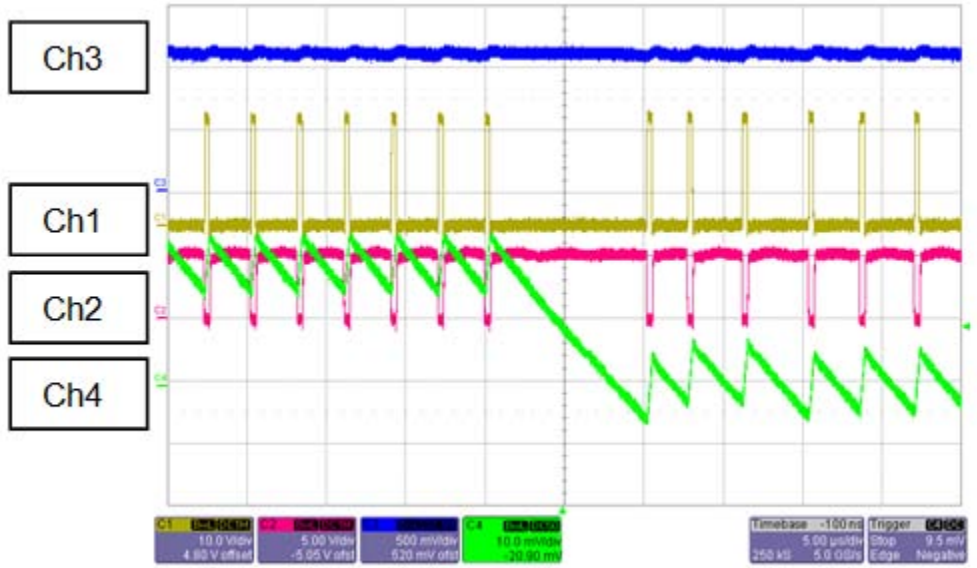

Fig. 9. 100% load transient in a nonisolated dc-dc converter. Vin = 12 V and Vout = 1.1 V. Waveforms include top MOSFET gate voltage (Ch1), bottom MOSFET gate voltage (Ch2), Vout (Ch3), and inductor current (5 A/div.)(Ch4).

In nonisolated buck converters this condition is acceptable as reverse current can go back to the input dc source through the body diode of the top MOSFET. But in isolated dc-dc converters this is an issue. If the synchronous MOSFET is turned off when current through it is negative, voltage stress can occur due to interruption of reverse current. This problem can be avoided if the synchronous MOSFET is turned off when inductor current is positive or when it reaches zero (i.e., just before going to negative value.)

During turn off, the synchronous MOSFET is to be turned off first in synchronization with a rectifier MOSFET gate signal. Then, the rectifier MOSFET is turned off after a few switching cycles so that inductor current can return to a positive value before the rectifier MOSFET is finally turned off. That technique is complicated. A simpler solution is to sense the inductor current and turn off the synchronous MOSFET when the inductor current becomes zero, not allowing it to go to negative.

About the Author

Suresh Kariyadan joined International Rectifier in June 2009 as senior staff engineer for POL Applications, Enterprise Power Business Unit (EPBU) where he is responsible for all Point Of Load customer support for the EPBU. The role involves understanding the customer's power supply requirements, providing reference designs, layout of PCBs, design verification tests, troubleshooting customer application boards and evaluating new product performance in application circuits.

Prior to joining International Rectifier, Suresh held senior engineering positions with Maxim Integrated Products and Cherokee International. He holds a Bachelor Degree in Electronics and Telecommunication from Kerala University, India.