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Why Struggle with Loop Compensation?

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In the power supply design industry, engineers sometimes have trouble compensating the control loop for their power supply. They try to get the loop to cross over at a very high switching frequency in an attempt to improve large-signal transient response, only to end up struggling with stability issues. One of the most popular control methods in power supply design is peak current-mode control. Even though this method is supposed to be easier to compensate than voltage-mode control, some power supply designers still struggle with compensating the voltage loop. The purpose of this article is to give some pointers that will, hopefully, make compensating the voltage loop in peak current-mode control easier.

Control Blocks In A Power Supply

When we studied control theory back in university, all control systems could be simplified by transfer function blocks. The voltage control loop in a peak current-mode-controlled power converter is no different. The voltage loop ($T_V(f)$) can be simplified and represented as the product of two different transfer blocks (Figure 1).

The first transfer block is the power-stage control-to-output transfer function ($G_{CO}(f)$), which can be described as the ratio of the change (ΔV_{OUT}) in output voltage over the change in control voltage (ΔV_C). Note that this block is actually the combination of the pulse width modulation (PWM) modulator gain (K) and the power supply output filter gain ($G_F(f)$). The second transfer block is generally the output-to-control transfer function ($G_C(f)$), sometimes referred to as the compensation transfer function, which can be described as ratio ΔV_C over the change in ΔV_{OUT}. If an optoisolator is used, it will have a transfer function block as well $G_{OPTO}(f)$ that would be found on the line between blocks K and $-G_C(f)$ blocks.

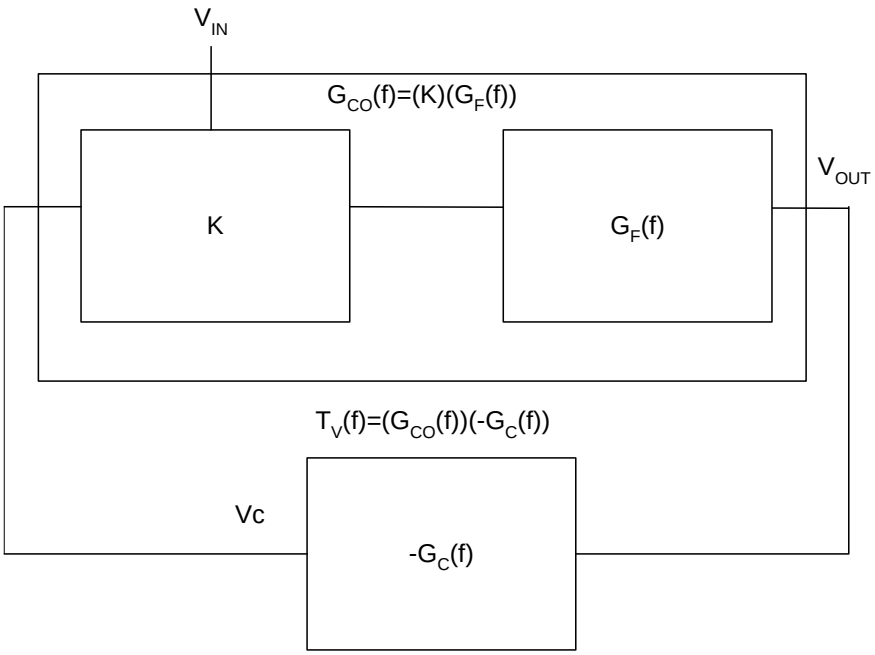

Fig. 1. Simplified block diagram of power supply voltage loop.

Figure 2 shows the functional schematic of a peak current-mode-control forward converter represented by the block diagram in Figure 1. The control blocks are separated by dashed lines.

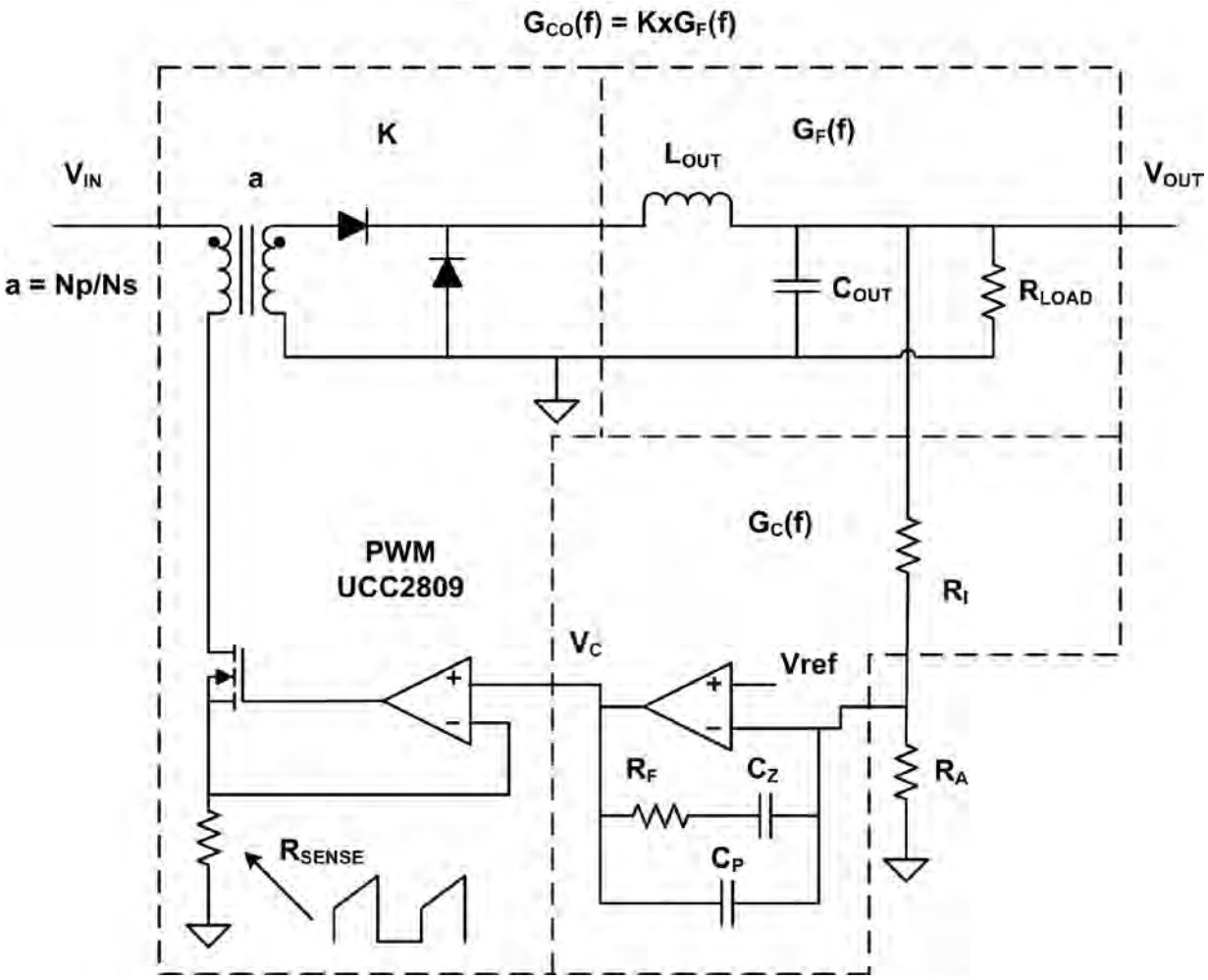

Figure 2. Simplified block diagram of power supply voltage loop.

Originally, the idea behind peak current-mode control was to control the average current through the inductor of the power stage, making it look like a current source by removing the double pole that occurs between the interaction of the output capacitor (C_{OUT}) and the power stage's inductor (L_{OUT}). A control block diagram of this model is presented in Figure 3.

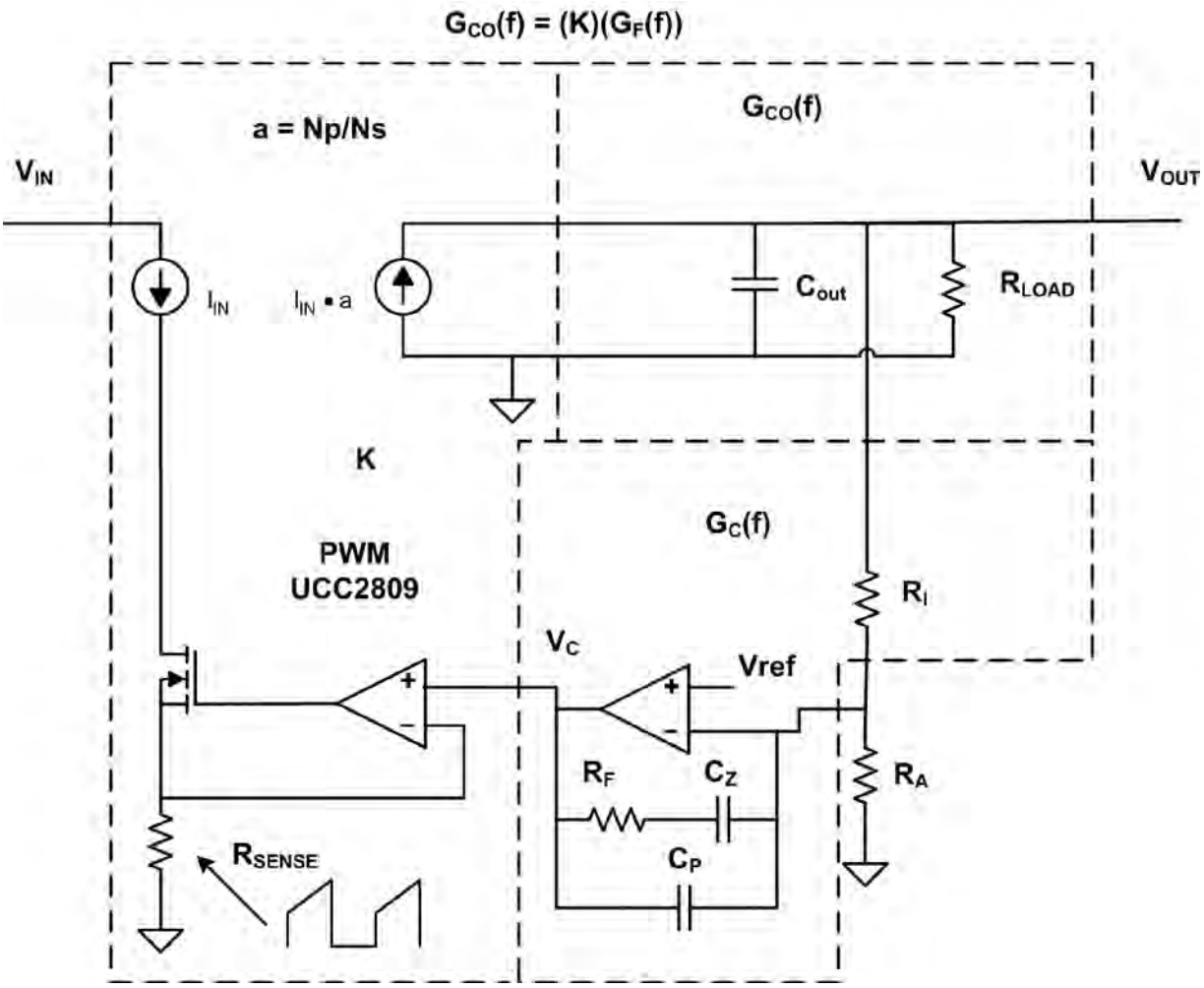

Figure 3. Modeling the inductor as a current source in a peak current-mode-controlled converter.

A simplified control-to-output transfer function ($G_{CO}(f)$) for Figure 2 is presented below. In this equation, a is the transformer's turns ratio, R_{LOAD} is the converter's output load impedance, C_{OUT} is the converter's output filter capacitance, and R_{ESR} is C_{OUT}'s equivalent series resistance. Another term, S(f), is the angular velocity as a function of frequency.

$$S(f) = 2\pi \times j \times f$$

From the control-to-output transfer function ($G_{CO}(f)$), you will see that there is a zero (f_{ZCO}) that occurs between the interaction of C_{OUT} and R_{ESR} and a pole (f_{PCO}) that occurs between the interaction of R_{LOAD} and C_{OUT}.

$$G_{CO}(f) = \frac{\Delta V_{OUT}}{\Delta V_C} = \frac{a \times R_{LOAD}}{R_{SENSE}} \frac{(S(f) \times R_{ESR} \times C_{OUT} + 1)}{(S(f) \times R_{LOAD} \times C_{OUT} + 1)}$$

$$f_{ZCO} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

$$f_{PCO} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

Over time, engineers using peak current-mode control discovered there was a double pole (f_{PP}) in $G_{CO}(f)$ that occurs at roughly half the switching frequency (f_S). The following equations describe the $G_{CO}(f)$ of a peak

current-mode-controlled forward converter that includes the effects of f_{PP}. Note that if you analyze the forward converter with a network analyzer, you will find this transfer function does not exactly match what the model describes.

The zero (F_{ZCO}) that occurs because of the interaction of R_{ESR} and C_{OUT} moves with load. The f_{PP} happens at slightly more than half the switching frequency. How will you ever compensate the voltage loop without an accurate model? You can do what engineers have been doing for years: Compensate the voltage loop by using a network analyzer to measure $G_{CO}(f)$ and then follow a few simple rules for stability that will be presented in this article.

$$f_{PP} \approx \frac{f_S}{2}$$

$$Gco(f) = \frac{\Delta V_{OUT}}{\Delta V_C} = \frac{a \times R_{LOAD}}{R_{SENSE}} \frac{(S(f) \times R_{ESR} \times C_{OUT} + 1)}{(S(f) \times R_{LOAD} \times C_{OUT} + 1)} \times \frac{1}{1 + \frac{S(f)}{2\pi \times f_{pp}} + \left(\frac{S(f)}{2\pi \times f_{pp}}\right)^2}$$

Slope Compensation

It was discovered that in a peak current-mode-control converter there could be subharmonic oscillations caused by sudden changes in duty cycle. This is because changes in duty cycle cause errors in the average output current (I_{OUT1}, I_{OUT2}) due to the control voltage (V_C) not being able to correct for the changes in duty cycle fast enough. To correct for this error a technique called slope compensation was developed. This technique adds a triangular voltage waveform to the current-sense signal ($V2=V_{SLOPE}+V_{RSENSE}$) that forces the average output current to not change drastically with sudden changes in duty cycle. Refer to Figure 4 for details.

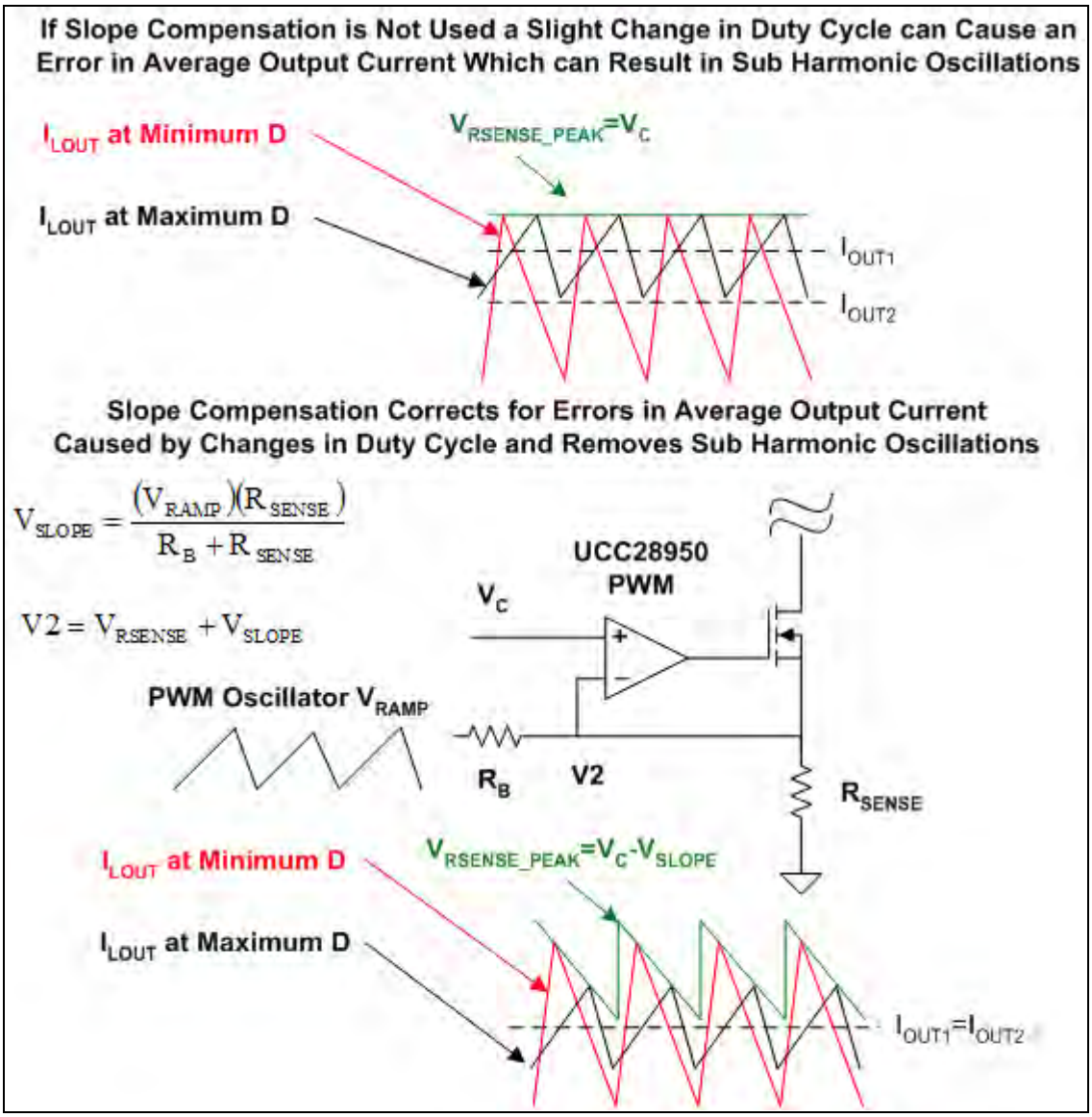

Figure 4. Slope compensation is needed for stability.

One of the most important steps in setting up the control loop for peak current-mode control is correctly adding slope compensation to the current-sense signal (V_{RSENSE}). If you do not use slope compensation, you will be fighting subharmonic oscillation, even though your network analyzer is telling you that the loop should be stable. If you add too much slope compensation, the converter will operate in voltage-mode control and not operate correctly, and may be unpredictable.

As a general rule to help ensure stability, the amount of slope compensation (V_{SLOPE}) added to the current-sense signal should be equal to half the down slope of the output inductor current (dI_{LOUT}). The following equations calculate the slope compensation (V_{SLOPE}) for the peak current-mode-controlled forward converter presented in Figure 2. In these equations, dI_{LOUT} is the change in inductor ripple current and V_{OUT} is the output voltage. L_{OUT} is the output filter inductance and D is the converter's duty cycle. Variable fs is the converter's switching frequency.

$$dI_{LOUT} = \frac{V_{OUT} \times dt}{L_{OUT}} = \frac{V_{OUT}(1-D)}{L_{OUT} \times fs}$$

If a transformer is used in your design, the magnetizing current (dI_{LM}) in the primary of the transformer caused by the magnetizing inductance of the primary (L_M) will add some slope compensation and needs to be accounted for when adding slope compensation. To ensure that the converter is not operating in voltage-mode

control, it is recommended that you choose a transformer for your design with a dI_{LM} that is less than half the reflected down slope (dI_{LOUT}) of the output inductor current. The following equations can be used for selecting the correct amount of slope compensation for the forward converter presented in Figures 1 and 2.

$$dI_{LM} = \frac{V_{IN} \times dt}{L_M} = \frac{V_{IN}(D)}{L_M \times fs}$$

$$dI_{LM} \le \frac{dIL_{OUT} \times 0.5}{a}$$

$$V_{SLOPE} = \left(\frac{dIL_{OUT}}{2 \times a} - dIL_m \right) \times R_{SENSE}$$

General Rules For Stability

In the power supply control loop ($T_V(f)$), when the loop is 180 degrees out of phase, this is equivalent to swapping the polarities of the inputs of an operational amplifier used in the feedback network ($G_C(f)$). If this occurs at the voltage-loop crossover when the feedback loop has a gain of one, the loop could become unstable and break into oscillations. To ensure this does not occur, we generally design $T_V(f)$ for 45 degrees of phase margin (PM) at voltage-loop crossover.

In most switch-mode power supplies, the control loop will eventually approach a 180-degree phase shift. To ensure this does not cause loop instability, we generally design for greater than 6 dB of gain margin (GM) to ensure the control signal is attenuated when $T_V(f)$ is 180 degrees out of phase. When evaluating the control loop ($T_V(f)$) the phase margin can be read as the magnitude of phase during crossover. The gain margin is calculated in the traditional way, 0 dB minus the gain in dB when the loop is 180 degrees out of phase. The gain and phase margin rule is a staple in good control-loop design. This rule is summarized below.

1. Set PM ≥ 45 degrees at voltage-loop crossover, which is defined as the frequency where the magnitude of the loop gain ($T_V(f)$) = 1 (i.e. 0 dB).

2. Set GM > 6 dB, where GM is defined as 0 dB – $\text{gain}_{@180\ \text{DEGREE PHASE SHIFT}}$.

Where Should My Voltage-Loop Crossover Be For $T_V(f)$?

According to Nyquist, for voltage-loop stability, the crossover frequency (f_c) needs to be less than half the converter's switching frequency (f_s).

3. $$f_C < \frac{f_S}{2}$$

In peak current-mode control, the voltage loop should be crossed over a decade before the double pole that occurs in $G_{CO}(f)$. Depending on the topology used, this double pole may occur at less than half the switching frequency. Using a network analyzer allows the designer to know exactly where the double pole occurs.

4. $$f_C < \frac{f_{PP}}{10}$$

Measure $G_{CO}(f)$ With A Network Analyzer

Even if you have a good model of your control-to-output transfer function, you will end up modifying the control loop based on measured results from a network analyzer. It is easier to compensate the voltage by initially using the voltage amplifier network ($G_C(f)$) as an integrator and measure the actual $G_{CO}(f)$ characteristics. This can be accomplished by setting capacitor C_P in Figures 1 and 2 to 1 µF to measure $G_{CO}(f)$ and not populating R_F and C_Z. The loop will not be optimized and the input voltage and load currents should be adjusted slowly to avoid oscillations.

The following two plots (Figures 5 and 6) show the measured gain and phase of a 600-W peak current-mode controlled, phase-shifted, full-bridge converter using TI's UCC28950 secondary-side controller. This controller

does not require an optoisolator and a standalone voltage feedback amplifier (TL431), making the voltage loop easier to compensate.

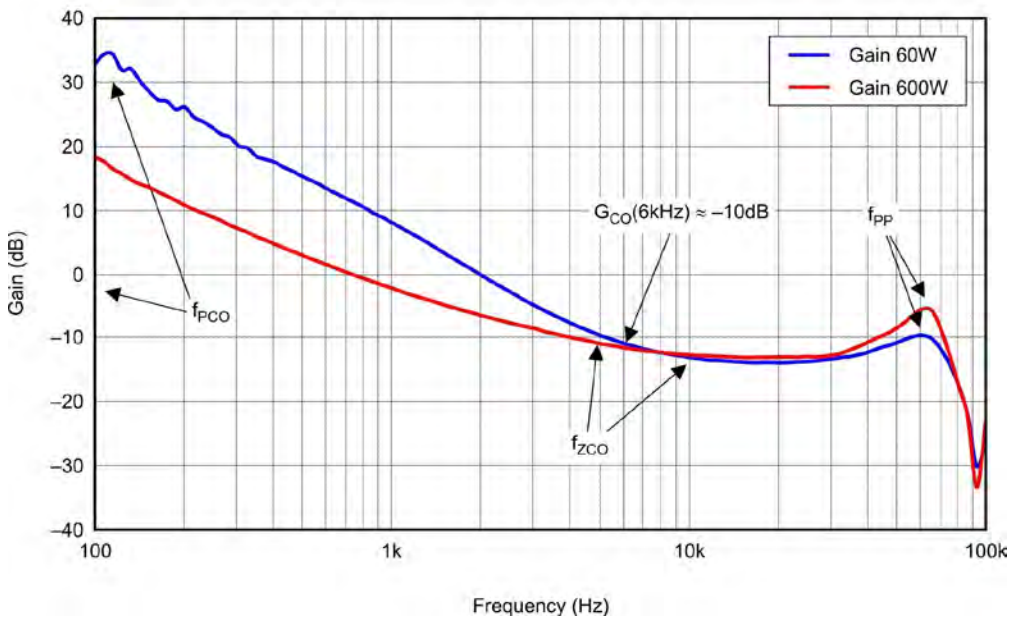

Figure 5. Control-to-output gain GCO(f) in dB.

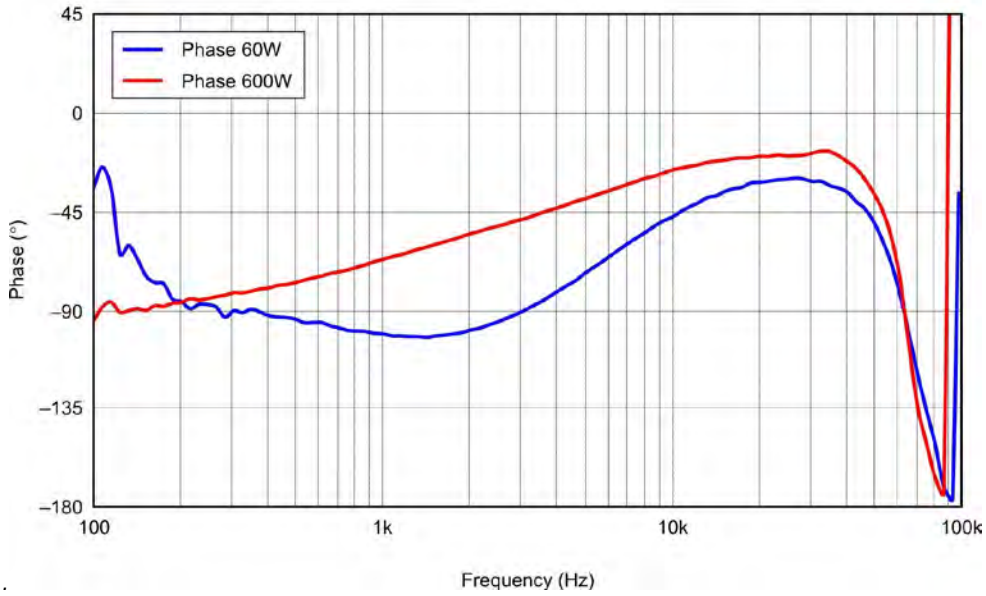

Figure 6. Control-to-output phase $G_{CO}(f)$ in degrees.

The $G_{CO}(f)$ is more complicated than what is defined above and you could spend hours deriving a transfer function that closely models the measured results. However, it is not necessary to compensate the loop once the actual frequency response data is obtained with a network analyzer. From the plots below it can be observed that the low-frequency pole (f_{PCO}) from the interaction of C_{OUT} and R_{LOAD} changes frequency with changes in output power. The zero in $G_{CO}(f)$ that is caused by the interaction of C_{OUT} and R_{ESR} also moves with load. The f_{PP} of $G_{CO}(f)$ for this converter occurs at roughly 60 kHz. Note that $G_{CO}(f)$ should be set up to cross the voltage loop ($T_V(f)$) a decade before this double pole at roughly 6 kHz.

$$f_C < \frac{f_{PP}}{10} = \frac{60kHz}{10} = 6kHz$$

To set up $G_C(f)$ requires knowing the highest gain of $G_{CO}(f_C)$ at crossover. From the measured $G_{CO}(f)$ this occurs at the 60-W load and is roughly -10 dB.

$$G_{CO}(f_C) \approx -10dB$$

Setting Up The Voltage Amplifier ($G_C(f)$)

One of the more popular compensation techniques for peak current-mode control is a type-two compensator that is presented in Figures 2 and 3. The following equation describes the transfer function. It has a pole that occurs at the origin. The type-two amplifier also has a zero (f_Z) that can be programmed by selecting R_F and C_Z values. Additionally, the type-two compensation network has a pole (f_P) that can be programmed by selecting R_F and C_P.

$$Gc(f) = \frac{\Delta V_C}{\Delta V_{VOUT}} = \frac{1}{S(f)(C_Z + C_P) \times R_I} \frac{(S(f) \times R_F \times C_Z + 1)}{\left(S(f) \times R_F \times \frac{C_P \times C_Z}{C_Z + C_P} + 1\right)}$$

$$f_Z = \frac{1}{2\pi \times R_F \times C_Z}$$

$$f_P = \frac{1}{2\pi \times R_F \times \frac{C_P \times C_Z}{C_Z + C_P}}$$

Resistor R_I and R_A are selected based on dc output voltage and resistor R_F is set at loop crossover to correct for the gain at $G_{CO}(fc)$. In this power converter, R_I was selected to be 9.09 kΩ. To cross over the voltage loop at roughly 6 kHz required an R_F resistor of 28.7 kΩ.

$$R_F = R_I \times 10^{\frac{-G_{CO}(f_C)}{20}} = 9.09k \times 10^{\frac{-(-10dB)}{20}} \approx 28.7k$$

Capacitor C_Z is set to give added phase margin at crossover and can be set a decade below the crossover frequency (f_C).

$$Cz = \frac{1}{2\pi \times \frac{f_c}{10} \times Rf} = 9.2nF$$

For this design a standard capacitor value of 10 nF was used for C_Z.

$$Cz = 10nF$$

This leaves one pole in the $G_C(f)$ feedback that is used to cancel the phase gain caused by the ESR of the output capacitor in $G_{CO}(f)$ after f_C. This helps maintain stability, ensuring the gain continues to roll off after voltage-loop crossover.

$$f_C > f_P < f_{PP}$$

To ensure the gain roles off before the double-pole frequency, set the pole frequency of the compensator at twice the crossover frequency. To compensate this voltage loop, a standard 470-pF capacitor for C_P is used.

$$f_P = 2 \times f_C = 12kHz$$

$$C_P = \frac{1}{2\pi \times Rf \times f_P} \approx 460\,pF$$

A standard capacitor of 470 pF was used for C_P.

$$C_P = 470\,pF$$

After selecting the compensation components for $G_C(f)$, double check the voltage loop with a network analyzer and adjust it if needed. The plots in Figures 7 and 8 were taken with a network analyzer to measure the voltage loop $T_V(f)$ at 60 W and 600 W. These plots show that the voltage loops crossed over (f_C) at roughly 3.8 kHz at 600-W load with a phase margin at crossover of 110 degrees. At a 60-W load $T_V(f)$ crossed over at roughly 5 kHz with greater than 45 degrees of phase margin at f_C.

The voltage loop at 10 percent load crossed over at 1 kHz less than the design target. However, loop compensation is not an exact science and being within 1 to 2 kHz is quite acceptable. Note that the gain was less than -30 dB as the phase of $T_V(f)$ approached 180 degrees. This yields a gain margin of greater than 6 dB. The network analyzer always has problems measuring -180 degrees. It cannot determine whether the phase is ±180 degrees.

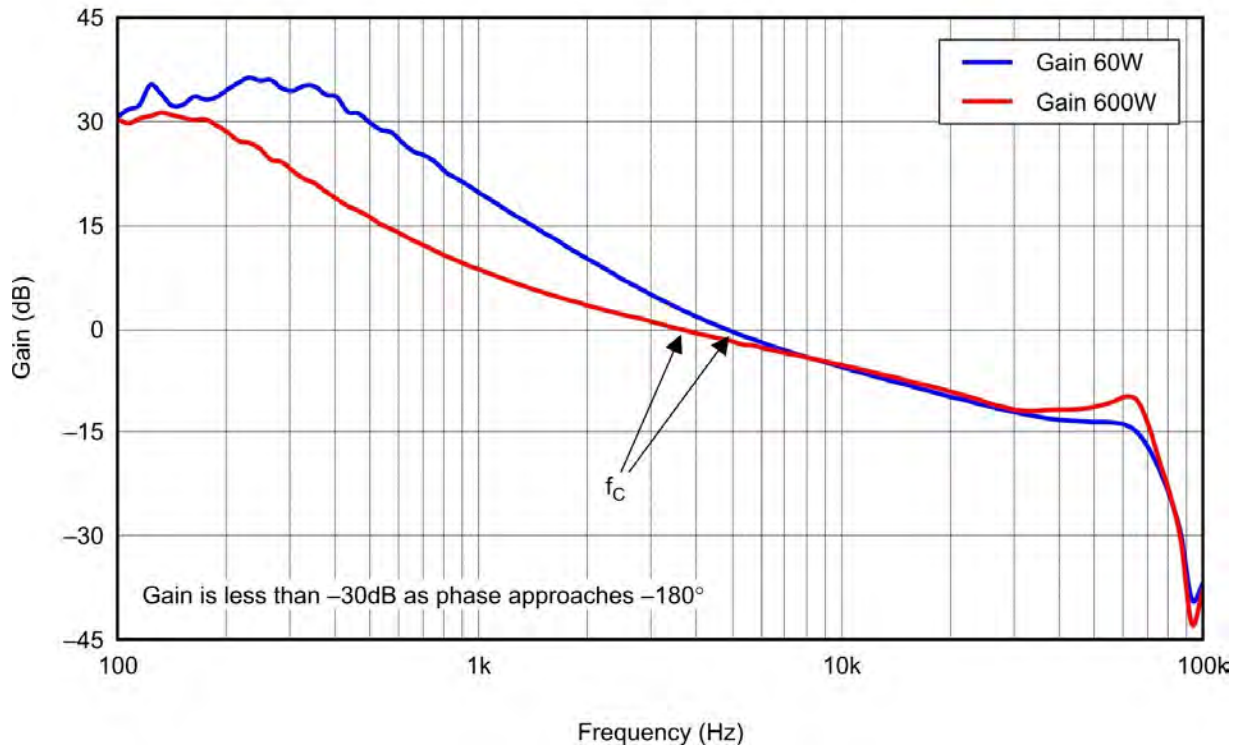

Figure 7. TV(f) loop gain in dB.

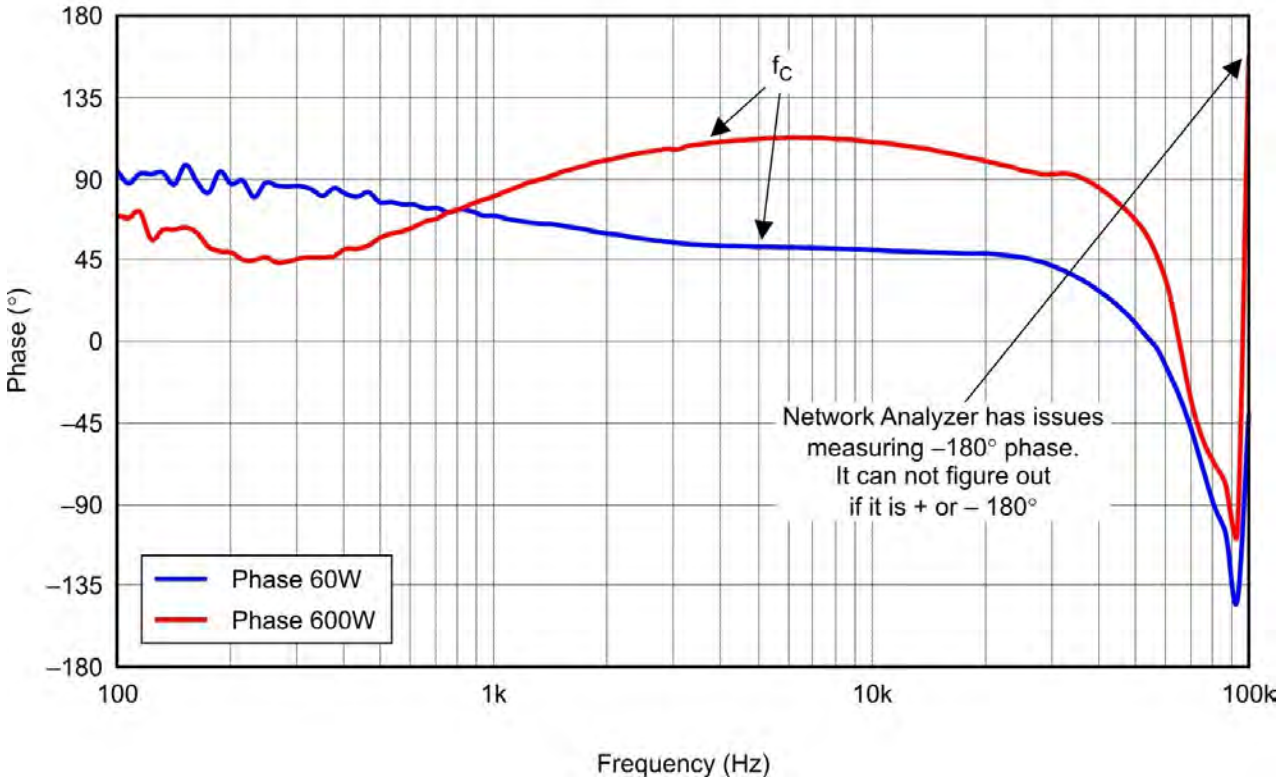

Figure 8. TV(f) loop phase in degrees.

Misconception

Speeding up the small-signal voltage loop $T_V(f)$ reduces the output capacitor bank. Remember there is an inductance in most switched-mode power supplies somewhere that will resist sudden changes in current. Large-signal current transients pass through C_{OUT} and the C_{OUT}'s R_{ESR}. To meet large-signal transient specifications requires selecting C_{OUT} and R_{ESR} to hold up and suppress large-current load transients.

The following equations should be useful in selecting the output filter capacitance required for the design. Variable $I_{TRANSIENT}$ is the large-signal instantaneous current load step, and variable dt is the amount of time the output capacitance is expected to suppress the large-signal transients. Variable $I_{AVERAGE}$ is the average current after the load step.

Worst case would be stepping from no-load to full-load conditions. These equations place 90 percent of the load-transient burden on the R_{ESR} and 10 percent on C_{OUT}.

$$R_{ESR} = \frac{V_{TRANSIENT} \times 0.9}{I_{TRANSIENT}}, C_{OUT} = \frac{I_{AVERAGE} \times dt}{V_{TRANSIENT} \times 0.1}$$

Conclusion

Over the years I have compensated many peak current-mode control voltage loops in power supplies. In the beginning, I struggled to get the control loops to cross over at much higher switching frequencies than necessary, only to have the loop become unstable due to the converter's double-pole frequency. The techniques presented in this paper for compensating these voltage loops saved me a lot of time and effort. I hope these techniques will provide the same benefits to you as well.

Reference:

Unitrode SEM 300, Topic 1, "Current-Mode Control of Switching Power Supplies," Lloyd H. Dixon, Jr, 1984.

About the Author

Michael O'Loughlin is an applications engineer with the Power Supply Control Products group at Texas Instruments. He specializes in offline and isolated power supply design and has authored numerous articles on power factor correction and power supply design related topics. Michael received his Bachelor of Science degree from the University of Massachusetts. Michael can be reached at ti_mikeoloughlin@list.ti.com.

For further reading on loop compensation, see the How2Power Design Guide, search the Design Area category and select Control Methods as the subcategory. To narrow your search, try entering keywords such as "control loop," "stability," or "compensation."