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SIMPLIS Simulation Tames Analysis of Stability, Transient Response, and Startup For DC-DC Converters

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In designing linear and switch-mode power supplies, engineers have long focused on the issue of load current transient demand and its impact on the power supply's output-voltage regulation and response characteristic. Many applications—based on ASICs, FPGAs, microprocessors and the like—have supply voltages whose levels are decreasing on an absolute basis and whose tolerance bands are decreasing on a percentage basis.

This trend is compounded by progressively increasing supply-current amplitudes and slew-rate demands. In many instances, an ASIC may be regularly commanded from its sleep state to its full rated current in such a short time and at such a high repetition rate that a severe burden is placed on the power supply. In these cases, it becomes critical that the supply exhibit a fast step-load transient response on its output voltage. That's needed not only to keep the output voltage within the ASIC's specification, but also for the cost and space savings promised if fewer output capacitors are required.

Against this backdrop, this article demonstrates a circuit simulation [1] of a non-isolated dc-dc converter that allows us to explore the converter's load-transient behavior, control-loop stability and output-voltage startup characteristic (all of which are interrelated). The simulation, which is based on a full time-domain, non-linear, switching model of the converter, is essentially a "virtual prototyping" tool that gives the designer several well-known benefits. Among these are fewer PCB spins, early identification of design errors, shortened design time, and ultimately, reduced engineering cost.

Aside from the simplicity and flexibility of the simulation process described here, its convenience renders it viable for everyday use by the practicing power electronics engineer. With this approach, there's no need to derive averaged models of the converter or identify the current-loop sampling gain contribution!

This simulation method accommodates circuit non-idealities, including error amplifier finite gain-bandwidth characteristic and switch minimum on-time constraints, using small-signal ac analysis simulation to produce meaningful bode plot results up to half the switching frequency. The output voltage waveform in response to a load transient can then be simply determined with time-domain simulation using the same model. The key benchmarks of output transient performance—peak deviation and settling time—are readily obtained. Finally, with this simulation method, the startup characteristic can be scrutinized as it pertains to soft-start time, output voltage waveform monotonicity, and pre-bias startup compatibility.

A Regulator Case Study

A fixed switching frequency, naturally-sampled, peak current-mode controlled converter is shown in Fig. 1. This particular design example employs a commercially available PWM synchronous buck regulator [2] operating in continuous-conduction mode (CCM) with a purely resistive load. Note that the parasitic resistances of the filter inductor and output capacitor, R_{dcr} and R_{esr}, are denoted explicitly in Fig. 1.

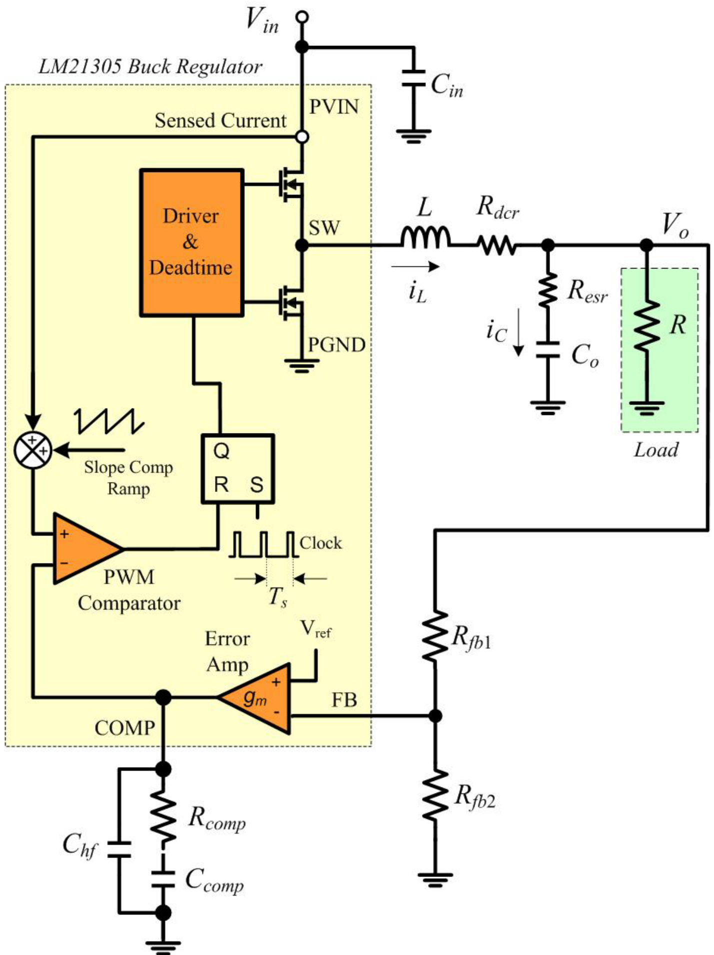


Fig. 1. The power train of an LM21305-based dc-dc synchronous buck regulator employs a peak current-mode PWM control loop structure and a transconductance error amplifier with type-II voltage loop compensation.

The outer voltage loop employs a type-II voltage-compensation circuit and conventional operational transconductance error amplifier (EA) with its inverting input, labeled the feedback (FB) node, connected to feedback resistors R_{fb1} and R_{fb2}. A compensated error signal appears at the EA output (COMP), the outer voltage loop thus providing the reference command for the inner current loop.

As illustrated in Fig. 1, a slope-compensation ramp of amplitude V_{slope} is added to the sensed current to lessen the risk of subharmonic oscillation. The associated quality factor, Q, and slope-compensation parameter, m_c, of the current-mode structure are defined as [3, 4]

$$Q = \frac{1}{\pi(m_c D' - 0.5)}. \quad (1)$$

$$m_c = 1 + \frac{S_e}{S_n}. \quad (2)$$

where S_e is the slope-compensation ramp slope and S_n is the off-time slope of the sensed-current signal. S_n is the duty-cycle complement. The circuit operating conditions, key component values and control circuit parameters relevant to the LM21305 regulator example are specified in Table 1.

Table 1. LM21305 buck converter parameters.

V_{in}	12 V	R_{dcr}	9 mΩ	C_{bw}	32 pF
V_O	3.3 V	R_{esr}	2 mΩ	V_{slope}	0.2 V
$I_{O(max)}$	5 A	$R_{ds(on)HS}$	44 mΩ	S_e	0.10 V/µs
L	3.3 µH	$R_{ds(on)LS}$	22 mΩ	S_n	0.13 V/µs
C_O	100 µF	g_m	2 mS	m_c	1.76
f_S	500 kHz	R_{oEA}	880 kΩ	Q	0.42

SIMPLIS Circuit Simulation

Using the parameters from Table 1, a SIMPLIS switching model circuit simulation is presented in Fig. 2. Fortunately, just one SIMPLIS model is sufficient to inspect the small-signal control system, large-signal transient response, and startup characteristic.

A few subtle details in the simulation model are worth detailing. The EA is implemented using a controlled source known as a voltage-controlled current source (VCCS) with built-in limiter function to conveniently define the EA sink and source current capability of ±250 µA. The high-side switch current is sensed by a current-controlled voltage source (CCVS) with gain of 50.54 mΩ. The minimum high-side switch on-time is set to 60 ns by the clock pulse-width that sets the PWM latch.

Slope compensation is achieved using a 0.2-V sawtooth ramp synchronized to the clock. Soft-start function is implemented by feeding 10 µA into soft-start capacitor C_{ss} connected to the EA non-inverting input so that the reference voltage ramps linearly until it reaches 0.6 V. The low-side FET is operated in diode-emulation mode during startup such that the device is gated off when the inductor current ramps down to zero. The inductor current is sensed by looking at the voltage across its DCR and the low-side drive is terminated by AND gate U2.

The output rail is diode connected to a pre-bias voltage source. The pre-bias voltage source minus the diode drop sets the output voltage pre-bias level. The output filter capacitor is a level 3 model representing a 100-µF 1210 ceramic with 2-mΩ ESR, 0.3-nH ESL, and 1-MΩ leakage resistance. Finally, variables ‘A’ and ‘B’ are included in the values of R_{fb2} and C_{comp}, respectively. Both ‘A’ and ‘B’ default to unity but can take on a range of values to sweep the relevant component value in a multi-step analysis simulation run.

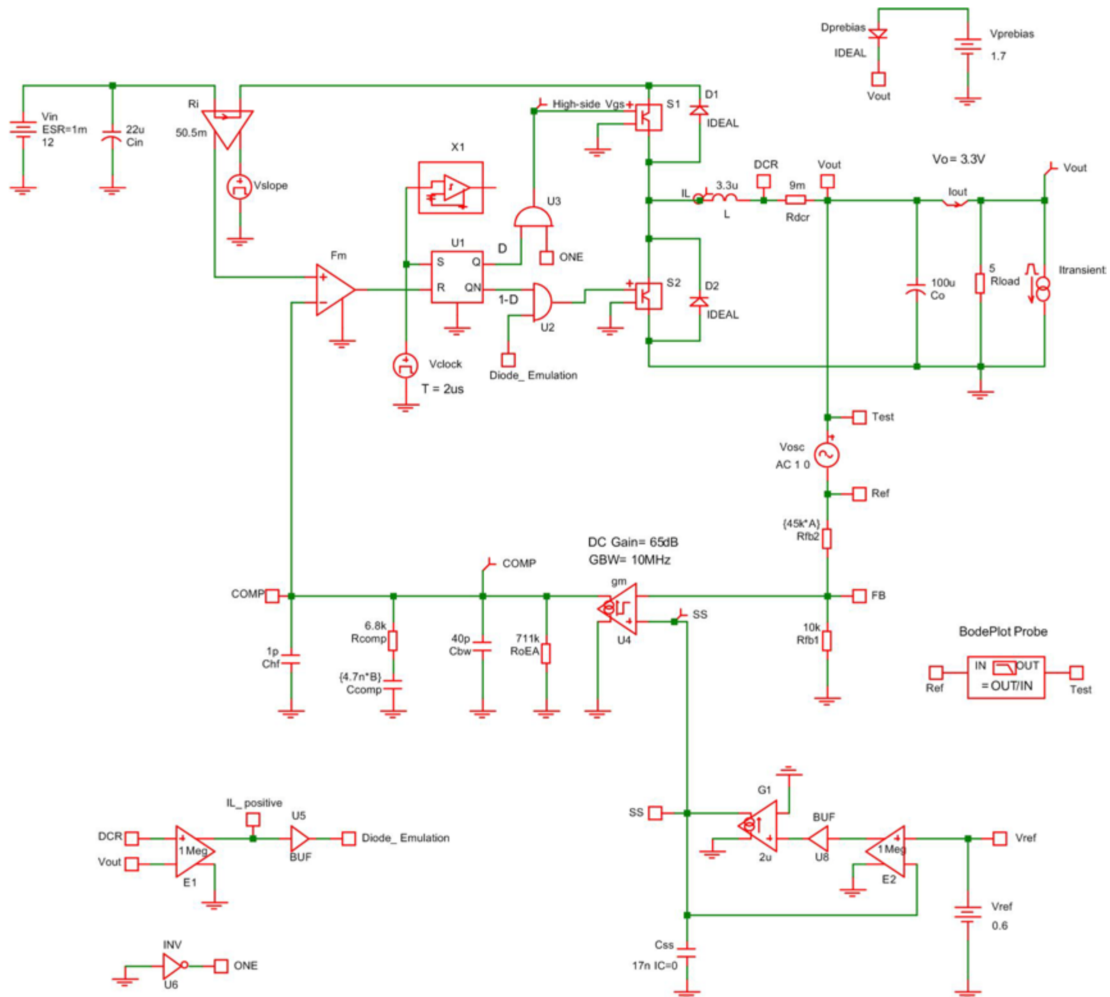


Fig. 2. A SIMPLIS model used to perform ac and transient analyses of an LM21305-based buck converter.

Any relevant transfer function of the converter system can be measured by breaking the loop at the upper feedback divider resistor, injecting a variable-frequency oscillator signal, and analyzing the frequency response at the appropriate nodes—exactly the same steps as required in a practical measurement.

The element with reference designator X1 in Fig. 2 is the SIMPLIS clock-edge trigger, which is used to find the circuit periodic operating point (POP) before running the ac analysis. POP analysis works on the full non-linear switching time-domain model of the circuit and enables the subsequent ac or transient analyses. The ac source with reference designator V_{osc} in Fig. 2 is the input stimulus for the ac amplitude. This source is automatically controlled during simulation to keep the ac response in the linearized small-signal region.

Loop Stability

A type-II compensator using an EA with transconductance, g_m, is shown in Fig. 2. The dominant pole of the EA open-loop gain is set by the EA output resistance, R_{oEA}, and effective bandwidth-limiting capacitance, C_{bw}. The EA bandwidth is modeled in the simulation by capacitor C_{bw} so that the open-loop bandwidth is

$$f_{EA-BW} = \frac{g_m}{2\pi C_{bw}}. \qquad (3)$$

The compensator transfer function from output voltage to COMP is a two-pole, one-zero expression given by [4]

$$G_c(s) = \frac{\tilde{v}_{comp}(s)}{\tilde{v}_{out}(s)}.$$

$$\cong -\frac{R_{fb1}}{R_{fb1}+R_{fb2}} \frac{g_m R_{oEA}(1+sR_{comp}C_{comp})}{(1+sR_{oEA}C_{comp})(1+sR_{comp}(C_{hf}+C_{bw}))}. \qquad (4)$$

The reader interested in a detailed treatment of peak current-mode compensation strategy and current-mode system loop gain can refer to [3]. Note that capacitor C_{hf} is sometimes not installed, allowing the EA itself to solely provide high-frequency attenuation by virtue of its finite gain-bandwidth. The simulated frequency response of the compensator is given in Fig. 3. The EA has an open-loop dc gain of 65 dB and a 10-MHz single-pole gain-bandwidth characteristic. The 180° phase lag related to the EA in the inverting configuration is not included in the phase plots. The low-frequency compensator pole, compensator zero, and high-frequency compensator pole are plainly apparent.

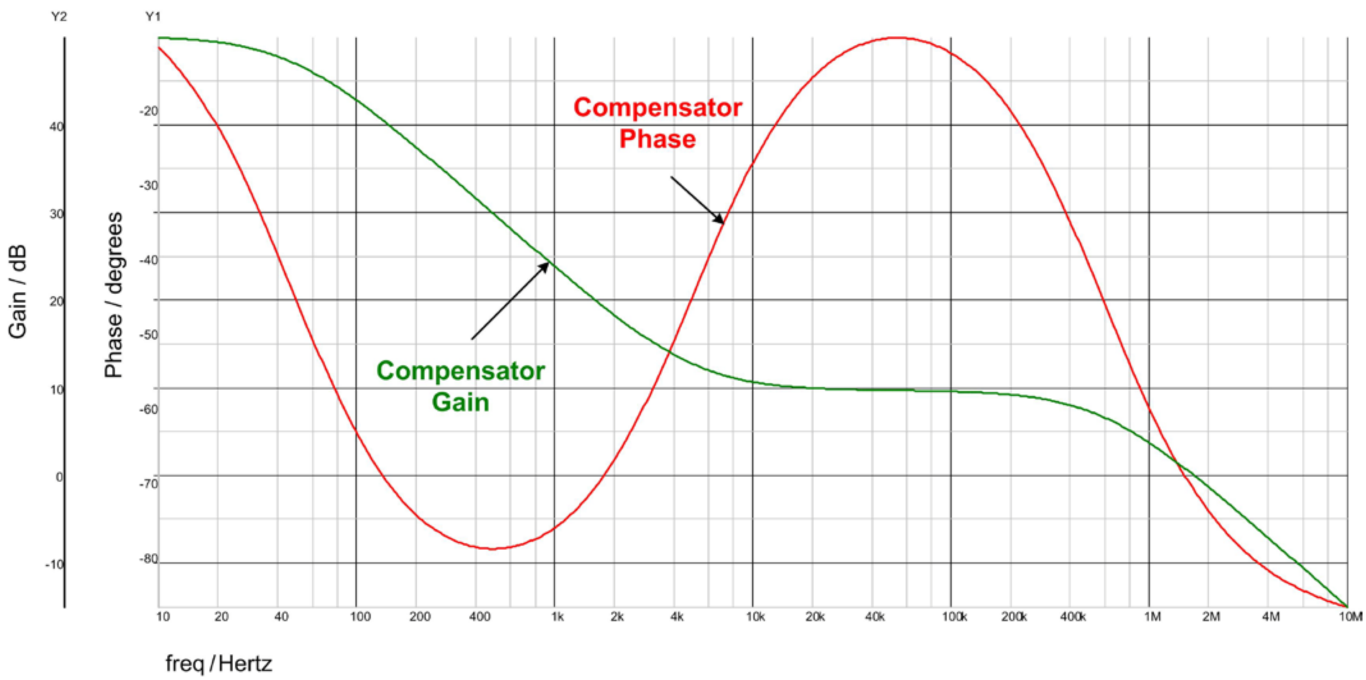


Fig. 3. Bode plot simulation result of compensator transfer function, Gc(s).

Fig. 4 illustrates the simulated loop gain and phase plot of the exemplified converter. The crossover frequency is 70 kHz and the phase margin (the difference between the loop phase and –180°, EA inversion phase lag notwithstanding) is 51°.

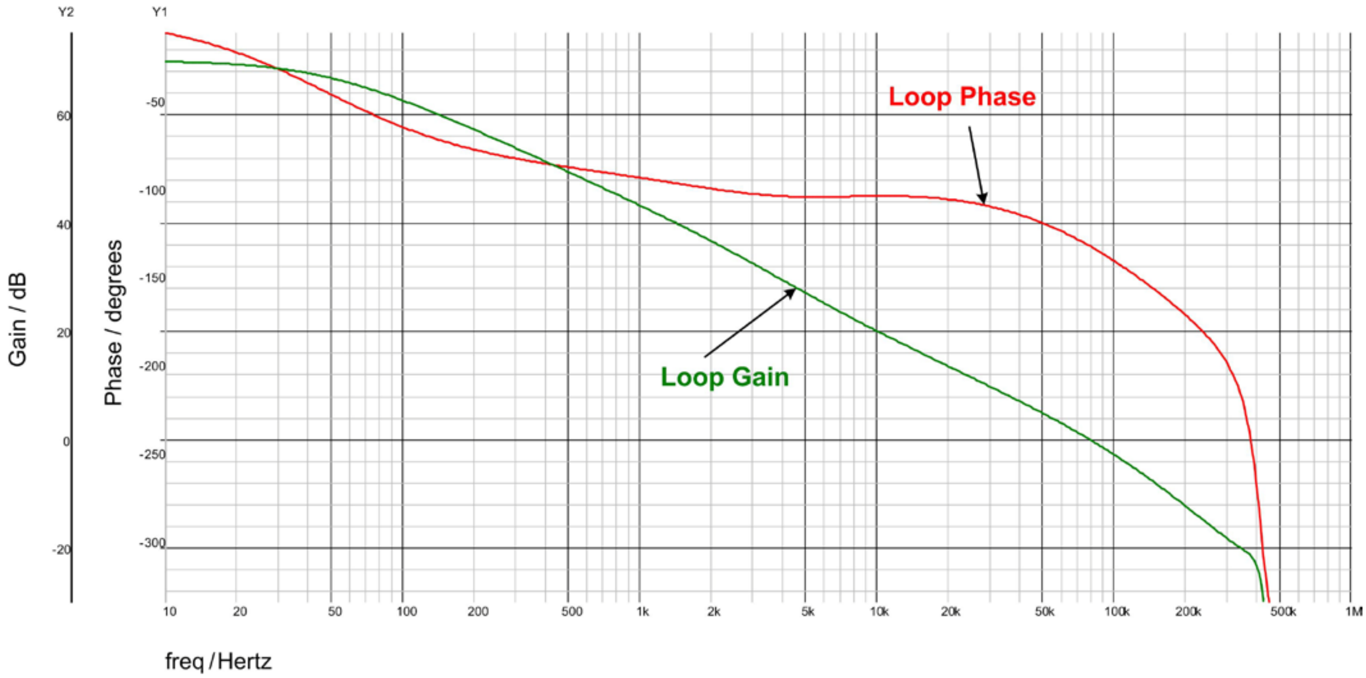


Fig. 4. Bode plot simulation result of loop small-signal transfer function, T(s).

Fig. 5 illustrates the simulated bode plot of the COMP-to-output transfer function. The sampling-gain term of the current loop contributes the steep phase roll-off at high frequencies. The load pole is clearly discernible. Assuming no reduction in output capacitance with applied voltage, its ESR zero is located at 800 kHz so its effect is irrelevant. The voltage coefficient of ceramic capacitors, however, can be quite substantial and the actual capacitance at the frequency of interest should be experimentally characterized.

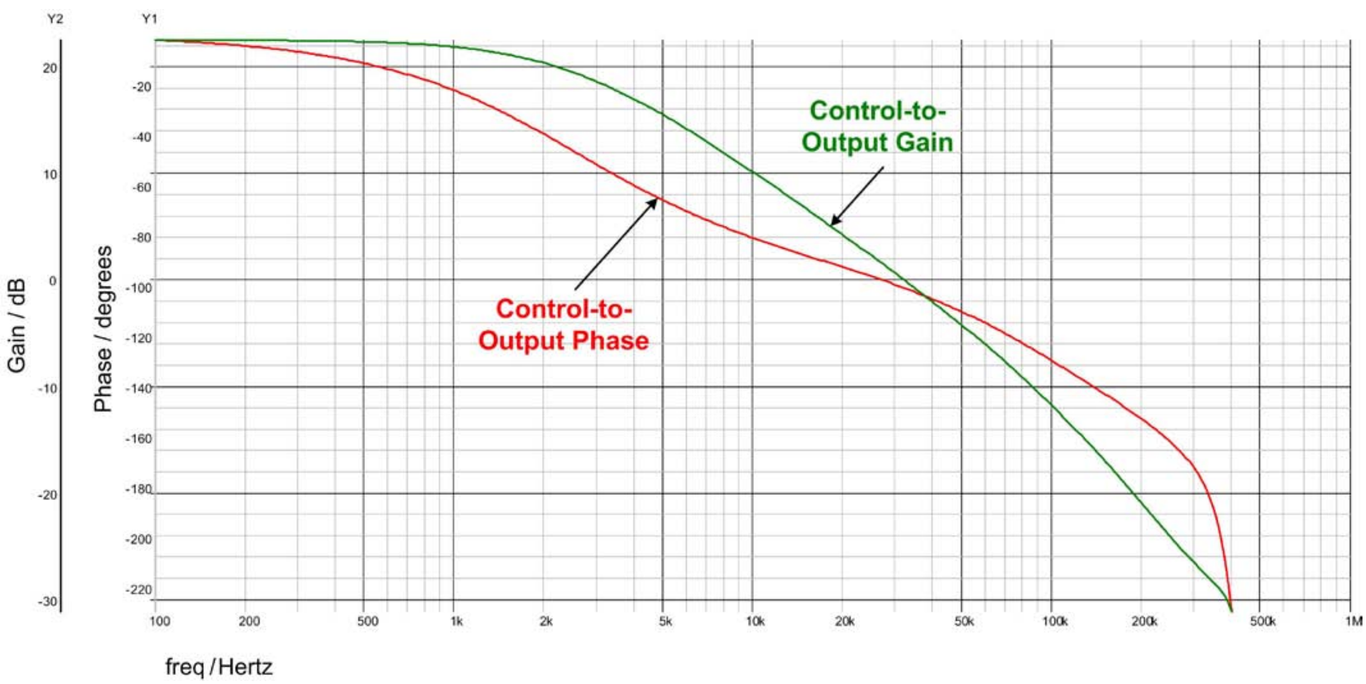


Fig. 5. Bode plot simulation result of control-to-output small-signal transfer function, C-O(s).

As evident in equation 4, the penalty for using a transconductance-type EA is that both feedback resistors, R_{fb1} and R_{fb2}, factor into the compensator gain. The loop crossover frequency, all else being equal, will decrease as the output voltage increases. A multi-step simulation run is performed to measure the loop gain with the output voltage setpoint at 3.3 V, 1.8 V and 1.2 V. Using variable 'A' as a scale factor for the upper feedback resistance, R_{fb2}, the output voltage is set before each simulation run. The results are plotted in Fig. 6. The crossover frequency at 1.2-V output is 133 kHz, but the phase margin erodes to 29°.

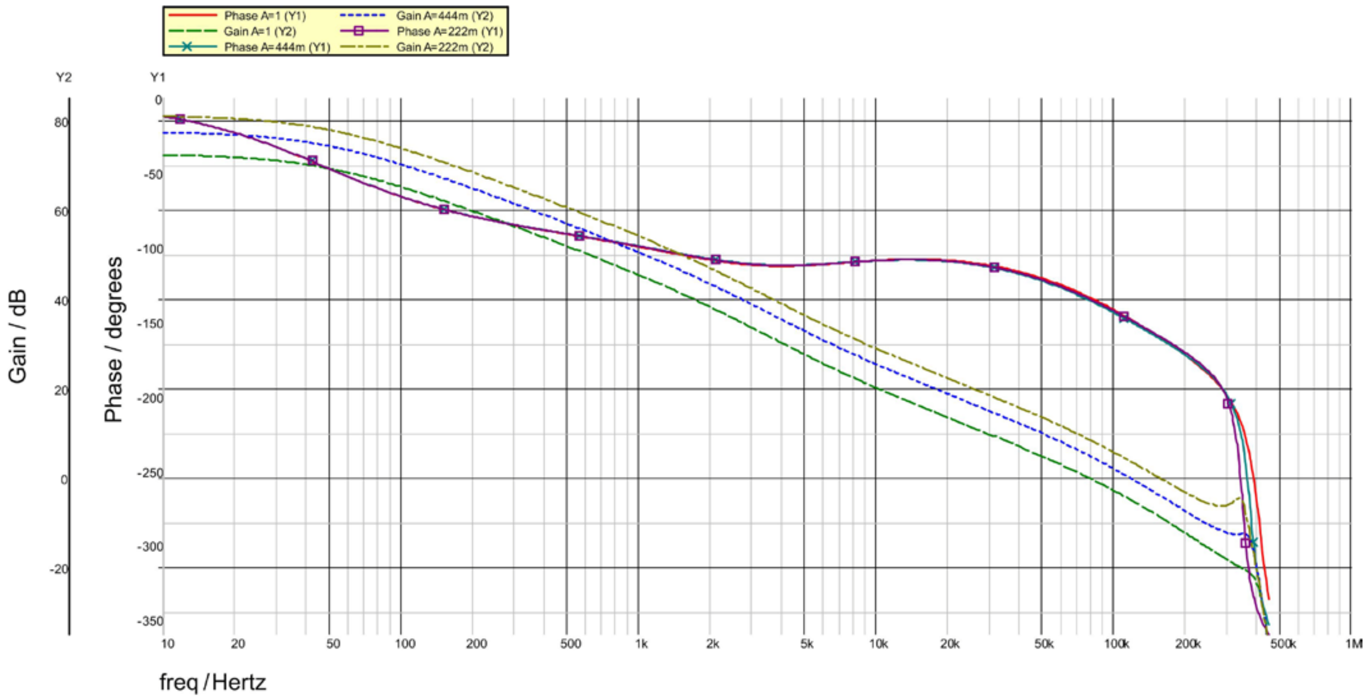


Fig. 6. Bode plot simulation result of loop transfer function, T(s), with output voltage of 3.3 V, 1.8 V and 1.2 V.

The implication is twofold: the compensation may need retuning if the output voltage changes; the performance is impaired if a module-style converter with wide output range is required. In contrast, if an op-amp type EA is employed, the FB node is effectively at ac ground and R_{fb2} bears no influence on the loop dynamics. The compensator transfer function is not dependent on output-voltage setpoint.

Load Transient Response

Using a SIMPLIS time-domain transient analysis, load-on and load-off transient responses are obtained as shown in Fig. 7. The load step is from 1 A to 5 A at 4 A/μs. The output voltage, output current, inductor current, COMP, and high-side switch drive waveforms are plotted. The peak deviation is 100 mV and settling time is 30 μs.

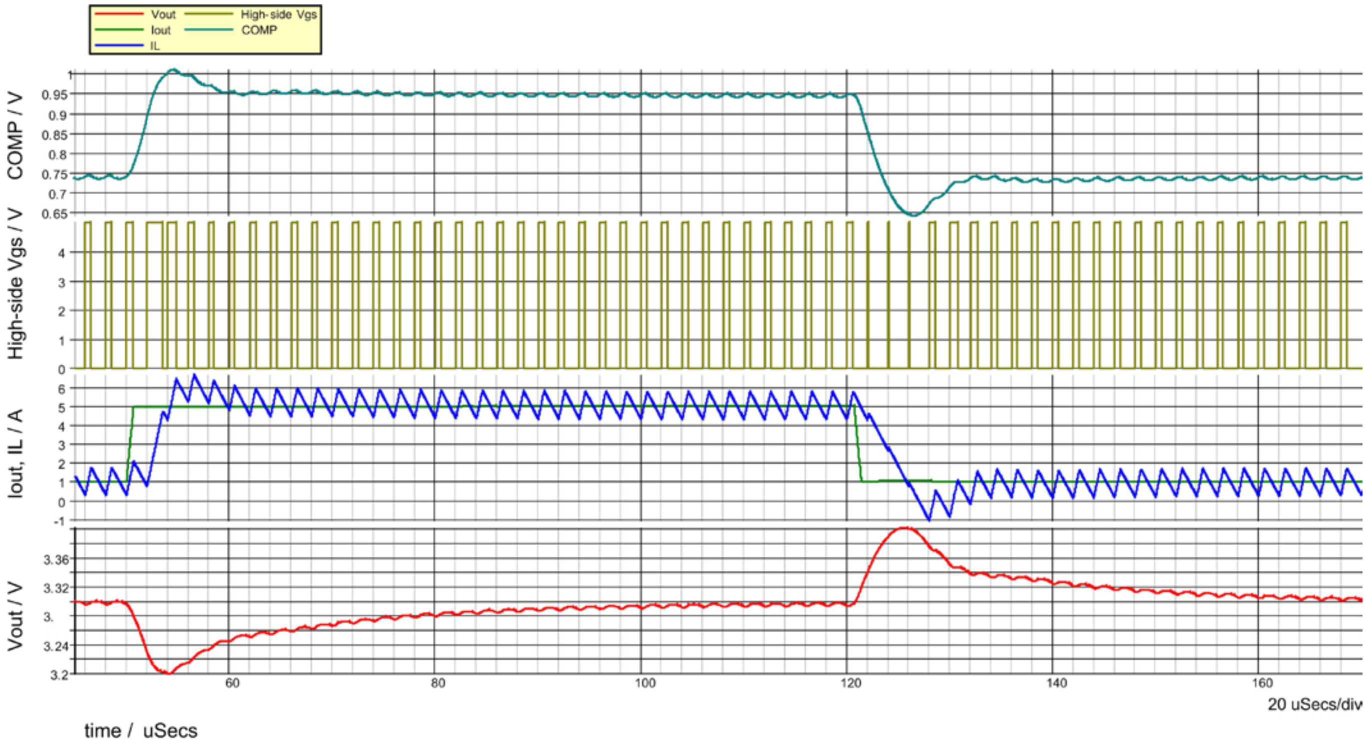


Fig. 7. Load-on step transient simulation with high-side gate drive and COMP waveforms.

The compensation zero frequency represents the dominant time constant in a load transient response characteristic [4]. A large C_{comp} capacitance is thus antithetical to a fast transient response settling time. C_{comp} can be reduced, however, to tradeoff phase margin and settling time. A phase margin target of 50° to 60° is ideal and it is found that the compensator zero is optimally located above the load pole but below the power stage resonant frequency.

$$\frac{1}{\omega_p R_{comp}} \le C_{comp} \le \frac{1}{\omega_{LC} R_{comp}};$$
$$\omega_{LC} = \frac{1}{\sqrt{LC_o}}; \omega_p \cong \frac{1}{R_{load} C_o} \qquad (5)$$

Of course, a smaller compensation capacitance is also advantageous if the transconductance EA has a low output drive current capability. Load-on and load-off transient responses are obtained with high (6.8 nF) and low (2.7 nF) compensation capacitor values chosen so that the compensator zero is located directly at the load pole and the power-stage resonant frequencies, respectively. Using variable 'B' as a scale factor for C_{comp}, the compensator zero is set before each simulation run. The results are plotted in Fig. 8.

It is evident that the lower value of compensation capacitance results in a much more favorable settling time. Interestingly, this is achieved with very little relative change in the bode plot. There's approximately 1-kHz decrease in crossover frequency and 4° less phase margin with the 2.7-nF capacitor than with the 6.8-nF capacitor.

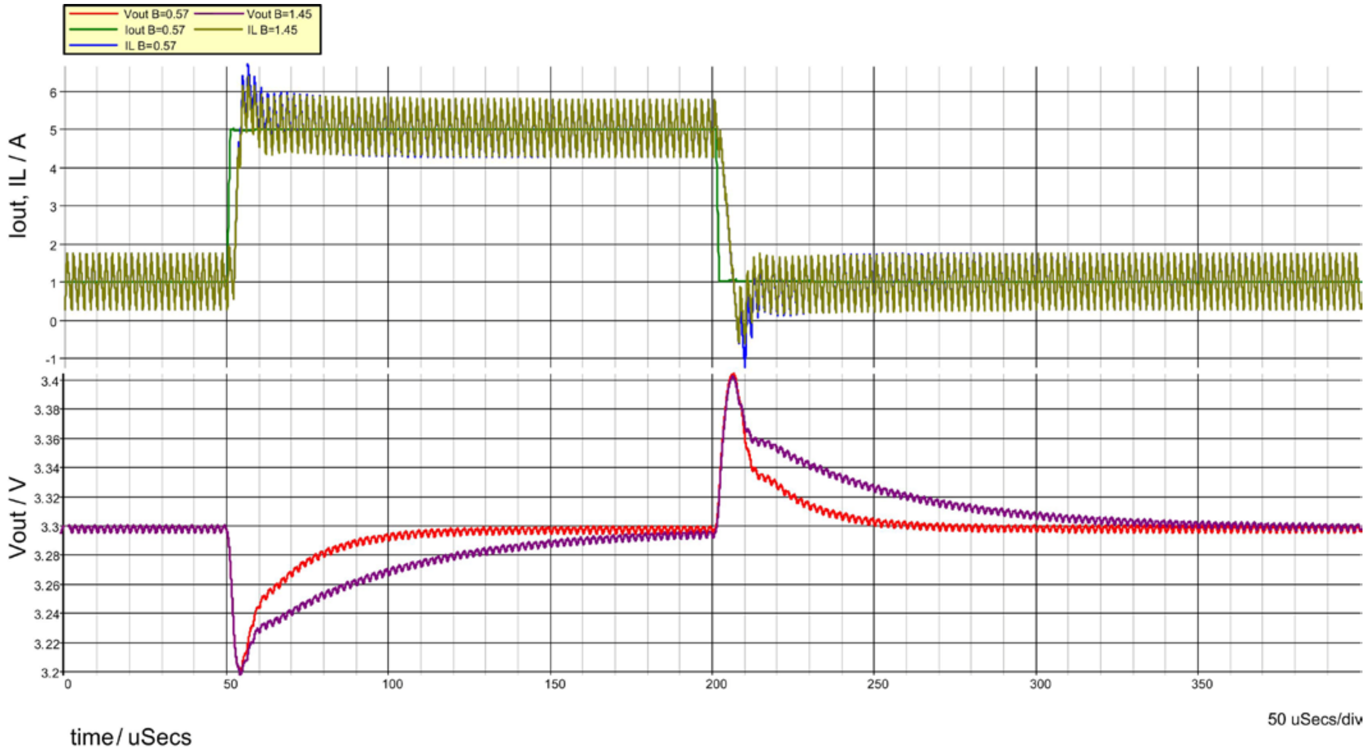


Fig. 8: Load step transient response simulation with two values of compensation capacitance.

Startup

To obtain the output-voltage startup characteristic, a SIMPLIS time-domain transient analysis is run with the initial condition of the output capacitor voltage set to zero and the POP analysis not selected to run. The soft-start time is 1 ms and startup is into a 0.66-Ω resistive load. The output-voltage waveform is monotonic during the entire ramp time with no dips or flat spots as shown in Fig. 9. Note the transition from diode-emulation mode to fully synchronous operation once the soft-start interval has expired.

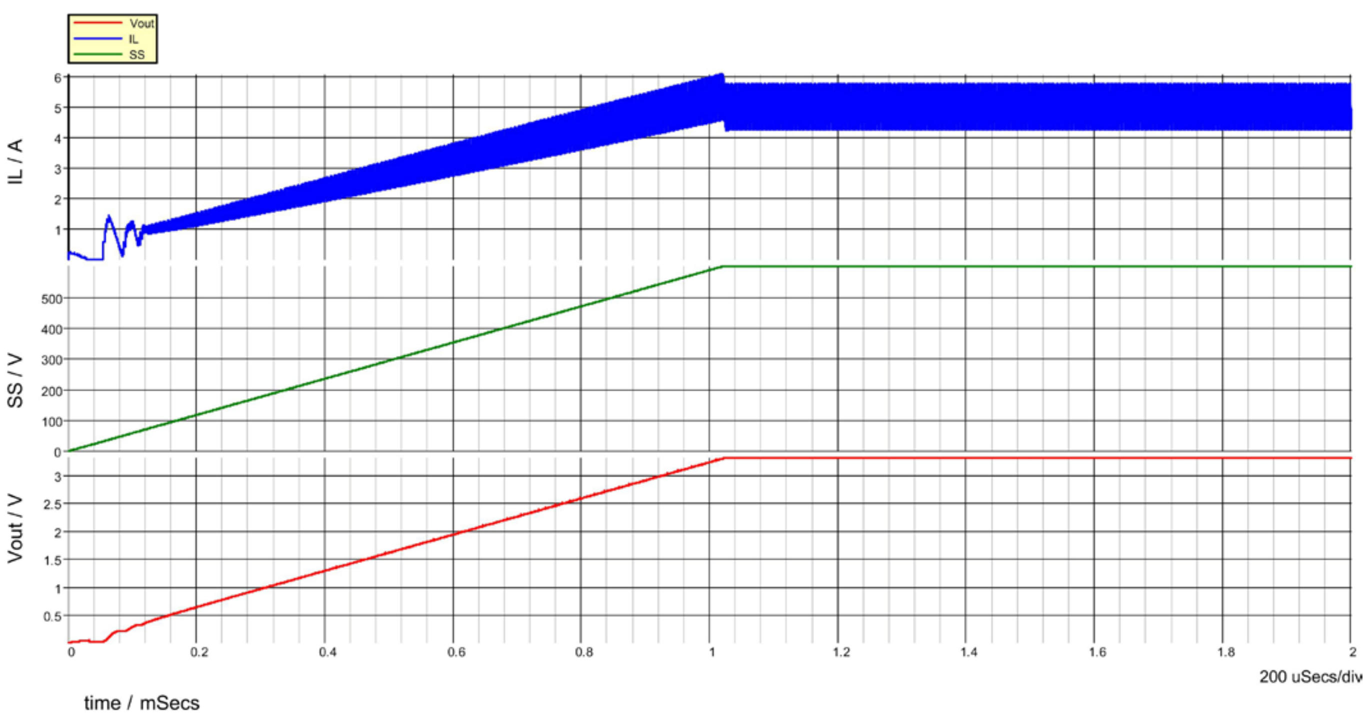


Fig. 9. Startup simulation.

Fig. 10 demonstrates pre-bias startup compatibility. Again, the output-voltage waveform is monotonic during the startup ramp from the pre-bias level of 1.0 V to the steady-state operating point of 3.3 V. Perhaps more important, as the low-side FET operates in diode-emulation mode during startup, negative inductor current is prevented and the regulator does not sink current from the output rail.

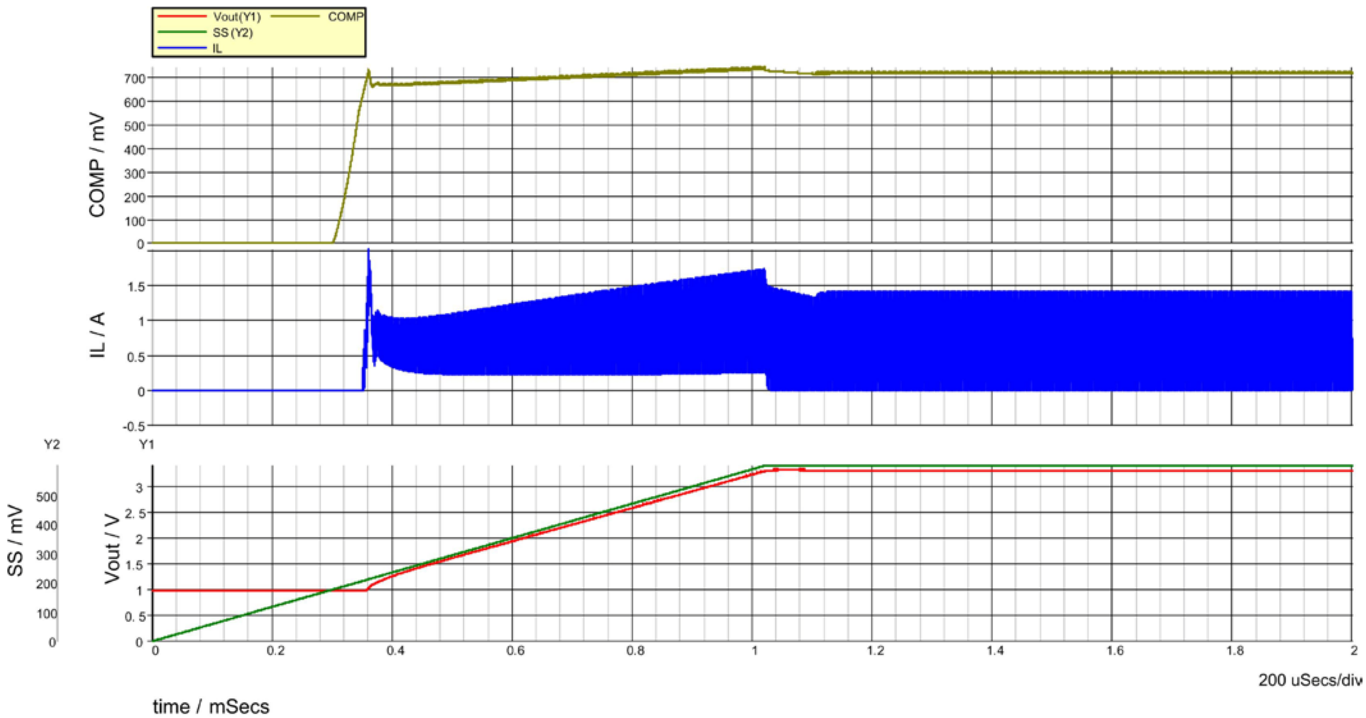


Fig. 10. Startup simulation with 1.0-V pre-biased output.

References:

1. SIMPLIS Technologies Advanced Power System Simulation, Rev 6.0, www.simplistechnologies.com

2. Product datasheet for National Semiconductor's LM21305 5A Adjustable Frequency Synchronous Buck Regulator from the PowerWise Family, http://www.national.com/pf/LM/LM21305.html.

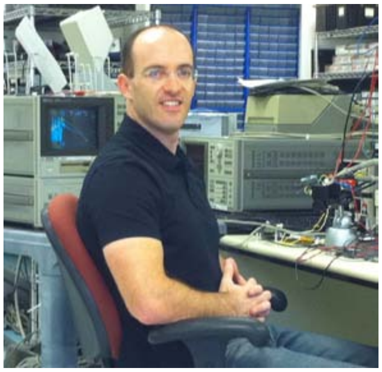
3. Robert Sheehan, National Semiconductor, 'Current-Mode Modeling – Reference Guide', http://www.national.com/analog/power#appnotes.

4. Timothy Hegarty, National Semiconductor, 'Peak Current-Mode DC-DC Converter Stability Analysis', http://powerelectronics.com/power_management/regulator_ics/peak-current-mode-dc-dc-201006.

Further Reading:

National Semiconductor's Webench Power Designer, http://www.national.com/analog/webench/power.

About the Author



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