ISSUE: September 2010

Debunking An Old Myth: Those New Devices Will Fall Off The Board

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In the bad old days, perhaps ten to fifteen years ago, leadless semiconductor packages were something to avoid in the power electronics world. By "leadless," we mean packages with no protruding pins, not to be confused with lead-free packages, which do not contain any lead (Pb). The "forbidden" leadless packages were the BGAs, flip chips, and what we now know as the PQFN packages.

Back then, you needed the leads protruding from the package for a little compliance. The coefficient of thermal expansion (CTE) for the plastic package was fairly different from that of the system consisting of the printed circuit board (PCB), traces and solder. Without leads that could flex a little bit, eventually the solder would fracture and failure would ensue.

But times have advanced as have the materials. The issue of CTE mismatch is no longer a reason to forego using leadless packages. Nevertheless, when semiconductor FAEs like myself recommend these packages to customers, we still hear this response: "We can't use THOSE devices—they will fall off the board."

To assure customers that the leadless devices are safe, I've investigated the CTEs of packaging and board materials. My findings are summarized in this article.

Eliminating CTE Uncertainty

In a way, the customer's response is certainly understandable. As a designer, I avoided the first few waves of leadless parts for these same reasons. The CTE of the mold compound was never specified in the datasheet. For good reliability over many thermal cycles, we'd clearly want the CTE of the mold compound of a leadless device to match that of the PCB, which brings up another question: What then is the CTE of the circuit board material and the copper traces on it?

Back when I designed consumer electronics equipment, I used to watch 6-in. wide PCBs on phenolic material go through a wave-soldering process and come out hot at 6.1-in. wide. That CTE was prohibitively large in most any high-reliability application. But that was a different world. Today modern mold compounds and PCB materials have CTEs that are much more closely aligned.

The table below presents a summary of the CTE values for the mold compound for older parts with leads and pins, newer leadless parts, and PCB materials. I gathered this information from the mold compound vendors and Coomb's PCB handbook, and then cross checked it with a couple of PCB manufacturers.

As listed in the table, the CTE of the mold compound of a typical through-hole device is approximately 90 ppm/°C. The CTE of the PCB, solder and traces is between 15 and 20 ppm/°C. That would be a huge difference without compliant leads. For example, if the useable junction temperature range of a through-hole device was -40°C to +125°C, then a 1-in. device mounted on a 1-in. PCB would differ by as much as 0.010 in. over this temperature range. A lead could easily absorb this difference, but a rigid plastic package could not. Eventually, after enough thermal cycles, a leadless package with this mold compound would overstress the solder joints and the connections would fail. In an extreme case, the device might simply fall off of the PCB.

The good news is that the leadless plastic packages have accounted for this concern. The CTE for the PQFN-type packages is between 8 and 12 ppm/°C. The DirectFets are 17 ppm/°C. This matches the PCB and traces very well in most any FR4 application.

Table 1. Coefficients of thermal expansion for semiconductor packaging and PCB materials

Applicable Device Package	Material Function	Material Name	CTE (ppm/°C)	Notes
3-mm x 3-mm, 5-mm x 6-mm plastic quad flat no-lead (PQFN) with copper clip	Mold compound	Sumitomo E670	12	
3-mm x 3-mm, 5-mm x 6-mm plastic quad flat no-lead (PQFN) with bond wires	Mold compound	Hitachi CEL-9220	8	
D^2Pak, TO-220, some SOICs and DIPs	Mold compound	MG15F	90	
Leads, pins, PCB trace conductors	PCB trace conductor (copper)		17	
FR4 PCB dielectric material	PCB material	FR4	15-20	Includes pre-preg., Higher glass content yields lower CTE, Higher resin content yields higher CTE
Phenolic PCB dielectric material	PCB material	Phenolic	60-200	Depends on composition
DirectFET	DirectFet can material	Copper alloy	17	
DirectFET	DirectFet pad material	Copper alloy	17	
Any	Silicon device die	Silicon	2.6	
Any	Die-attach compound	Thermally/electrically conductive epoxy	40-120	
	Solder (95.8% tin, 3.5% silver, 0.7% copper)	Lead-free solder	21	

About The Author

Paul Schimel was raised on the banks of the mighty Des Plaines River in the southern suburbs of Chicago, Illinois. By his mother's account, he was apparently abducted by hungry wolves and raised in a doorless barn at an early age. In spite of this claim, he started his engineering career at the age of 5 when he managed to muster enough purchase on a screwdriver to unscrew the cover to the service panel and prod around with a stainless steel kitchen fork. He was revived in an ambulance shortly thereafter.

Two weeks later, he did it again, thus determining that there were two hot sides and one neutral with respect to the steel freezer that he was standing on for the test. (He couldn't discriminate phase with his instrumentation.) From there he went on to investigate just about everything that's been put together.

He was in the positive (making stuff work) by age 11, spending most of his free time working on things in the back alleys of Cicero, Ill. with mentors and childhood buddies. He was working conventional machine tools and welding by 14. Through high school, he fixed most anything that was breakable including yard equipment, two-way radio gear, power tools, TVs, and stereos. He attended the School of Electrical Engineering at the University of Illinois at Urbana Champaign, specializing in power electronics where he earned a BSEE degree and had his hands in every power electronics project that the department was doing including the Hybrid Electric Vehicle and the Sunrayce Solar Powered Car.

After this, he went on to spend eight years in successful design engineering roles in consumer equipment including power supply design for projection and direct view televisions and telecommunications equipment including ring generators, battery rectifiers/eliminators, dc-dc converters, and UPSs—both switch-mode and ferroresonant. His design work encompassed prototypes, PCB layout, magnetics design, electronic design, debug, thermal management, EMC testing, safety agency approvals, mechanical design, and design for mass production.

He then moved on to field applications engineering where he has spent the last six years on power management support and design work for Unitrode/TI, Fairchild and International Rectifier. He has assisted successful designs from mW to MVA and from prototype stages to finished end equipment. He moonlights in broadcasting, antique test equipment restoration, metal working, wood working, TIG welding, loudspeaker building, and amateur radio (K5NJP). He holds a commercial radio telephone license, a refrigeration license, and he is a licensed PE.

The vast majority of folks that purport themselves as having technical knowledge need two hours to explain what they do. When Mr. Schimel is asked the same question, he says "I make stuff go. Circuits, cars, trains, air conditioners, motors, relationships, plumbing, whatever it is…I make it go!"

Mr Schimel holds several patents on magnetic structures for power electronics and novel circuitry. He has published several hands-on type articles in Power Electronics Technology, EDN, RSES, QST and various other trade publications. He has been a senior field applications engineer at IR for the last three years and he enjoys it immensely

For further reading on power semiconductor packaging, see the How2Power Design Guide, select the Design Area category and search the Packaging and Interconnects subcategory.