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How2 Understand eGaN Transistor Reliability

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Efficient Power Conversion's (EPC) enhancement-mode gallium-nitride (eGaN) power transistors, although similar to standard power MOSFETs, deliver performance unattainable by silicon-based devices. EPC power transistors offer standard power converter topologies added performance and improved efficiency while maintaining the simplicity of older designs. EPC's risk-reduction results to date include the placement of over 760 devices, at their maximum operating ratings, in a wide variety of stress tests. Over 950,000 total device hours of reliability testing validates the readiness of eGaN transistors to supplant their silicon counterparts for power switching applications.

Overview Of Reliability Test Results

The key reliability considerations for power transistors include: (a) device stability in the on-state when the transistor is fully enhanced with voltage applied on the gate; (b) device stability in the off-state when the transistor is in voltage-blocking mode withstanding up to its rated drain-source voltage; and (c) device stability in switching operation. Device stability is impacted by device design, packaging technology, and operating environment. Good reliability results, based on millions of device hours under stress, have been reported for depletion-mode GaN HEMTs (high electron mobility transistors) for RF applications [1-3] and power switching applications [4].

In June 2009, Efficient Power Conversion introduced the first enhancement-mode gallium nitride-on-silicon power transistors designed specifically as replacements for power MOSEFTs [5]. These high electron mobility transistors were subjected to a wide variety of stress tests under conditions that are typical for power MOSFETs used in switch-mode power conversion. These tests included:

- Stability under drain-source bias whereby parts were subjected to a drain-source voltage equal to the maximum rated voltage at the maximum rated temperature (high-temperature reverse bias, or HTRB)
- Stability under gate-source bias whereby devices were subjected to gate-source voltages at the maximum rated temperature (high-temperature gate bias, or HTGB)
- Temperature cycling (TC)
- Temperature and humidity, with bias from drain to source (THB)
- Operating life whereby parts were assembled onto power supply boards and subjected to actual dc-dc conversion operating conditions

Reliability test results are summarized in Table 1, in which the type of test, stress conditions, part numbers, sample size, stress hours, and number of failures are listed. JEDEC standards were followed when applicable.

Parts were mounted on FR408 adaptor cards and electrical parameters were measured at time zero. Interim readout points were all at room temperature. The underfill material used, where applicable, was Loctite FP4549Si.

As seen in Table 1, the eGaN transistor has demonstrated excellent reliability. At the time of this writing, over 760 parts were stressed for over 950,000 device hours of reliability testing with no failures. Over the entire stress period, device electrical parameters remained stable.

Several reliability issues with non-commercial GaN devices have been reported in the literature. Two major issues are current collapse (dynamic $R_{DS(ON)}$) [6-17] and gate-leakage degradation [18-21]. EPC's eGaN products were subjected to a wide variety of stress tests to validate they functioned reliably under

accelerated stress conditions and did not display noteworthy degradation as a result of the mechanisms reported in the academic literature.

Table 1. Summary of EPC's eGaN transistor reliability test results.

Stress Test	Test Condition	Part Number	Sample Size	# of fails	
				1000HR	3000HR
HTRB	100Vds, 125°C	EPC1001	45	0	-
HTRB	40Vds, 125°C	EPC1014	50	0	-
HTRB	200Vds, 125°C	EPC1012	50	0	-
HTRB	200Vds, 125°C	EPC1010 with underfill	50	0	-
HTRB	200Vds, 150°C	EPC1010	50	0	0

Stress Test	Test Condition	Part Number	Sample Size	# of fails	
				1000HR	3000HR
HTGB 5V	5Vgs, 125°C	EPC1001	45	0	0
HTGB 5.4V	5.4Vgs, 125°C	EPC1001	45	0	0
HTGB 5V	5 Vgs, 150°C	EPC1010	45	0	-
HTGB -5V	-5Vgs, 125°C	EPC1001	50	0	-

Stress Test	Test Condition	Part Number	Sample Size	# of fails	
				1000cys	
TC	-40C to 125°C	EPC1001	45	0	-
TC	-40C to 125°C	EPC1014	50	0	-
TC	-40C to 125°C	EPC1012	45	0	-
TC	-40C to 125°C	EPC1012 with underfill	45	0	-

Stress Test	Test Condition	Part Number	Sample Size	# of fails	
				1000HR	
THB	85°C/85RH, 40Vds	EPC1014	45	0	-
THB	85°C/85RH, 40Vds	EPC1015	45	0	-
THB	85°C/85RH, 100Vds	EPC1010	25	0	-
THB	85°C/85RH, 100Vds	EPC1010 with underfill	25	0	-

Stress Test	Test Condition	Part Number	Sample Size	# of fails	
				1200HR	
Power Supply Life Test	10A, 250 kHz, 30°C	EPC1001	10	0	-

Dynamic $R_{DS(ON)}$

Dynamic $R_{DS(ON)}$, also known as "current collapse", is a phenomenon whereby the drain current decreases as a result of electron trapping near the channel region (see the schematic of a GaN HEMT structure in Fig. 1.) The magnitude of current collapse is strongly dependent on the electric field at the gate edge where electrons can be accelerated [6]. Electrons may be trapped in the AlGaN/dielectric interface where they charge up the surface states, which then act as a virtual gate electrode. This can result in a reversible degradation of drain current [7].

Electrons can also be trapped in the AlGaN barrier layer itself or in the GaN buffer layer below. These high-energy electrons can also generate traps, further promoting charge trapping. The high electric field could also result in mechanical defects due to the inverse-piezoelectric effect, forming electrically active deep levels that trap electrons and cause a reduction of intrinsic carrier concentrations and the

maximum drain current [8,9]. The crystallographic defects and strain relaxation also lower the electron density in the region next to the gate, thereby reducing the current-carrying capability [10].

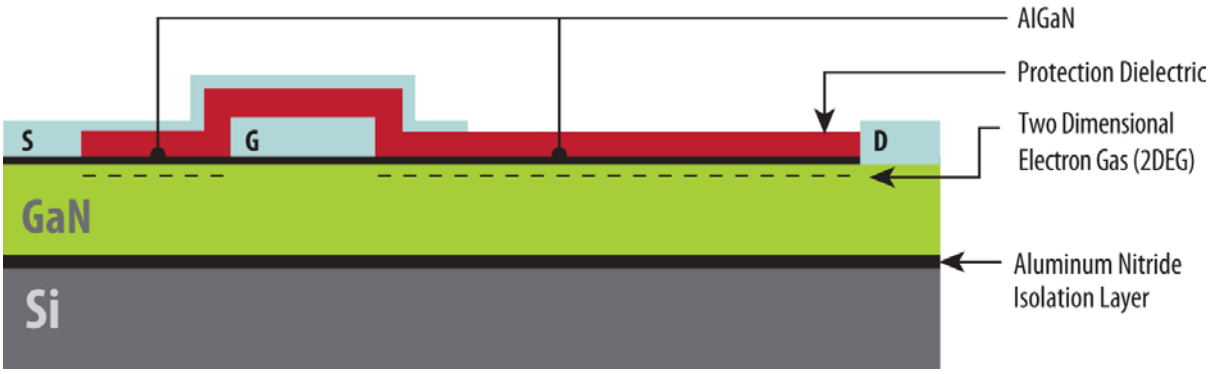

Figure 1. EPC's eGaN transistor structure (not to scale.)

Device design improvements using gate and source field plates are an effective way to reduce the electric field, thereby suppressing the increase in on-state resistance as well as gate-leakage degradation [6,11]. Surface passivation, or surface treatments, can also be effective at reducing the surface-trap density and thereby reducing hot-electron degradation [2-13]. The use of a conducting substrate acting as a backside field plate helps to mitigate electron trapping in the buffer region beneath the channel [6]. In addition, better confinement of electrons in the potential well and overall improvement in the material quality of AlGaN/GaN epitaxial layers are important to combat dynamic $R_{DS(ON)}$ [14-16].

EPC has taken steps in material growth, device design, and process optimization to minimize the potential device-degradation mechanisms [22].

Fig. 2 is an illustration of $R_{DS(ON)}$ over stress time of EPC1010 with the maximum drain-source voltage applied at an elevated temperature of 150°C (HTRB). Fifty EPC1010 devices were drain biased at 200 V in the stress chamber with gate and source shorted to ground. Device parameters were measured initially at time zero and at each interim readout point. The normalized $R_{DS(ON)}$ is the ratio of the post test value over the initial value for each device at each interim readout point. $R_{DS(ON)}$ was measured with 5 V on the gate and the source at ground potential. As can be seen, $R_{DS(ON)}$ stayed stable over the stress period of 3000 hours. As with EPC1010, a 200-V eGaN transistor, minimal $R_{DS(ON)}$ variation was observed in the 100-V (EPC1001) and 40-V (EPC1014) eGaN transistors on HTRB when biased with the rated drain-source voltage at an elevated temperature of 125°C.

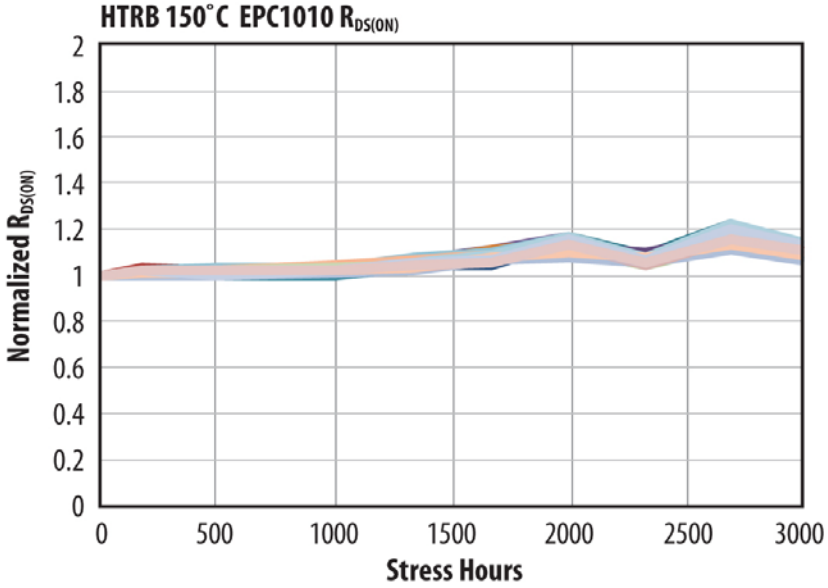

Fig. 2. EPC1010 devices were stressed with 200 V applied on the drain in the stress chamber at 150°C, source and gate shorted to ground. $R_{DS(ON)}$ was measured with 5 V on the gate at 25°C.

The stability under gate bias is illustrated in Fig. 3 where the normalized $R_{DS(ON)}$ is plotted against the stress time. Forty five EPC1001 devices were gate biased at 5 V at 125°C in the stress chamber with drain and source shorted to ground (HTGB). Some devices showed $R_{DS(ON)}$ shift of about 20% relative to the initial electrical values at the beginning of the test but stayed stable over the stress period of 3000 hours.

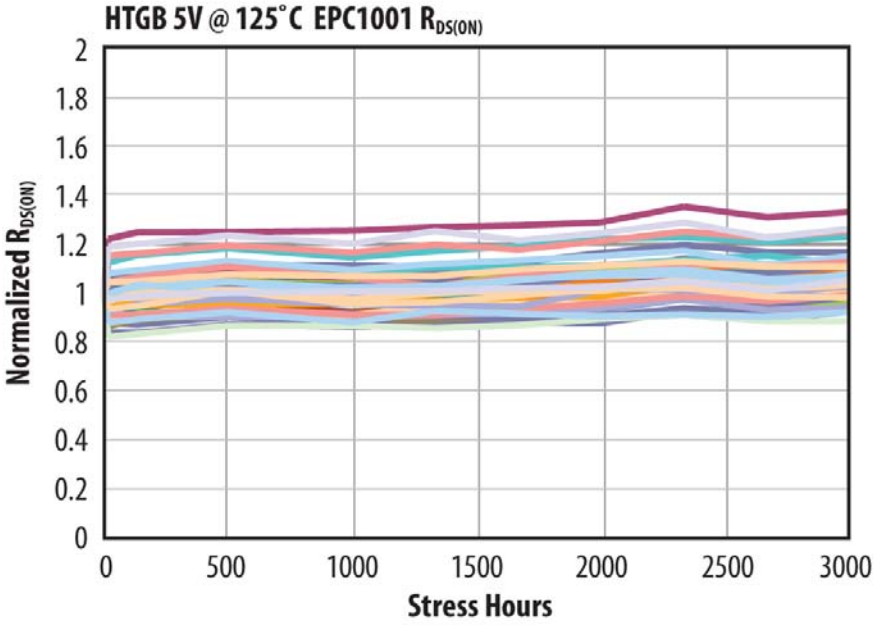

Fig. 3. EPC1001 devices were stressed with 5 V on the gate in the stress chamber at 125°C, drain and source shorted to ground. $R_{DS(ON)}$ was measured with 5 V on the gate at 25°C.

To test reliability under typical high-stress operating conditions, including the stability of $R_{DS(ON)}$, EPC built 48-V to 1-V power supply boards using a "buck converter" topology (see Fig. 4(b)). For the burn-in test, EPC1001 (100-V, 7 -mΩ) transistors were used for both the control transistor and rectifier switches. This kind of a test is particularly useful because, in a standard "buck" topology dc-dc converter operating at the high V_{IN}/V_{OUT} ratio of 48 V to 1 V, the control transistor is turned ON with a very low duty cycle (~2%). Conversely, the rectifier transistor is turned ON with a very high duty cycle (~98%). This test therefore stresses devices both at high drain-source voltage and high drain current under actual, fast-switching conditions.

The converter was operated at 48-V input, 1-V 10-A output, and at a switching frequency of 250 kHz. The circuit efficiency was measured at time-zero hour, 24, 48, 72, 168, 500, 1000, and 1200 hours. The normalized efficiency vs. burn-in hours (Fig. 4(a)) stayed virtually unchanged over the entire burn-in period.

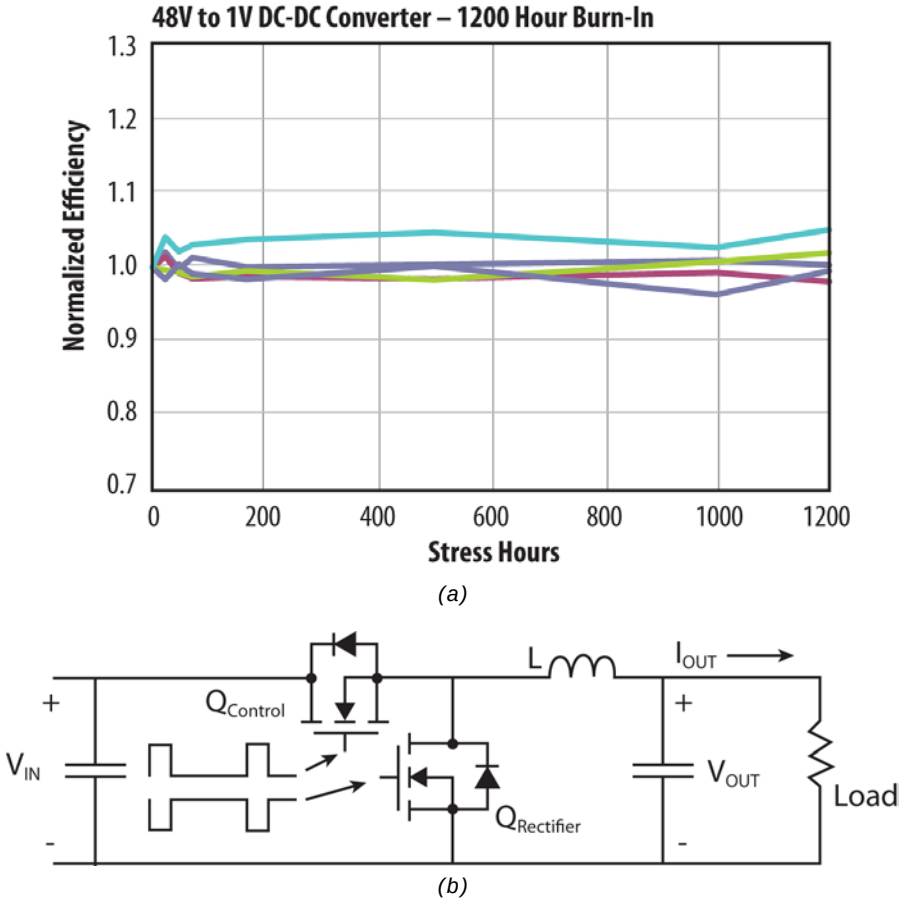

Fig. 4. Power supply life test using EPC1001 at 30°C and 10 A. The normalized converter efficiency is plotted over 1200 hours of operating life in (a), and the power supply test circuit is shown in (b).

The dynamic $R_{DS(ON)}$ phenomenon is not only accelerated by the electric field, but also when both channel current and a high electric field are present in the device [17]. The constant conversion efficiency demonstrated in the power-supply-operation life test indicated that there was no obvious $R_{DS(ON)}$ degradation in EPC eGaN transistors under high electric field in the OFF-state, or high channel

current in the ON-state, or during switching when both high electric field and high current exist simultaneously.

Recognizing the importance of minimizing the dynamic $R_{DS(ON)}$, and committed to continuous design and process improvement, EPC is working to further improve this characteristic.

Gate-Leakage Stability

Documented gate-leakage-degradation mechanisms include inverse-piezoelectric effect [18-19], carrier traps generated by high-energy electrons [20], and Schottky-contact degradation [21]. EPC's eGaN transistors do not use a Schottky gate and therefore are not vulnerable to this last mechanism.

GaN HEMTs are predicated on the piezoelectric properties of the material in conjunction with spontaneous polarization. The electric field generated between AlGaN and GaN as a result of strain caused by the lattice mismatch allows high electron-channel densities to form at the AlGaN/GaN interface. High electric fields at the gate edge under drain bias can increase the strain (inverse piezoelectric effect) and therefore affect device reliability. The inverse piezoelectric effect theory has been proposed to explain failure modes that could not be explained by hot-electron injection.

In this theory, high electric fields increase the strain in the AlGaN barrier layer. When a critical drain-gate voltage is reached, crystallographic defect formation occurs [18-19]. These crystallographic defects act as deep-level traps assisting electron tunneling, significantly increasing the gate-leakage current.

Another proposed mechanism is related to electron-initiated impact ionization near the gate edge in the off-state under high drain-gate bias. Electrons tunneling through the AlGaN barrier create hot holes with energies adequate to inject back into the AlGaN barrier. These holes may recombine with the trapped electrons releasing energy to produce bulk and transition-layer tunnel traps and interface states [20].

To verify the EPC eGaN transistors do not suffer from these degradation mechanisms, EPC subjected hundreds of parts to high drain-bias tests. Fig. 5 is an illustration of the gate-leakage performance of EPC1010 with 200 V applied on the drain, gate and source shorted to ground (HTRB). The gate leakage (IGSS) was measured with 5 V on the gate and with the drain and source shorted to ground. No gate leakage degradation was observed over the stress period of 3000 hours. As with EPC1010, no gate-leakage degradation was observed over the stress period for the 100-V (EPC1001) and 40-V (EPC1014) transistors in the HTRB tests with the max rated drain-source bias applied.

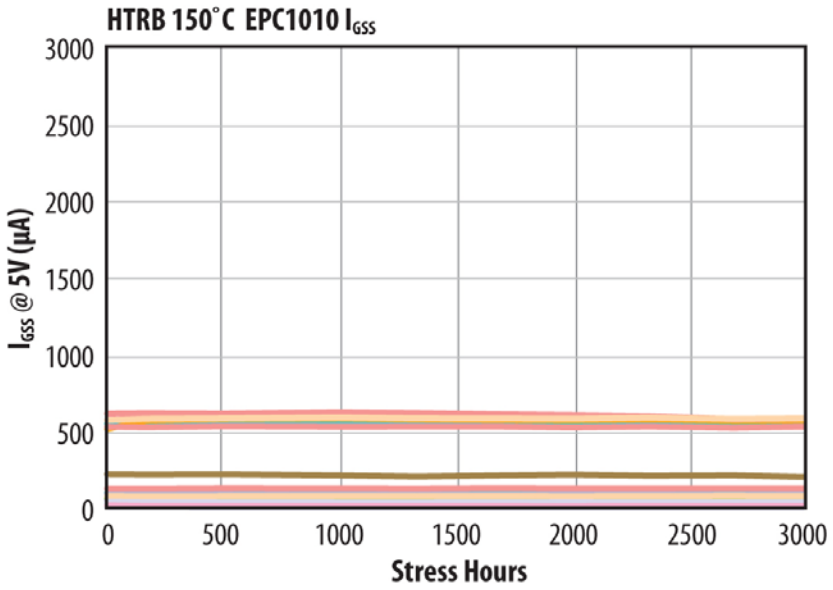

Fig. 5. EPC1010 devices were stressed with 200 V applied on the drain in the burn-in chamber at 150°C, source and gate shorted to ground. The gate leakage was measured with 5 V on the gate with drain and source shorted to ground at 25°C.

Stability Under Gate Stress

Device stability under gate stress was evaluated by subjecting parts to high-temperature gate bias (HTGB) at an elevated temperature of 125°C. Fig. 6 is an illustration of the gate leakage in the gate stress test where 5 V was applied on the gate in the stress chamber with drain and sources shorted to ground. As shown in Fig. 6, the leakage current stayed stable and no leakage degradation was observed. The same part number was also subjected to a higher stress with 5.4 V on the gate at 125°C. As with the gate stress test with 5 V on the gate, the gate leakage was stable over the entire stress period of 3000 hours.

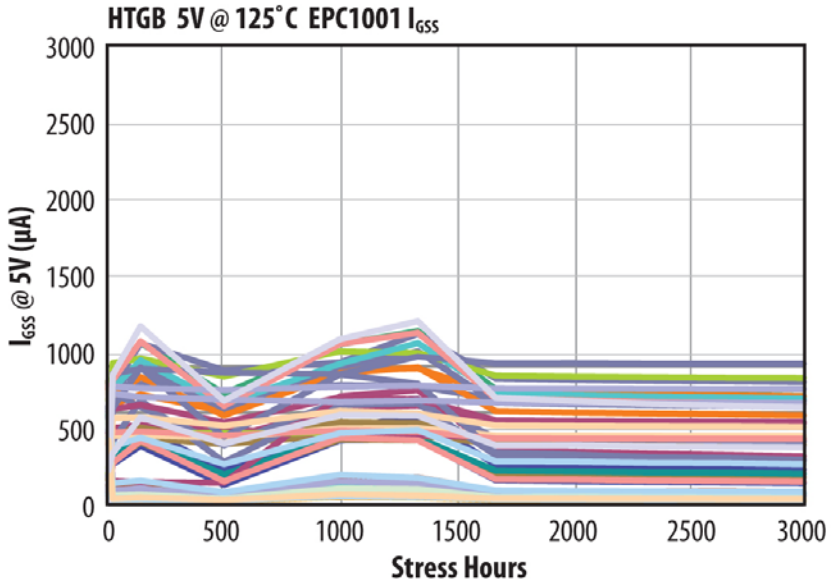

Fig. 6. EPC1001 devices were stressed with 5 V on the gate in the burn-in chamber at 125°C, drain and source shorted to ground. The gate leakage was measured with 5 V on the gate with drain and source shorted to ground at 25°C.

Users should avoid subjecting parts to more than 6 V in operation until further improvement on gate rating is made. Transistors subjected to a gate bias greater than 6 V showed stable gate leakage, but began to show an increase in the drain-to-source leakage.

EPC recognizes this weakness and is working to improve the gate's maximum voltage rating.

Humidity Sensitivity

EPC's eGaN transistors are lateral devices with all three terminals (gate, drain, and source) on the front side of the chip. The active device is fully encapsulated by passivation layers on the front side as shown in Fig. 7. This configuration allows EPC's eGaN transistors to be used as bare die without additional packaging. The advantages of eliminating plastic packages include elimination of parasitic resistance and inductance, added thermal resistance, internal package mechanical stress, space reduction and overall cost reduction.

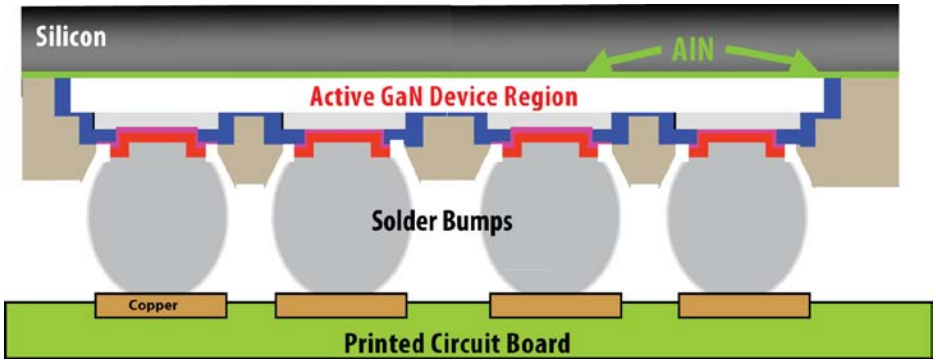

Fig. 7. eGaN transistors can be used as a "flip chip". When compared to plastic packages, this design reduces cost and requires less space.

Even though the devices are not in "normal" plastic packages, it has been demonstrated that they can perform reliably. Fifty EPC1010 transistors were subjected to a drain-source bias of 100 V at 85°C in a humidity chamber with 85% relative humidity (twenty five out of the fifty parts were underfilled). The

drain-source leakage over 1000 hours of stress (shown in Fig. 8) demonstrates the device stability. As with EPC1010, no drain-source-leakage degradation was observed over a 1000-hour stress period for the 40-V (EPC1014 and EPC1015) transistors.

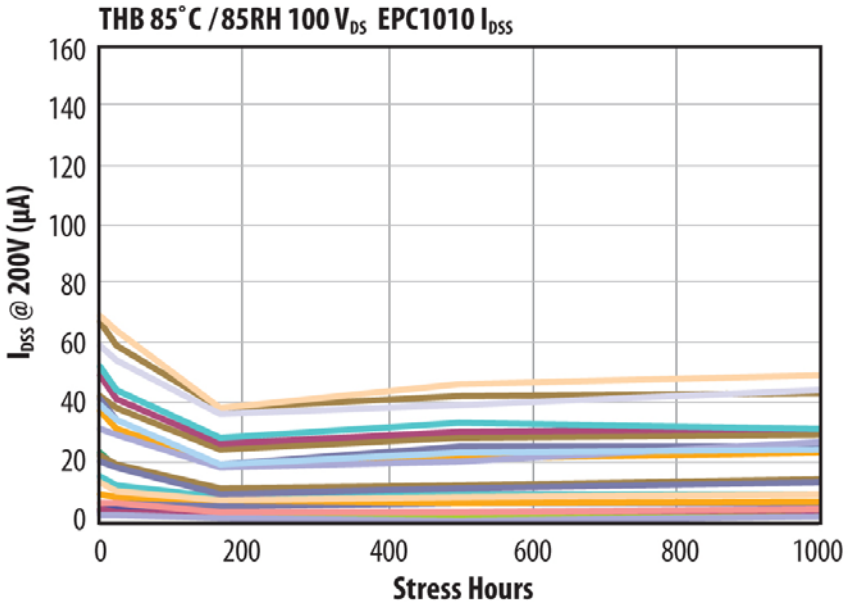

Fig. 8. EPC1010 devices were stressed with 100 V applied on the drain at 85°C in a humidity chamber of 85% relative humidity. The drain leakage was measured with 200 V on the drain with gate and source shorted to ground at 25°C.

Temperature Cycling

Fig. 7 shows how EPC's eGaN transistor can be used as a "flip chip" mounted onto a printed circuit board (PCB). To test the solder-joint stability under temperature cycling for this configuration, EPC put three device types (EPC1001, EPC1014, EPC1012) under temperature cycling from -40°C to 125°C, at a rate of two cycles per hour. The solder material for these part numbers was eutectic SnPb solder (63Sn-37Pb.) [23] (Lead-free parts will be introduced in late 2010.)

The normalized $R_{DS(ON)}$ was plotted in Fig. 9 to show the device stability under this stress condition. The on-state resistance, as well as all other device parameters, remained stable over the stress period of 1000 cycles.

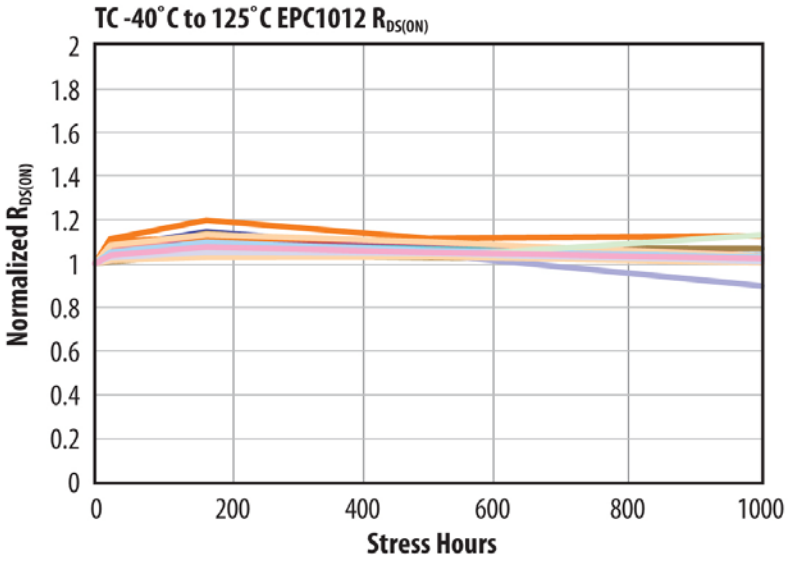

Fig. 9. EPC1012 devices were temperature cycled between -40°C and 125°C at a rate of two cycles per hour. $R_{DS(ON)}$ was measured with 5 V on the gate at 25°C.

Device ESD Capability

Electrostatic discharge (ESD) tests were conducted on EPC1014 and EPC1015. EPC1014 is a smaller size device (1.7 mm x 1.1 mm) and EPC1015 is a larger device (4.1 mm x 1.6 mm) representing the spectrum of EPC's product offerings. Both human body model (HBM) and machine model (MM) tests were conducted on these two part numbers. JESD22-A114F was followed for the HBM, and EIA/JESE22-A115-A was followed for the MM. The ESD results are summarized in Table 2.

Table 2. ESD results.

Pin-Pin(+/-)	EPC1015 HBM	EPC1014 HBM	EPC1015 MM	EPC1014 MM
G-S (+)	CLASS 1A	CLASS 1A	CLASS A	CLASS A
G-S (-)	CLASS 1A	CLASS 1A	CLASS A	CLASS A
G-D (+)	CLASS 1B	CLASS 1A	CLASS B	CLASS A
G-D (-)	CLASS 1B	CLASS 1A	CLASS B	CLASS A
S-D (+)	> CLASS 3A	> CLASS 3A	CLASS C	CLASS C
S-D (-)	> CLASS 3A	> CLASS 3A	CLASS C	CLASS C

The source-drain path has low sensitivity to ESD. On HBM, both EPC1014 and EPC1015 exceeded ±4000 V drain-source without fail, making them Class 3A (or higher) capable. On MM, both EPC1014 and EPC1015 passed ±400 V drain-source, making them Class C capable.

Due to the extremely low input capacitance of EPC's transistors, the gates are ESD sensitive. Both EPC1014 and EPC1015 were Class 1A rated gate-source on HBM and Class A rated gate-source on MM. EPC1015 passed ±500 V gate-drain, making it Class 1B capable on HBM, and passed ±200 V gate-drain, making it Class B capable on MM. EPC1014 was Class 1A-rated gate-drain on HBM and Class A-rated gate-drain on MM.

Conclusions

EPC's eGaN transistors bring designers significant performance and size advantages over silicon power MOSFETs. These advantages can be used to improve system efficiency, reduce system cost, reduce size, or a combination of all three. Because EPC's products were designed as power MOSFET replacements,

designers can use their existing building blocks, skills and knowledge with only minor changes. Reliability testing has also demonstrated that the technology is now ready for general commercial use.

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For more on GaN power transistors and their applications, see the How2Power Design Guide, select the "Popular Topics" category, and then search the "Silicon Carbide and Gallium Nitride" subcategory.