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High Step-Down Ratio Buck Converters With eGaN Devices

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The intermediate bus architecture (IBA) is currently the most popular power system architecture in computing and telecommunications equipment. It typically consists of a +48 V system power distribution bus that feeds on-board bus converters, which in turn supply power to nonisolated, dc-dc converters. These nonisolated converters generate the low supply voltages required to power the various logic circuits. Because of their proximity to the circuits they power, these converters are commonly referred to as point-of-load converters (POLs).

The IBA bus architecture did not spring up overnight, but rather evolved as a refinement of the 48 V distributed power architecture (DPA) that was previously the architecture of choice in telecom and computing applications. In that architecture, a series of isolated 48 V input dc-dc converters generated all of the board-level supply voltages. (For those interested in the developments that led to the IBA, see "Evolution Of The Intermediate Bus Architecture (IBA)" at the end of this article.)

Although the IBA is widely used, it is coming under scrutiny. Some companies using a +48 V system power distribution bus with on-board bus converters and POLs are wondering if they can simplify their systems. For them, a single "POL" that converts the +48 V system bus directly to the load voltages is a very interesting idea. Until now, the technical limitations of the current silicon MOSFET technology and cost concerns have made it impractical to design such a POL and produce it commercially. However, recently introduced gallium-nitride (GaN) power devices have overcome these hurdles, making it feasible to build POLs with the high stepdown ratios needed to generate 1 V or less directly from a 48 V bus.

On-time Limitations Of Silicon

The biggest problem with implementing a buck converter that converts +48 V to 1.8 V, 1.2 V, or 0.8 V is the capability of today's silicon-based MOSFETs. This high stepdown ratio requires the buck converter to operate with very small duty cycles (for example, 2.5% to convert 48 V to 1.2 V).

Today's 60 V to 100 V rated MOSFETs have a minimum reliable on-time in the range of 100 ns to 200 ns. This would mean a maximum switching frequency of 125 kHz to 250 kHz. These are arguably reasonable switching frequencies with manageable switching losses in the control MOSFET. However, control is another issue. If the converter is operating just at the edge of the minimum on-time to maintain the nominal output voltage, the controller cannot reduce the duty cycle to maintain regulation during load transients. It is possible to implement non-linear pulse skipping control methods during this kind of operation, but those can have undesirable side effects.

To maintain good controllability, it is reasonable to keep the normal minimum on-time to at least five times greater than the minimum on-time of the switching devices. This brings the switching frequency of a 48 V to 1.2 V converter using silicon MOSFETs down to 25 kHz to 50 kHz. At these frequencies, much of the benefit is lost due to increased size of the output filter inductor and capacitors.

One possible way around the minimum on-time constraint would be to use a tapped inductor. However this introduces a fair amount of additional cost as well as loss in the leakage inductance between the two windings. Although there has been a fair amount of research in this area, this approach is not common in practice.

Systems using 12 V output, ac-dc front-end power supplies are also having issues. In some systems, such as high-density blade servers, the system power is measured in kilowatts, and the 12 V current in hundreds of amperes. This costs a lot in terms of large copper bus bars and expensive, high-current connectors.

OEMs wish they could use a +48 V bus to reduce distribution currents, but the cost in money and efficiency in going to a two-stage (bus converter plus POL converters) is too high.

To make matters worse, these system OEMs are having issues with the stepdown ratio from 12 V to load voltages less than 1 V. The same minimum on-time issues that give trouble converting 48 V to 1.2 V are coming into play in 12-V systems. This is driven in part by the very high switching frequency (up to 1 MHz) used in the POLs in these types of systems.

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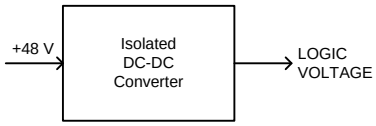
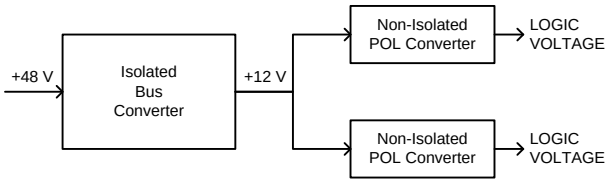
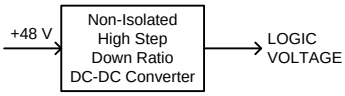
One approach being considered to solve this problem is to reduce the system distribution voltage, perhaps to 6 V. This solves the stepdown ratio issue, but doubles the already huge system distribution bus current.

Table 1 shows a summary and comparison of the efficiency of distributed power systems, intermediate bus architecture systems, and a system with single-stage, high-stepdown-ratio buck converters.

Table 1. Power systems architecture and metrics.

Distributed Power System Efficiency: 80% to 87%	
Intermediate Bus Power System Efficiency: 78% to 88% overall	
Single High-Ratio Stepdown Converter System Efficiency: 80% to 86%	

Enter The eGaN Device

But what if we had a device that could switch reliably and with low loss in 10 ns? All of the limitations and problems described above created by the minimum on-time of today's silicon MOSFETs would vanish. Small and efficient high-ratio single-stage stepdown converters could now be built. No longer would converting +48 V to load voltages like 1.2 V, or converting +12 V to 0.7 V be a problem.

Devices with this fast switching time are in fact available today from Efficient Power Conversion (EPC). EPC's eGaN enhancement-mode gallium-nitride (GaN) transistors have been commercially available for over a year. Devices available today range from a 40 V transistor with a 4 mΩ on-resistance and 33 A rated drain current to a 200 V transistor with a 25 mΩ on-resistance and 12 A rated drain current. These devices also have much lower capacitance than silicon MOSFETs and body diodes with no reverse-recovery charge (Q_{RR} = 0 nC).

Devices like this open the door to two very interesting possibilities for almost any kind of switching power converter:

- More-efficient operation at the same frequency
- Higher frequency operation with the same efficiency

Experimental Set-up

To explore these possibilities, two high-stepdown-ratio buck converters were built. One converter used state-of-the-art silicon devices rated at 60 V. The other converter used eGaN devices. These converters used the same output inductor and capacitors.

Each converter was operated at 200 kHz and 500 kHz. The input voltage was set to 48 V. The converters were run open loop and the duty cycle adjusted to maintain an output voltage of 1.2 V. Efficiency data was taken as the load varied from 0 A to 10 A (200 kHz) and 0 A to 8 A (500 kHz).

Fig. 1 shows the schematic of the test circuit.

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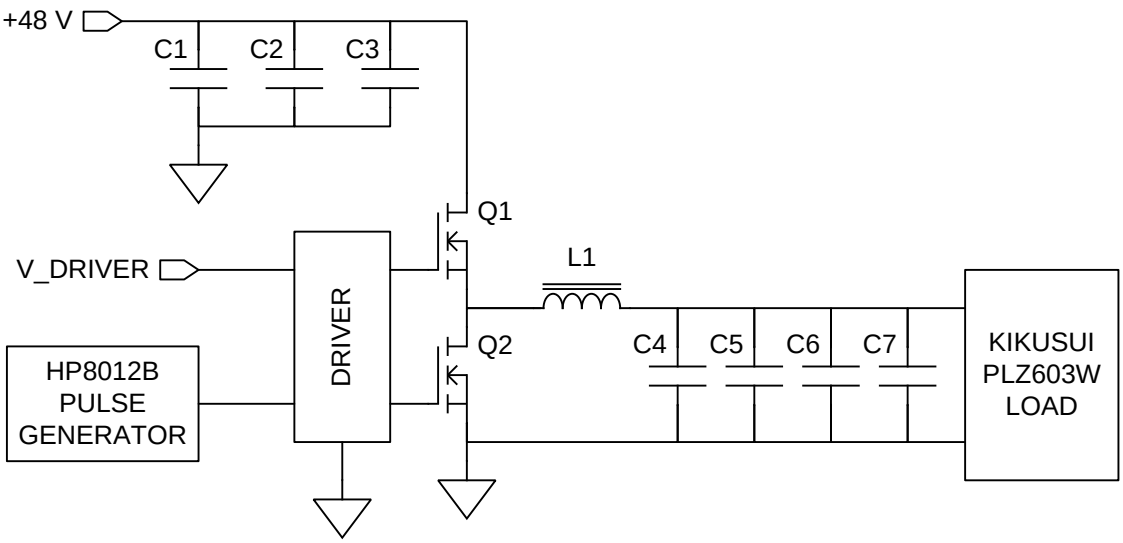

Fig. 1. Experimental circuit.

The experimental circuit was constructed using a two-phase buck converter demo board. This construction, using essentially the same current path and filter components, gives the best possible assurance that any difference is performance is only because of the differences between the silicon MOSFETs and the eGaN devices.

Fig. 2. shows a top view of the circuit. The silicon MOSFETs are mounted directly to the two-phase buck demo board. The eGaN devices are mounted onto a separate half H-bridge demo board (EPC part number 9002).

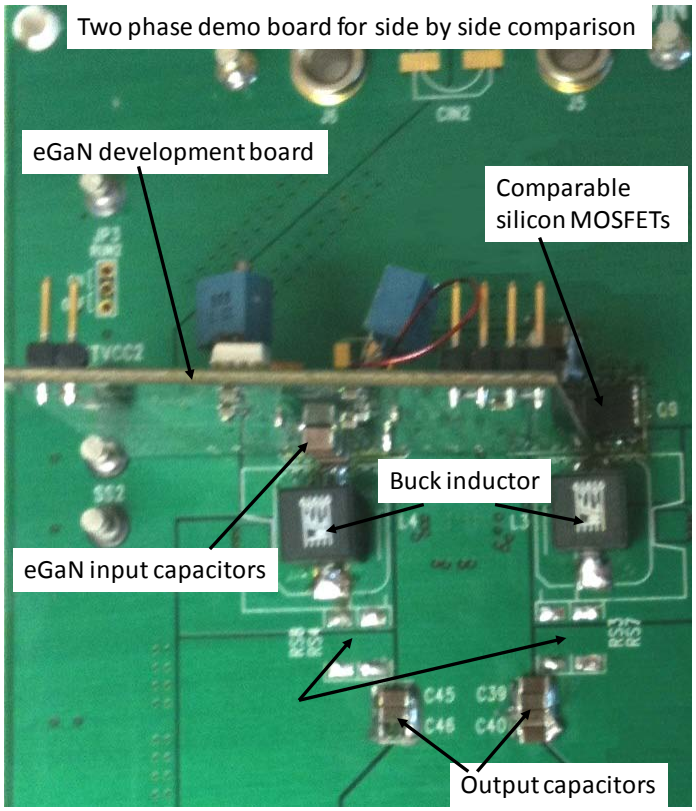

Fig. 2. Top view of the experimental circuit.

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Fig. 3. shows how the EPC demo board is attached to the two-phase buck demo board. This photo also shows the two potentiometers used to adjust the dead-time of the eGaN devices. The input bypass capacitors for the silicon MOSFETs are visible on the two-phase board. The input bypass capacitors for the eGaN devices are on the EPC demo board.

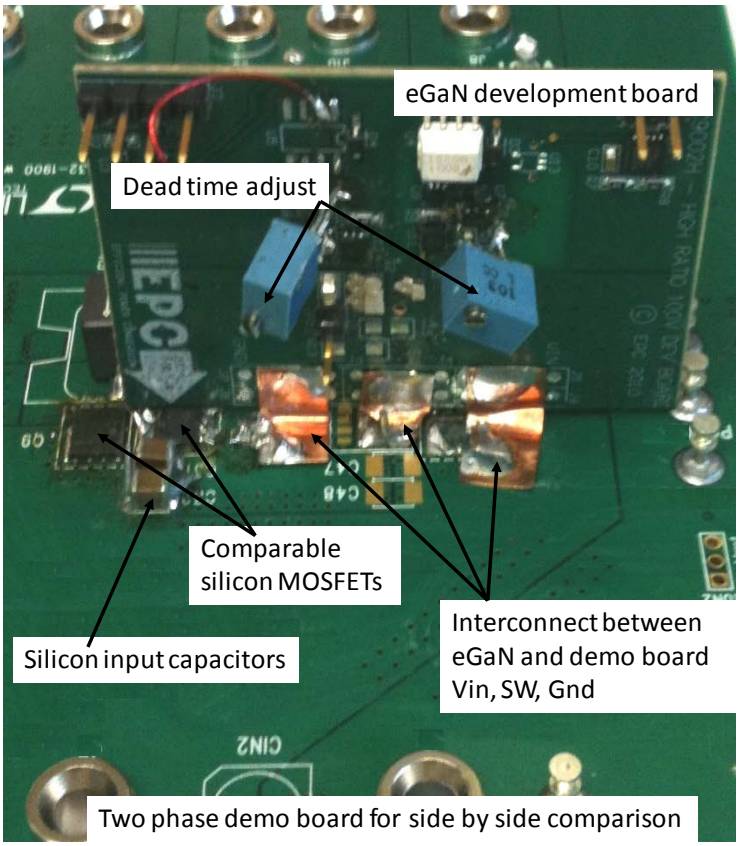

Fig. 3. Attachment of the eGaN demo board.

Fig. 4. shows the back side of the two-phase board. In this photo, it can be seen that the board is using the same drivers with the same dead-time adjustment potentiometers used for the silicon MOSFETs.

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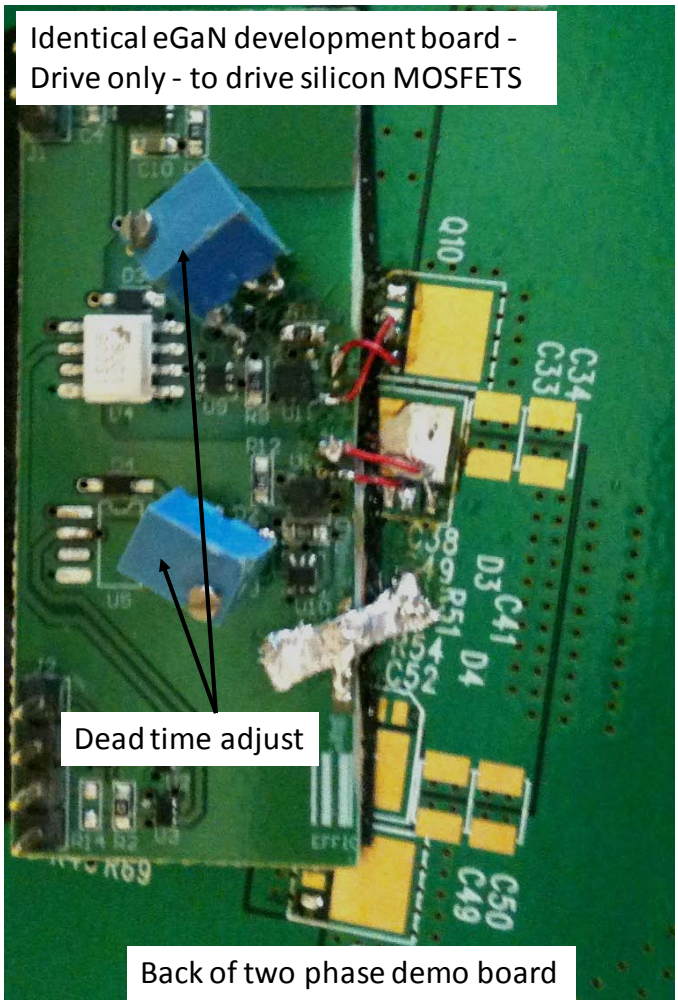

Fig. 4. Drivers for the silicon MOSFETs.

The silicon transistors were selected because they are representative of the best generally available in the market today. Another criterion was to match as closely as possible the on resistance and current rating of the silicon and eGaN devices. Table 2 gives a summary of the key characteristics of the transistors used in this experiment.

Table 2. Characteristics of the silicon and eGaN transistors.

	Part Number	V_{DS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (mΩ)	Q_G (nC)	Figure Of Merit (mΩ-nC)	Package Type	PCB Area (mm^2)
Silicon control FET	Si7850	60	6.2	25	18	450	PowerPAK SO-8	31.7
Silicon sync FET	RJK0652	60	35	6.5	29	189	LFPAK	29.8
eGaN control transistor	EPC1007	100	6	24	2.7	65	Flip Chip	1.8
eGaN sync transistor	EPC1001	100	25	5.6	10.5	59	Flip Chip	6.7

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A few points jump right out when comparing the transistors. First, the gate charge of the silicon devices is many times that of the GaN devices. The silicon control FET requires 18 nC to switch; the eGaN device requires only 2.7 nC. This 6:1 ratio means the eGaN devices will have a substantially lower switching loss. The synchronous rectifier transistors also have a large difference in total gate charge.

The next thing to notice is that, due to the much lower gate capacitance, the standard figure-of-merit (FOM) of the eGaN devices is three to seven times better than that of the silicon FETs.

The last significant difference is the PCB area required by the devices. The area shown in the table is simply the product of the outside dimensions of the package. The silicon devices require 61.5 mm² of board space. The eGaN devices only require 8.5 mm². The silicon devices require seven times the PCB area of the eGaN devices. In a system with many voltage rails, the savings in board space offered by the eGaN devices will be significant.

Fig. 5. is a photo of the EPC development board. The silicon MOSFETs have been placed on the board to show their relative size to the EGaN devices. A 1206 size capacitor is identified to set the scale. Note that the eGaN control transistor is smaller than the 1206 capacitor and the eGaN sync transistor is not much larger.

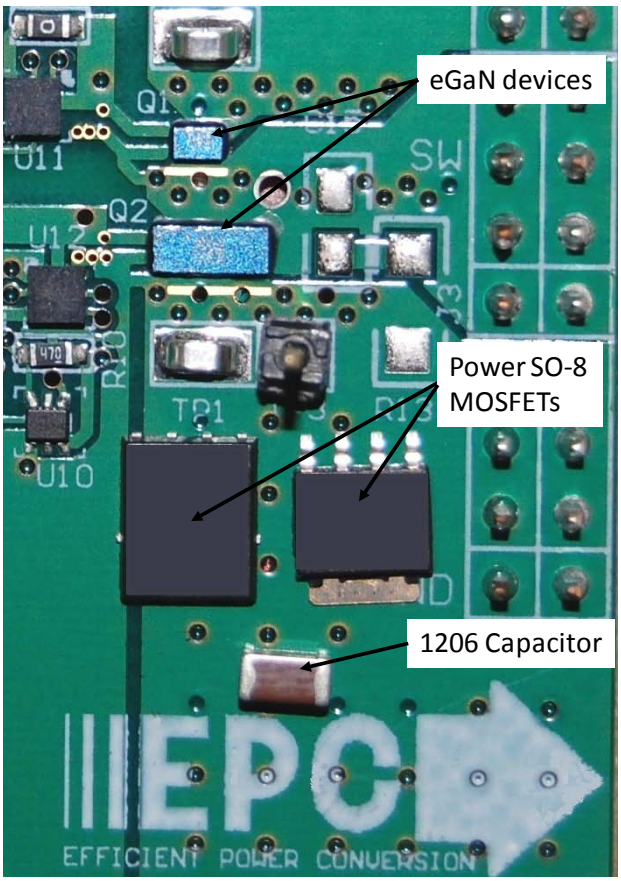

Fig. 5. Relative sizes of silicon MOSFETs and eGaN devices.

The inductor and capacitors are detailed in Table 3.

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Table 3. Input And output filter components.

Component	Reference designator	Part number	Characteristics
Input filter capacitor (200 kHz & 500 kHz)	C1, C2, C3	TDK C3225X7R2A225K	2.2 µF, 100 V, X7R, 1210, ceramic
Output filter inductor (200 kHz)	L1	Würth Electronic 7443320220	2.2 µH, 18.0 A, 3.05 mΩ, 12.1 mm x 11.4 mm
Output filter capacitors (200 kHz)	C4, C5, C6, C7	TDK C3216X5R0J476M	47 µF, 6.3 V, X5R, 1206, ceramic
Output filter inductor (500 kHz)	L1	Würth Electronic 7443340100	1.0 µH, 17.0 A, 2.95 mΩ, 8.4 mm x 7.9 mm
Output filter capacitors (500 kHz)	C4, C5[1]	TDK C3216X5R0J476M	47 µF, 6.3 V, X5R, 1206, ceramic

Note 1: For the 500 kHz converter only two output capacitors were used.

Table 3 also shows the board-space advantage achieved by increasing the switching frequency from 200 kHz to 500 kHz.

At 200 kHz, the inductor requires at least 0.21 in² (138 mm²), and the four output capacitors require at least 0.029 in² (18.6 mm²). The total board area of the 200 kHz output filter is 0.24 in² (157 mm²).

At 500 kHz, the inductor requires at least 0.10 in² (66 mm²), and the single-output capacitor requires only 0.007 in² (4.6 mm²). The total board area for the 500 kHz output filter is about 0.1 in² (71 mm²)—more than a factor of two smaller than the 200 kHz filter.

The higher-frequency design saves another 0.14 in² (90 mm²) over the size reduction offered by just the physical dimensions of the GaN devices.

Experimental Results: 200 kHz

Fig. 6 shows the measured efficiency when the two converters were operated at 200 kHz. A quick glance reveals that the converter with eGaN devices was about 2% more efficient over most of the load range.

Looking at the eGaN efficiency curve, we see that the silicon FETs actually have a slightly higher efficiency than the eGaN devices at light load. This is because the dead-time for the eGaN devices was optimized for maximum efficiency at higher output current. This resulted in a loss of zero-voltage switching at light loads. When the dead-time at light loads was adjusted for minimum loss, as an adaptive driver would do, the efficiency improved by as much as 5% at 1 A output current and the eGaN devices are more efficient over the entire load range.

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Fig. 6. Efficiency at a 200 kHz switching frequency.

Another way to look at the data is to look at the losses as a function of load, as shown in Fig. 7. We see that the silicon MOSFETs dissipate about a half watt more than the eGaN devices over most of the load range. In systems with many logic voltages, the half-watt savings of the eGaN devices will add up to a substantial power reduction at the system level.

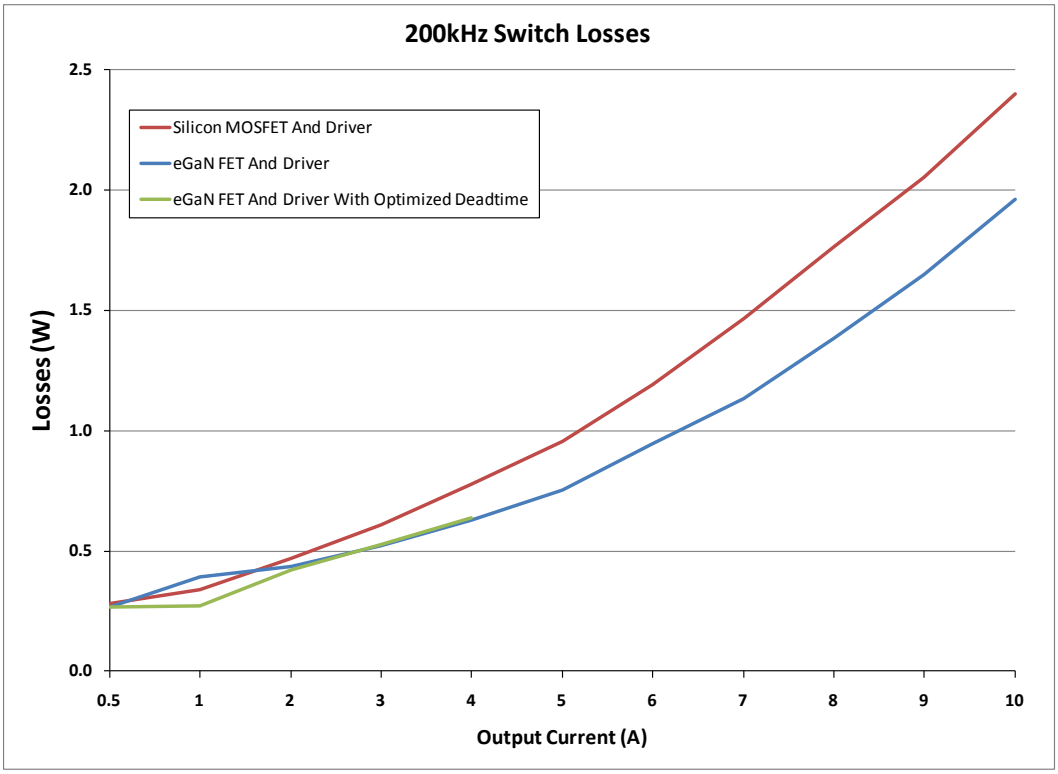

Fig. 7. Losses at 200-kHz switching.

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The losses shown here and below were calculated from the experimental data by:

- Calculating the input power $P_{IN} = V_{IN} \times I_{IN}$
- Calculating the output power $P_{OUT} = V_{OUT} \times I_{OUT}$
- Calculating the driver power: $P_{DRIVER} = V_{DRIVER} \times I_{DRIVER}$
- Estimating the losses in the inductor: $P_L = DCR \times I_{OUT}^2 + \text{Estimated Core Loss}$
- Calculating the overall efficiency: Efficiency $= P_{OUT}/(P_{IN} + P_{DRIVER})$
- Calculating the transistor loss: $P_{TRANSISTOR} = P_{IN} - (P_{OUT} + P_{INDUCTOR})$.

Note that the 48 V input and driver input power came from two different power supplies.

Dead-time Considerations

The data clearly shows the importance of an optimized dead-time for a given output current. Fig. 8. shows the switch-node voltage and output current (purple trace, inverted) of the eGaN converter while operating at no load. The dead-time is set long so that there is zero-voltage-switching on the transition.

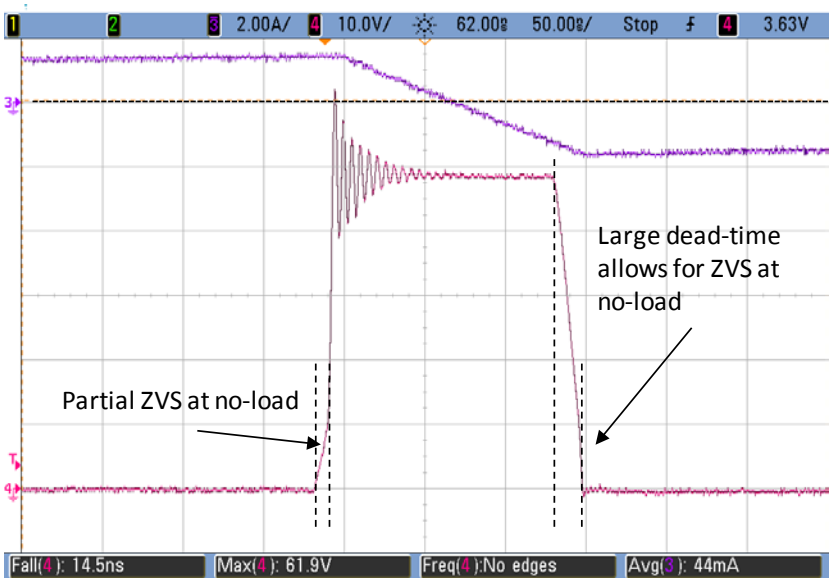

Fig. 2. No-load dead-time.

However, as shown in Fig. 9, a long dead-time causes a significant amount of conduction of the body diode at high output current.

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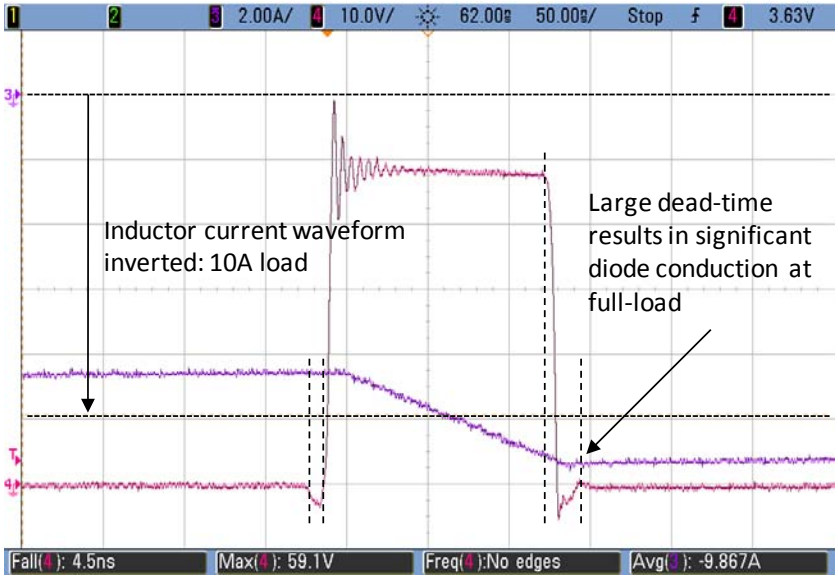

Fig. 9. Long dead-time at 10-A output current.

However, an optimized dead-time at high output current, shown in Fig. 10, results in minimal body-diode conduction time and maximizes efficiency. Take note of the rise and fall times of the switch-node voltage—less than 5 ns! This clearly shows the superior switching speed offered by the eGaN devices.

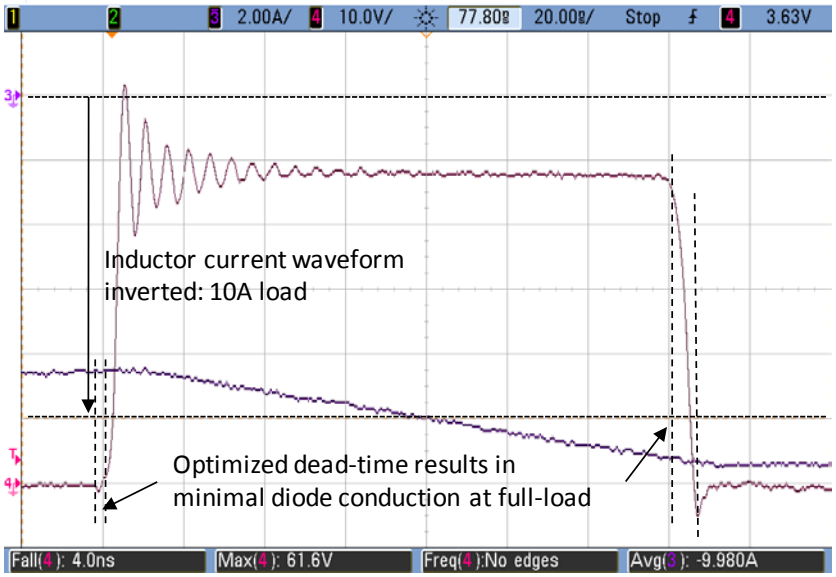

Fig. 10. Optimized dead-time at 10-A output current.

This experimental work clearly shows the need for an optimizing, adaptive driver for the eGaN devices.

Experimental Results: 500 kHz

Fig. 11. shows the measured efficiency when the two converters were operated at 500 kHz. A quick glance shows the eGaN device converters demonstrating their advantage at higher frequency—the eGaN converter is about 4% more efficient over most of the load range.

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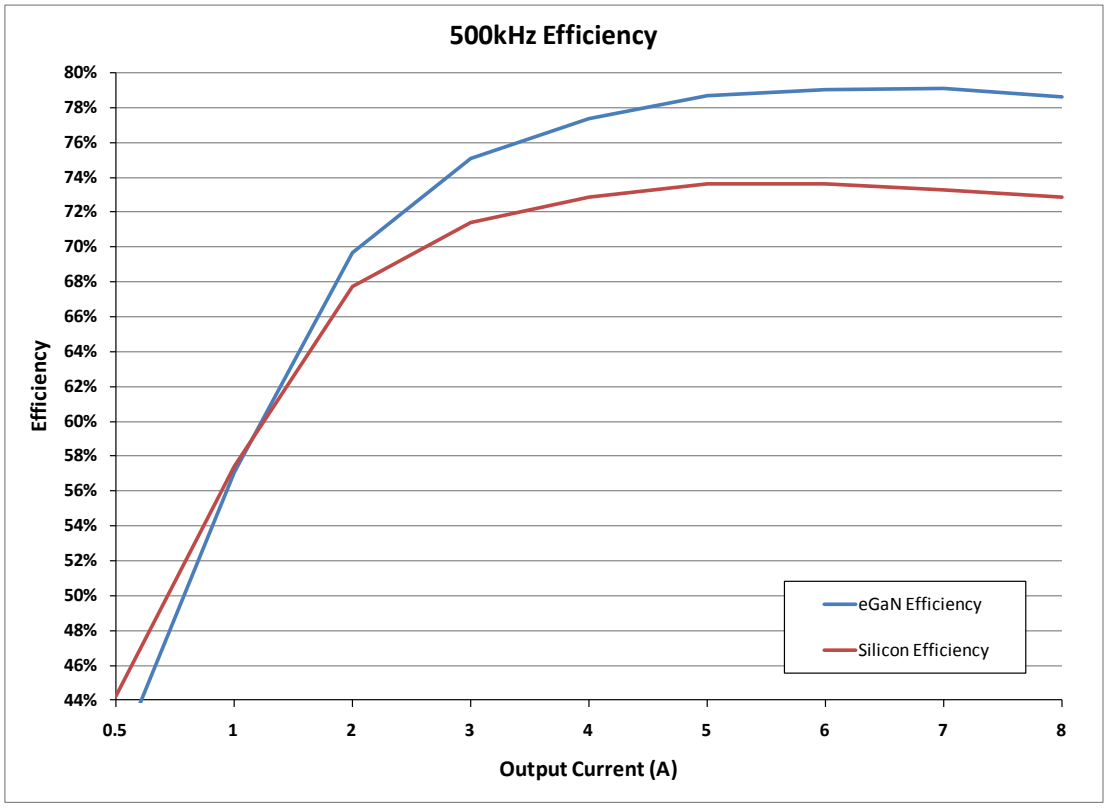

Fig. 11. Efficiency with 500-kHz switching

Looking at the losses (Fig. 12) shows that the silicon devices are dissipating about 1 W more than the eGaN devices at 8 A output.

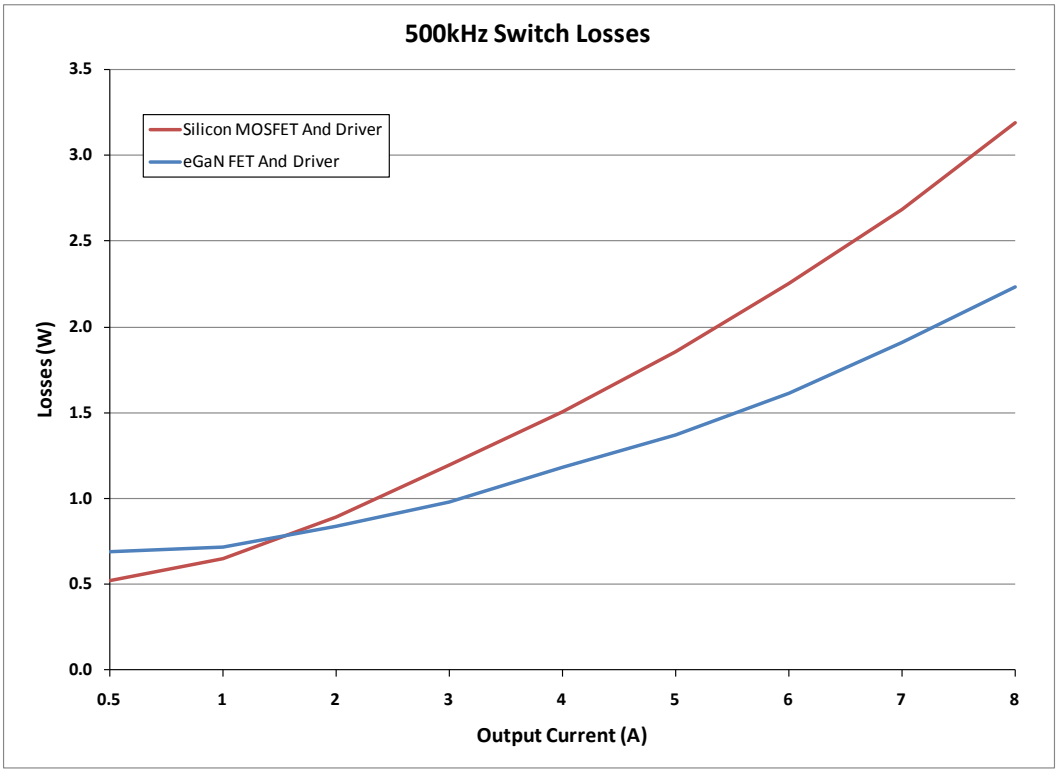

Fig. 12. Losses when switching at 500 kHz.

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It's also useful to look at the switch-node waveforms. Fig. 13 shows the switch-node voltage and output current (inverted) when switching at 500 kHz. Note that the on-time is about 100 ns. Even at this very short on-time, the waveform has nearly vertical edges and flat tops. We see that a controller could easily reduce the on-time by a factor of five in order to maintain control and good transient response during a sudden load reduction.

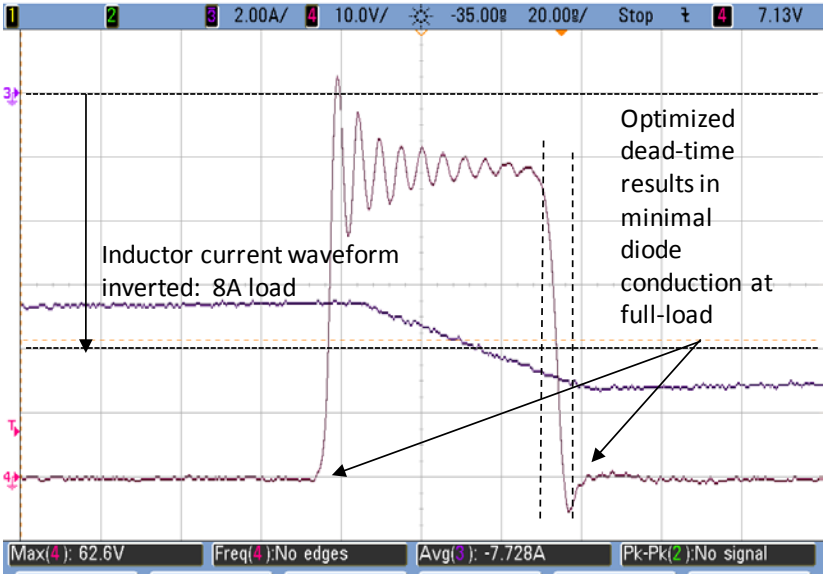

Fig. 13. Switch-node voltage with 500-kHz switching and optimized dead-time.

If the goal is fastest possible switching, Fig. 14 shows that with a hard-switched transition the rise time is about 2.5 ns. This kind of switching speed is simply unheard of with silicon power MOSFETs.

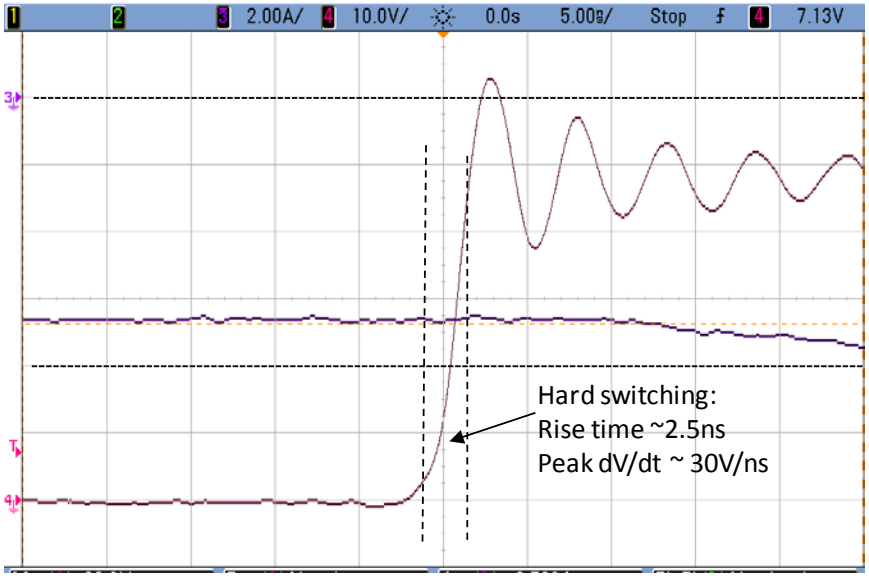

Fig. 14. Hard-switching transition time.

If the goal is to minimize the losses, Fig. 15 shows that soft-switching transitions of less than 5 ns are possible. The caveat is that the soft-switching transition time is load dependent.

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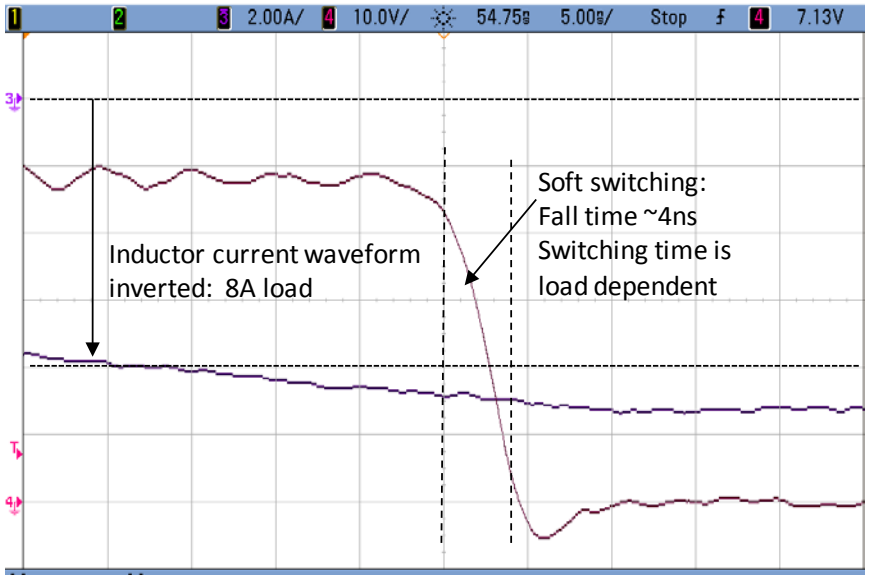

Fig. 15. Soft-switching transition.

While these fast transitions will allow us to operate at very high frequencies with good efficiency and small size, they will require care in the physical design. With voltages and currents switching in just a few nanoseconds, parasitic capacitances and inductances that are negligible today will not be in the future.

This is the same issue we faced as silicon MOSFETs started being widely adopted in the early 1980s. At that time, it was not anticipated that the source-lead bond wire could cause so many problems. We learned and we adapted. Power device designers did a better job with packaging, and circuit designers learned how to make Kelvin connections to the gate and source. Just as we talked about using "RF techniques" back then, we will once again be talking about "RF techniques" for the PCB layout, transformer construction, and heat sinking. These will all be manageable challenges and we can be sure that we will be seeing articles and papers in the coming months and years exploring this new frontier.

Conclusion

These experiments show that single-stage buck converters can be used to step down from 48 V to logic-level voltages with good efficiency. The single-stage converters offer significant savings in board space and parts count. OEMs using +48 V system power, either with fully regulated isolated dc-dc converters, or with an intermediate bus voltage, could benefit from these smaller single-stage converters.

And the future holds even greater promise. We have shown that an optimizing, adaptive controller can offer improved performance over wide ranges of load current. There are no technical barriers to creating an integrated driver for the eGaN devices with today's IC technology.

It is also important to note that the silicon MOSFETs used in this experiment are state-of-the-art devices that are the result of 30 years of continuous improvement. The characteristics of the silicon MOSFET are very near the theoretical limits of silicon. We cannot expect any additional order of magnitude improvements. The eGaN devices used in this experiment, however, are first-generation devices. Even though we are very early in the development, they are already outperforming the best available silicon devices. The history of semiconductors tells us we can expect huge improvements in the performance of GaN tranistors in the coming months and years.

These devices offer the power electronics designer the opportunity to improve the state-of-the-art in a leap that hasn't been seen since the advent of the silicon power MOSFET more than 30 years ago. There will be challenges and bumps in the road as the device makers refine the devices and the IC makers develop controllers and drivers that match the capability of the GaN device, but that should not deter power electronics designers from starting to ask themselves the question, "what can I do now that I couldn't do before?" The answers to that question are sure to be exciting and rewarding.

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Appendix: Evolution Of The Intermediate Bus Architecture (IBA)

In the beginning of the telephone age, system operators quickly realized they needed battery backup to offer very high availability to customers. The predominant battery technology was flooded-cell lead acid, which has high energy density, relatively low cost, and long life (if carefully maintained). The telephone system settled on using 24 cells in series. Each cell has a float voltage of about 2.17 V yielding a flow voltage about 52 V. However, when a load is put onto these cells, the voltage drops to about 2 V per cell, or 48 V for the entire battery string. To limit corrosion to wiring outside of the central office, a -48 system was, and is, used.

The -48 V power systems worked well for the telephone companies even into the transistor age. However, in the 1970s, when they started designing electronic switches with TTL logic and analog ICs they needed a reliable source of +5 V as well as related voltages such as ±12 V and ±15 V. This drove the development of 48 V to low voltage dc-dc converters. At first, these converters were either discrete designs on the same circuit board as the telephone circuitry, or entire pluggable "circuit packs." The telephone companies quickly worked toward higher density and higher reliability board-mounted dc-dc converter modules.

While telephone companies led the way, by the mid-1980s there were several companies offering board mounted 48 V to 5 V, 12 V, and 15 V dc-dc converter modules in various form factors.

The race was on. Throughout the 1990s the debate was, "distributed or central" power systems. Board-mounted dc-dc converters were widely used in computer, telephone, and networking equipment. Universally, these converters used an isolated topology, usually a variant of the forward converter, the active clamp forward converter, or, sometimes, the flyback converter.

By the late 1990s a storm was brewing. Logic voltages were dropping and the number of different voltages needed in a system was growing rapidly. It was becoming physically and economically difficult to power systems using "brick" converters, even as the size of the converters was shrinking.

By that time the use of 12 V input nonisolated dc-dc converters ("VRMs") to power the increasingly power-hungry microprocessors in desktop computers and servers was established. The huge volume of parts used in this application drove the cost down so much that 12 V input nonisolated dc-dc converters became relatively inexpensive. These nonisolated 12 V input converters were then combined with either 12 V output ac-dc power supplies or 48 V to 12 V output dc-dc converters, forming what is called the intermediate bus architecture ("IBA").

Because the IBA offered lower cost and equal or better overall efficiency, the IBA rapidly displaced the 48 V bus distributed power systems in most applications. Although discrete on-board point-of-load (POL) converter designs (a.k.a. embedded or down-on-the-board designs) have now replaced the fully assembled POL modules of the early 2000s, the IBA is still the most popular power system architecture in computing and telecommunications equipment.

Also by the late 1990s, the computing and network equipment companies realized that their equipment did not need the wide range (36 Vdc to 75 Vdc) input voltage of dc-dc converters used in battery-backed telephone power systems. They generally settled on a well regulated +48 V distribution voltage. This narrow input range enabled converters that were a few percent more efficient than the wide-input range converters.

The next step was to realize that, with a well regulated bus, the dc-dc converter converting the +48 V to the intermediate bus voltage did not have to be regulated. Several companies developed "dc-dc transformers", or "bus converters" that had a fixed-ratio stepdown. The most common converter has a 4:1 ratio and converts 48 V to 12 V. Bus converters with stepdown ratios of 5:1 (9.6 V output) were also introduced.

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About The Authors

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For more on GaN power transistors and their applications, see the How2Power Design Guide, select the “Popular Topics” category, and then search the “Silicon Carbide and Gallium Nitride” subcategory.

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