The Over-Power Phenomenon in DCM/CCM-Operated Flyback Converters (Part 3): Quasi Square-Wave Resonant Mode

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In parts 1 and 2 of this article series, we derived the equations that explain why flyback converters can deliver greater power under high input-line conditions versus low-line conditions. These previous articles focused on flyback converters operating at a fixed switching frequency and in continuous-conduction mode (CCM) or discontinuous-conduction mode (DCM). But despite its simplicity of design, the CCM flyback converter does not lend itself very well to synchronous rectification (SR) on the secondary side. Therefore, to achieve the higher efficiency associated with synchronous rectification, many designers are considering a change from CCM to a quasi square-wave resonant (QR) mode of operation where secondary-side shoot-through currents are eliminated.

QR converters operate at a frequency where the primary inductor current always remains at the border between continuous and discontinuous modes. This is known as boundary- or borderline-conduction mode, which is commonly referred to as BCM operation, and is also known as critical-conduction mode or CrM for short. These converters operate in a kind of self-relaxing mode that induces wide frequency variation as the load and line conditions change. A consequence of BCM is that the power delivered at high line under a fault condition, is larger than the one obtained at low line. Over-power protection (OPP) is thus mandatory for QR-mode flyback designs to avoid the need for overdesign of components or risk component destruction.

The Flyback Converter Operated In BCM

The waveforms associated with the BCM-operated flyback converter (Fig.1) reveal the absence of a valley current on the primary side: all of the stored energy is transferred at turn-off to the secondary side and the transformer magnetic core is fully reset on a cycle-by-cycle basis. The converter actually works in a free-running discontinuous mode where a dead-time DT is purposely inserted prior to the MOSFET turn-on event. This dead-time is adjusted to ensure valley-switching operation (i.e. a turn-on when the drain-source voltage is at its minimum value), naturally minimizing capacitive losses in the power MOSFET.

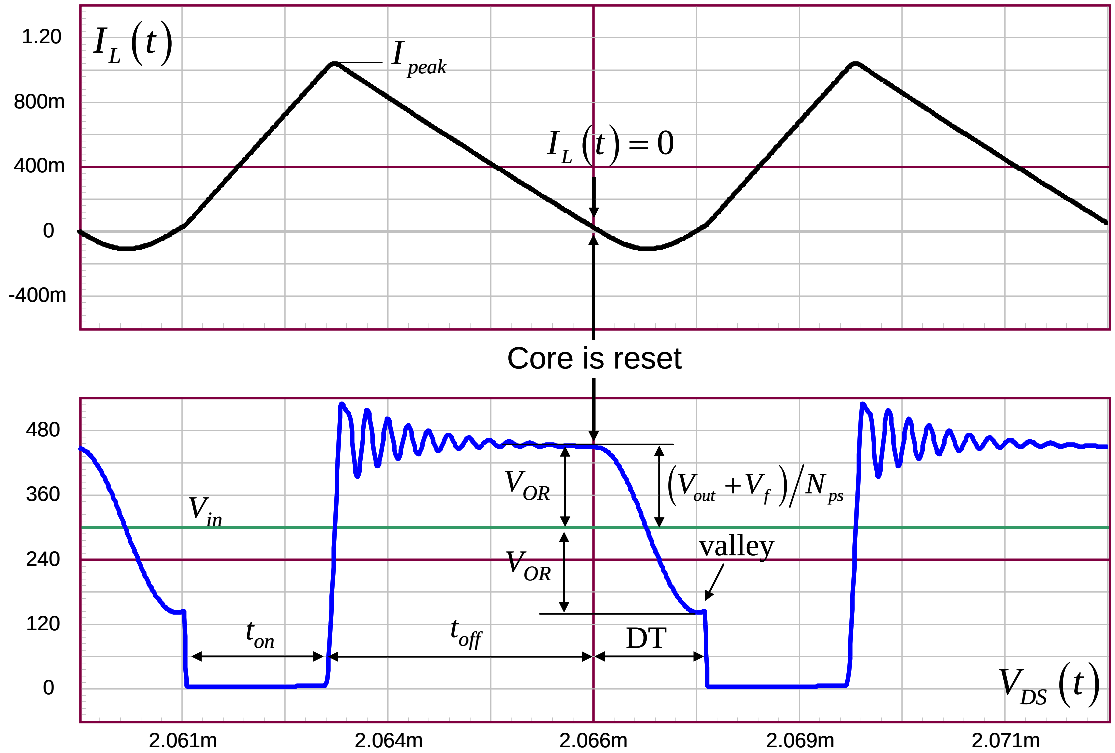

Fig.1. When a flyback converter operates in continuous-conduction mode, the current flowing through the magnetizing inductor of the transformer, $I_L(t)$, ramps from a valley point up to a peak value (I_{peak}).

An integrated circuit controlling a QR converter does not include a fixed-frequency clock. Rather, it operates in self-relaxing mode: at power-on, the MOSFET is turned on and the current ramps up in the primary inductance at a slope defined by:

$$S_{on}=\frac{V_{in}}{L_p} \tag{1}$$

However, the pace at which the peak current value is reached depends on the input-line conditions. At low line, the gentle slope of this curve means that the on-time duration for the MOSFET is high. At high line, the slope is steeper and the peak current value is reached more quickly, so the MOSFET's on-time is shorter. When the peak is reached, the controller instructs the MOSFET to switch off. The flyback voltage immediately appears on the primary side and demagnetization of the transformer takes place. The down slope affecting the primary inductor current now becomes:

$$S_{off}=-\frac{V_{out}+V_f}{NL_p} \tag{2}$$

where N is the turns ratio linking the primary and the secondary windings, V_{out} is the output voltage, V_{in} is the input voltage, V_f is the forward voltage drop of the secondary-side diode and L_p is the transformer's primary inductance.

When the inductor current reaches zero, there is no energy left in the transformer core. The magnetic circuit in this state is said to be reset. At the time the primary current has reached zero, all semiconductors on both the primary and the secondary sides are blocked. Therefore, the drain node is completely floating, "seeing" a lumped capacitance C_{lump}, charged to the flyback voltage V_{OR} plus the input voltage V_{in}. As this capacitor voltage must return to its rest level V_{in}, it will naturally discharge through an oscillation involving the primary inductance L_p, damped by the various ohmic losses present in the path. We can show that the oscillation frequency obeys the following equation:

$$F_{osc} = \frac{1}{2\pi\sqrt{L_p C_{lump}}} \quad (3)$$

The oscillation is thus straddling the input voltage level, going through ups $(V_{in} + V_{OR})$ and downs, the valleys, equal to $(V_{in} - V_{OR})$. The dead-time duration is therefore adjusted by the designer so that the MOSFET turn-on event occurs exactly when the drain voltage is in one of these valleys, hence the eponymous term for these converters, which are sometimes referred to as valley-switching converters. To perform valley switching, the dead-time DT must equal half of the natural oscillation period defined by equation (3). Its duration is therefore:

$$\mathrm{DT} = \pi\sqrt{L_p C_{lump}} \quad (4)$$

A time-delay of duration DT is then inserted into the control loop by the dedicated controller, which waits for a certain amount of time before reactivating the power MOSFET once the core reset is detected. During this time, the free oscillation reaches the valley, naturally discharging the voltage on the parasitic drain capacitor. If we assume a primary inductance of 350 µH and a lumped capacitance on the drain of 200 pF, then half of the oscillating period corresponds to a delay of:

$$\mathrm{DT} = 3.14 \times \sqrt{350u \times 200p} = 831\mathrm{ns} \quad (5)$$

Deriving The Switching Frequency

As explained in the introduction, a QR converter is, in essence, a self-relaxing structure. A change in its operating conditions, delivered power or input voltage, will modify its operating frequency and its power capabilities. To compute the maximum power it can deliver, we must know two key parameters that are the inductor peak current and the switching frequency. Let us start by “zooming in” on the primary and secondary currents as shown in Fig. 2:

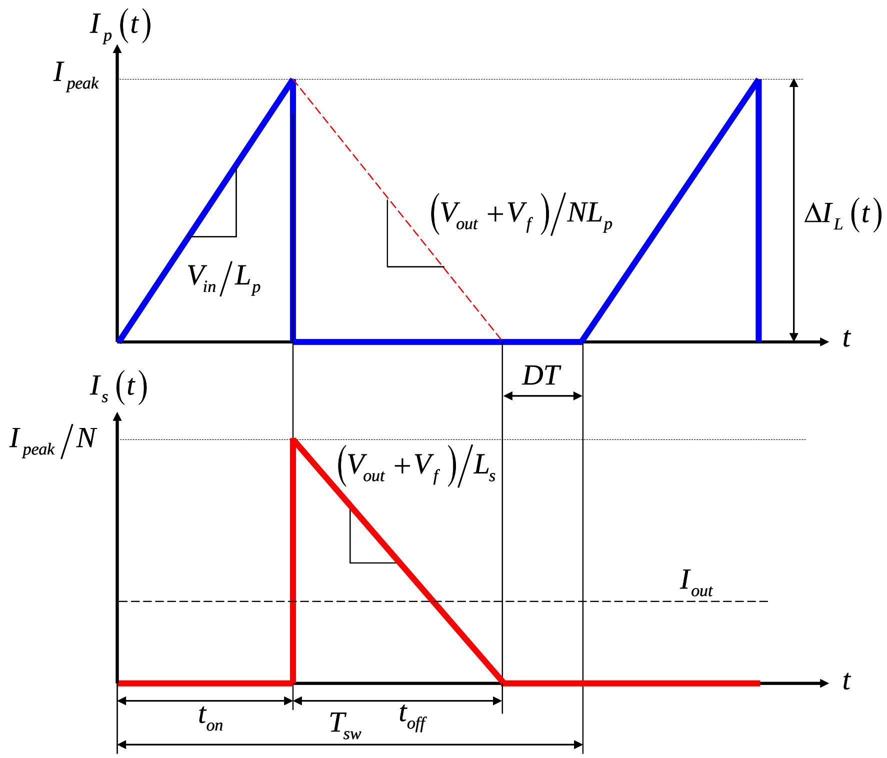

Fig. 2. Zooming in on the primary- and secondary-current waveforms helps us to derive the basic equations for a QR converter.

From these curves, we can start writing a few pertinent equations to describe the power MOSFET's on and off times. The peak inductor current I_L depends on the primary slope and the on-time:

$$I_{L,peak} = S_{on} t_{on} \tag{6}$$

If we extract t_{on} and replace S_{on} with equation (1), we have

$$t_{on} = \frac{L_p}{V_{in}} I_{L,peak} \tag{7}$$

The demagnetization time is the time needed for the inductor current to decrease from I_{peak} down to zero:

$$I_{L,peak} = -S_{off} t_{off} \tag{8}$$

Replacing S_{off} with its definition in equation (2) and solving for t_{off}, we obtain:

$$t_{off} = I_{L,peak} \frac{NL_p}{V_{out} + V_f} \tag{9}$$

Having on hand t_{on}, t_{off} and DT, the switching period T_{sw} is simply the sum of these three components:

$$T_{sw} = t_{on} + t_{off} + \mathrm{DT} \tag{10}$$

The power transmitted by a flyback converter operated in the discontinuous-conduction mode obeys the following expression:

$$P_{out} = \frac{1}{2} L_p I_{L,peak}{}^2 F_{sw} \eta \tag{11}$$

In this expression, F_{sw} is the operating switching frequency, I_L the primary inductor peak current and η (eta) the total efficiency. In a system where the loop controls the peak-current setpoint, equations (7) and (9) are likely to change and so will the operating frequency. As a result, we have two unknowns in equation (11): the peak-current setpoint and the switching frequency. Let's extract the peak current from equation (11):

$$I_{L,peak} = \sqrt{\frac{2T_{sw}P_{out}}{L_p \eta}} \tag{12}$$

With this definition, we can substitute it for I_{peak} in equations (7) and (9):

$$t_{on} = \frac{L_p}{V_{in}} \sqrt{\frac{2T_{sw}P_{out}}{L_p \eta}} \tag{13}$$

$$t_{off} = \sqrt{\frac{2T_{sw}P_{out}}{L_p \eta}} \frac{NL_p}{V_{out} + V_f} \tag{14}$$

If we now follow equation (10), we obtain:

$$T_{sw} = \sqrt{\frac{2T_{sw}P_{out}}{L_p\eta}}\left(\frac{L_p}{V_{in}} + \frac{NL_p}{V_{out} + V_f}\right) + \mathrm{DT} \tag{15}$$

We can re-arrange this expression in a slightly different way:

$$-T_{sw} + \sqrt{T_{sw}}\sqrt{\frac{2P_{out}}{L_p\eta}}\left(\frac{L_p}{V_{in}} + \frac{NL_p}{V_{out} + V_f}\right) + \mathrm{DT} = 0 \tag{16}$$

Let's assign the following values to some of the variables:

$$x = \sqrt{T_{sw}} \tag{17}$$

$$B = \sqrt{\frac{2P_{out}}{L_p\eta}}\left(\frac{L_p}{V_{in}} + \frac{NL_p}{V_{out} + V_f}\right) \tag{18}$$

In that case, equation (16) can be rewritten as follows:

$$-x^2 + Bx + DT = 0 \tag{19}$$

The positive root of this second-order equation is found to be:

$$x = \frac{\left(B + \sqrt{B^2 + 4DT}\right)^2}{4} \tag{20}$$

If we replace *B* in equation (20) and take the inverse to get the switching frequency, a nice equation emerges:

$$F_{sw} = \frac{4}{\left(\sqrt{4\mathrm{DT} + \frac{2L_pP_{out}\left(V_f + V_{out} + NV_{in}\right)^2}{\eta V_{in}^2\left(V_{out} + V_f\right)^2}} + \frac{\sqrt{2}L_p\left(V_f + V_{out} + NV_{in}\right)\sqrt{\frac{P_{out}}{\eta L_p}}}{V_{in}\left(V_{out} + V_f\right)}\right)^2} \tag{21}$$

To check the frequency variations of a 65-W QR converter, we have designed a power supply featuring the following component values:

$V_{in,HL}$ is the dc input voltage high line, 370 V

$V_{in,LL}$ is the dc input voltage low line, 120 V

V_{out}, is the output voltage, 19 V

V_f is the forward drop of the rectifying diode at the nominal output current, 0.5 V

L_p is the transformer's primary inductance, 350 µH

C_{lump} is the lumped capacitance on the drain node, 200 pF

t_{prop} is the total propagation delay, 350 ns

R_{sense} is the sense resistor, 0.2 Ω

V_{sense} is the maximum authorized sense value, 0.8 V

N, is the turns ratio between the secondary and the primary sides, 1:0.25

η_{LL} and η_{HL} are the respective values of efficiency at low- and high-line input voltages, 85% and 89%

From equation (21), we can calculate the switching frequency for a 65-W load at both input line levels:

$$F_{sw,LL} = 39\,\text{kHz} \tag{22}$$

$$F_{sw,HL} = 71.8\,\text{kHz} \tag{23}$$

To more accurately determine the frequency variation as the input voltage changes, we have plotted the excursion of this variable in a chart presented on the left-side of Fig. 3. As you can see, the span is quite big. The worst aspect of this variation is its impact on the peak current setpoint, which has been plotted on the right-side of the figure using equations (12) and (21). The difference between the high- and low-line condition is also rather large, around 1 A.

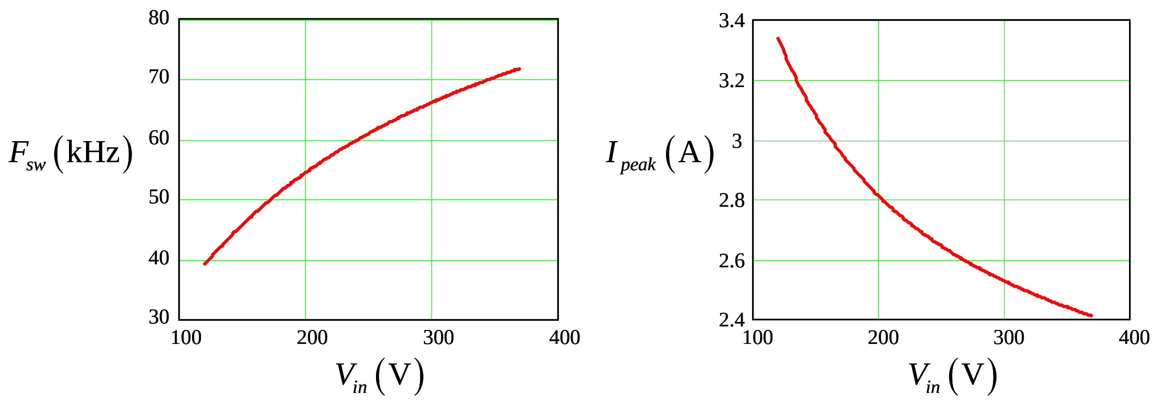

Fig. 3. The switching frequency and the peak current drastically change as the input voltage moves.

Such a wide span in the range of operating peak currents induces a real excess of output power when the controller hits the maximum peak current. Let's understand why.

The Problem Is The Limit

As explained in the previous articles, most current-mode controllers safely clamp the peak-current setpoint to a precise value in case of a feedback voltage runaway. This situation happens at start-up, for instance, where the loop remains open until the output voltage reaches its target. In a short-circuit situation, the feedback signal is also lost and the primary current must be clamped at some point. In a QR controller like the NCP1380/1379 from ON Semiconductor, an internal clamp limits the maximum excursion $V_{sense,\max}$ to 0.8 V across the sense resistor. In fault condition, the maximum inductor peak current I_L is therefore limited to:

$$I_{L,\max} = \frac{V_{sense,\max}}{R_{sense}} + S_{on} t_{prop} \tag{24}$$

In a fixed-switching frequency converter, the operating peak current at low and high line differs slightly because of the propagation-delay contribution. Therefore, if you limit the peak current to a point where you can pass the required power at low line, the power obtained at high line changes, but not by an enormous proportion. For

instance, let's assume we have a DCM converter whose maximum peak current at high line, exceeds the maximum peak current at low line by 16%. Being in DCM, the transmitted power obeys equation (11) and the output power difference between low and high line reaches (all other terms considered constant):

$$\Delta P_{out} = 1.16^2 = 1.345 = 34.5\% \tag{25}$$

This reasonable value can be compensated by the addition of a small-amplitude OPP signal as shown in the previous articles.

In a QR converter, the situation really differs because of the frequency excursion shown in Fig. 3. The low-frequency operation at the lowest input forces the designer to adopt a high peak current and a small sense resistor. In our design example, Fig. 3 indicates a peak current around 3.4 A to pass the required power at low line. To account for some margin, we selected a maximum peak current of 4 A, leading to the selection of a sense resistor of:

$$R_{sense} = \frac{V_{sense,\max}}{I_{L,\max}} = \frac{0.8}{4} = 0.2\Omega \tag{26}$$

In normal mode, at low line, the operating current will therefore be around 3.4 A and if, for some reason such as an output overload, it slightly increases by 18% to 4 A, the controller protection will quickly trip, naturally limiting the transmitted power. When the peak current is clamped in a fault condition, the switching frequency is also clamped. The switching frequency in this clamped-current condition can be directly derived from the founding equations (7), (9) and (4) since $I_{L,\max}$ is known through equation (24):

$$F_{sw} = \frac{1}{I_{L,\max} L_p \left(\frac{1}{V_{in}} + \frac{N}{V_{out} + V_f} \right) + \mathrm{DT}} \tag{27}$$

The numerical application for both input-line levels gives us the following frequency values when the peak current is pushed to its maximum limit:

$$F_{sw,LL,\min} = \frac{1}{\left(\frac{0.8}{0.2} + \frac{120}{350u} \times 350n \right) \times 350u \times \left(\frac{1}{120} + \frac{0.25}{19 + 0.5} \right) + 831n} = 32\,\mathrm{kHz} \tag{28}$$

$$F_{sw,HL,\min} = \frac{1}{\left(\frac{0.8}{0.2} + \frac{370}{350u} \times 350n \right) \times 350u \times \left(\frac{1}{370} + \frac{0.25}{19 + 0.5} \right) + 831n} = 40.7\,\mathrm{kHz} \tag{29}$$

Now that we have the operating frequencies when the converter experiences a fault at both input levels, we can express the maximum power delivered in these modes, using equation (11):

$$P_{out,\max,LL} = \frac{1}{2} L_p I_{L,peak,LL}{}^2 F_{sw,LL,\min} \eta_{LL} = 0.5 \times 350u \times \left(\frac{0.8}{0.2} + \frac{120}{350u} \times 350n \right) \times 32k \times 0.85 = 80.6\,\mathrm{W} \tag{30}$$

$$P_{out,\max,HL} = \frac{1}{2} L_p I_{L,peak,HL}{}^2 F_{sw,HL,\min} \eta_{HL} = 0.5 \times 350u \times \left(\frac{0.8}{0.2} + \frac{370}{350u} \times 350n \right) \times 40.7k \times 0.89 = 121\,\mathrm{W} \tag{31}$$

What can explain this 50% difference between the power capability at low line and that at high line? The answer lies in Fig. 4. At low line, the maximum peak current is selected to cope with the nominal power requirement. For a 3.4-A current needed at low line, we selected 4 A as a limit. Therefore, in low-line conditions, a 600-mA

increase in the current is enough to trip the protection. This is the parameter $\Delta I_{L,LL}$ that appears in the upper section of Fig. 4.

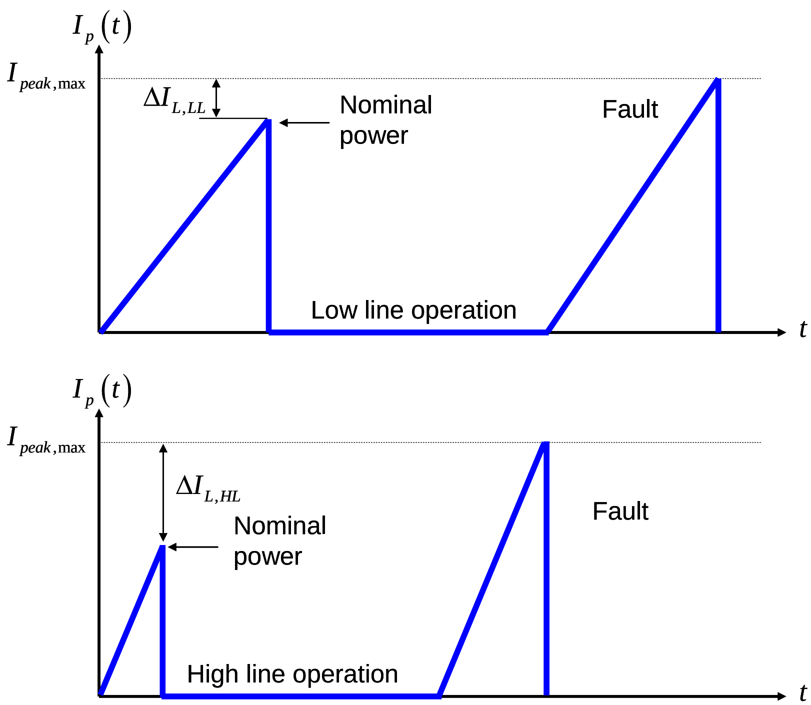

Fig. 4. Under high-line conditions, the peak current required to deliver the nominal required output power is significantly lower than the peak current required at low line. As a result, a much larger increase in current is required to trip the overcurrent protection at high line, which explains why power runaway can occur during high-line conditions before the overcurrent protection trips. This explanation assumes that the same current limit is used for both high-line and low-line operation.

The situation differs at high line. When loaded by the nominal load, the peak current reduces to 2.4 A, 1 A less than at low line. To trip the protection in this case, you need a current increase of 4 A - 2.4 A = 1.6 A, almost three times the previous excursion. This phenomenon is explained by the increase in switching frequency at high line. It allows a reduction of the operating inductor current to pass the same amount of power at high line than at low line. In this condition, a means to limit the power capability is badly needed—the over-power protection (OPP) circuitry.

Reducing The Maximum Current At High Line

As detailed in the previous articles, OPP is a known method of limiting power runaway when a faulty converter is operated at high line. In other words, techniques exist to dynamically reduce the maximum current setpoint as the input line changes.

The calculation of the compensated peak-current value for a QR converter differs from that of a fixed-switching converter because we have two unknowns, the peak current we look for and the new switching frequency at that current value. The adopted strategy is to equate the power delivered by the compensated faulty converter at high line to that delivered at low line also in fault mode. In other words, from equation (30), we will calculate the new peak current, clamped so that the converter does not deliver more than 80 W when in fault at high line. Let's calculate the corresponding frequency using equation (21) where P_{out} is now 80 W:

$$F_{sw,HL} = \frac{4}{\left(\sqrt{4\times 831\text{n} + \frac{2\times 350u\times 80\times(0.5+19+0.25\times 370)^2}{0.89\times 370^2(19+0.5)^2}} + \frac{\sqrt{2}\times 350u\times(0.5+19+0.25\times 370)\sqrt{\frac{80}{0.89\times 350u}}}{370\times(19+0.5)}\right)^2}$$

$$= 59.2\,\text{kHz} \quad (32)$$

From this value, we can extract the necessary peak current using equation (12):

$$I_{L,\max,CMP} = \sqrt{\frac{2P_{out}}{\eta L_p F_{sw}}} = \sqrt{\frac{2\times 80}{0.89\times 350u\times 59.2k}} = 2.95\,\text{A} \quad (33)$$

This value reflected as a current-sense setpoint needs to account for the propagation delay:

$$V_{sense,\max,CMP} = R_{sense}\left(I_{L,\max,CMP} - \frac{V_{in,HL}}{L_p}t_{prop}\right) = 0.2\times\left(2.95 - \frac{370}{350u}\times 350n\right) = 516\,\text{mV} \quad (34)$$

As our controller features an internal 0.8-V reference voltage, from equation (34), it must be reduced at high line to:

$$V_{OPP} = V_{sense,\max} - V_{sense,\max,CMP} = 0.8 - 0.516 = 284\,\text{mV} \quad (35)$$

In other words, the 0.8-V internal reference has to be reduced by 35.5% when the converter is supplied from a high-line input. The NCP1380/1379 use the same non-dissipative proprietary OPP technique as the one implemented in the NCP1250. Please refer to parts 1 and 2 of this series to learn about this method.

Once the OPP circuitry is implemented, we can now plot the power capability of the compensated converter and compare it to that of the non-compensated one. The curves appear in Fig. 5.

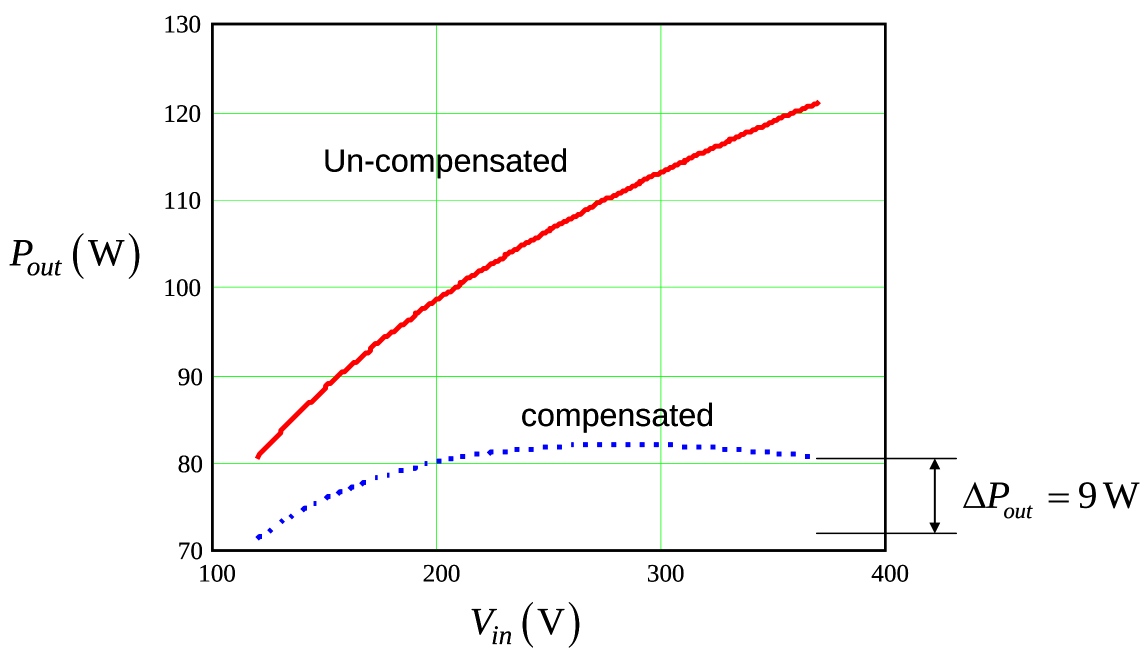

Fig. 5. Thanks to OPP the power runaway at high line is now well under control.

The compensation is efficient and keeps the output power well under control at high line, reducing the risk of thermal runaway and fire. As the OPP is also present at low line, it slightly affects the maximum delivered power. In our case, it goes down to around 71 W as indicated in Fig. 5.

Conclusion

Part 1 of this article explained why a flyback converter operated in the discontinuous-conduction mode or in the continuous-conduction mode could deliver more power at high line than at low line when operated at a fixed-switching frequency. In a QR converter, the switching frequency varies and depends on the operating conditions, making the output power runaway at high line worse than in the fixed-frequency case. Despite the increase of unknowns in the equations, we have shown here in part 3 of this article that the compensation technique required by a QR converter does not really differ from that of a fixed-frequency converter. In the end, the application of the OPP technique discussed here leads to a nicely compensated power chart.

References:

1. C. Basso, "The Over-Power Phenomenon In DCM/CCM-Operated Flyback Converters (Part 1)" How2Power Today, October 2010.

2. C. Basso, "The Over-Power Phenomenon in DCM/CCM-Operated Flyback Converters (Part 2): Fixed-Frequency CCM Operation" How2Power Today, November 2010.

About The Author

Christophe Basso is an application engineering director at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he authored a second book, "Switch-Mode Power Supplies: SPICE Simulations and Practical Designs", published by McGraw-Hill in 2008. His work was positively reviewed in several magazines and in a recent PELS newsletter. Christophe holds a BSEE-equivalent from the Montpellier University, France and a MSEE from the Institut National Polytechnique de Toulouse, France. He holds 17 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on power protection, see the How2Power Design Guide, search the Design Area category and select Power Protection as the subcategory.