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# Paralleling Electrolytic and Ceramic Capacitors Perks Up POL Transient Response

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The distributed power supply architecture, pervasive in myriad applications including communications infrastructure equipment and computing systems, uses an intermediate bus and multiple downstream dc-dc regulators dedicated and proximate to each "point-of-load." The ASICs, FPGAs, and microprocessors that comprise these loads have supply voltage requirements whose levels are decreasing on an absolute basis and whose tolerance bands are decreasing on a percentage basis.

This trend is compounded in the face of rapidly increasing supply current amplitudes and slew rate demands, and it becomes imperative to understand the effects of load-current transient demands in the context of the static and dynamic regulation voltage constraints. The hallmarks of point-of-load (POL) dc-dc regulators are efficiency, load transient response, and cost. The single-phase synchronous buck converter [1,2] has proven over time to be the definitive, preferred and universally-used POL topology with 12-Vdc bus voltage and low to medium load currents (up to 25 A).

Ordinarily, the POL regulator's output capacitor energy store combined with its control loop response are prescribed to maintain the integrity of the output voltage within both the static and transient tolerance margins. Two limitations are materially apparent:

- the output capacitor and
- the control loop bandwidth.

The usual boundaries restricting the output capacitor in power management applications are driven by finite available pc-board area, component footprint and profile specification, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take increasing precedence in shaping the regulator's load transient response as the output current ramp amplitude and slew rate increase.

The second limitation relates to the switching frequencies of POL regulators, typically ranging from 250 kHz to 750 kHz and limited by, for example, excessive frequency-proportional switching losses (especially at high output currents), thermal limitations or EMI concerns. As a consequence, the control-loop bandwidth, normally constrained to 20% of the switching frequency when conventional fixed-frequency linear control schemes are employed, is relatively low. For example, a POL regulator switching at 300 kHz has a modest maximum practical loop bandwidth of just 60 kHz.

That said, it's worthwhile to obtain some perspective not only on POL step-load transient behavior, but also its dependence on the output filter capacitance. In this article, we'll explore the rationale of paralleling capacitors of dissimilar chemistries yet complementary performance. The load transient waveforms will be reported using time-domain simulation, allowing examination of the key indices of load transient performance–peak deviation and settling time. Lastly, we'll assess the implementation of a POL module based on a commercially available PWM controller IC.

## POL Regulator Transient Response

Fig. 1 represents the model of a buck regulator that serves as the template for the subsequent discussion. The three-element model of the output filter capacitor denotes the ESR and ESL explicitly. Detailed modeling of the temperature and frequency dependence of the various capacitor elements or the dielectric leakage losses is superfluous to this discussion.

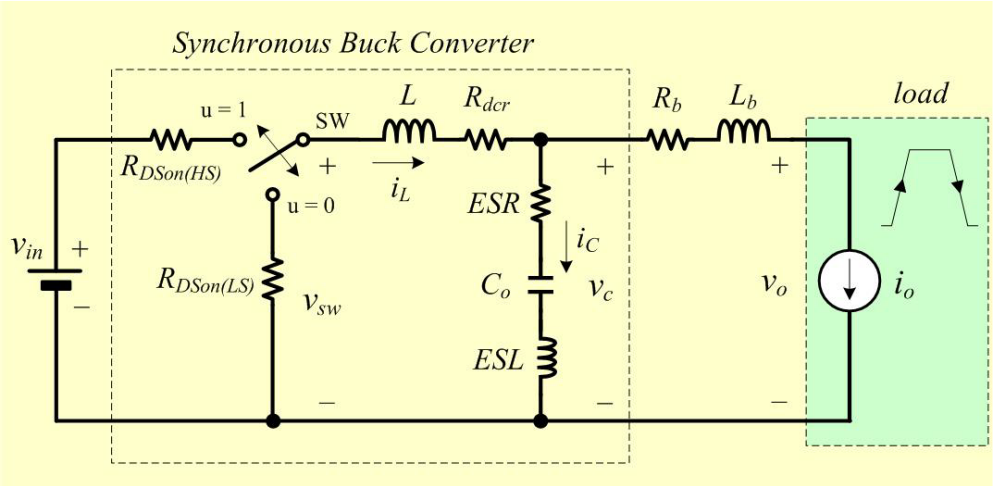


*Fig. 1. Single-phase dc-dc synchronous buck regulator model.*

The resistive parasitic components of the filter inductor $R_{dcr}$, power MOSFETs $R_{DS(on)}$, and PCB trace and connection resistance $R_b$ of the power delivery path are also shown in Fig. 1. To the extent that its effect is far above the frequency range of interest, parasitic inductance in the power path, denoted by $L_b$, is usually overlooked. This is especially true if numerous small capacitors are connected immediately adjacent to the load, for example in the socket cavity of a microprocessor. A time-varying current source $i_o(t)$ is used to model the load. Note that the "remote" sensing point of the output voltage $V_o$ is purposely located on the load side of the bus resistance $R_b$.

Fig. 2 conceptually illustrates the relevant current waveforms during both load stepup and stepdown transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load-on transient. Similarly, during and after a load-off transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that needs to be depleted as quickly as possible.

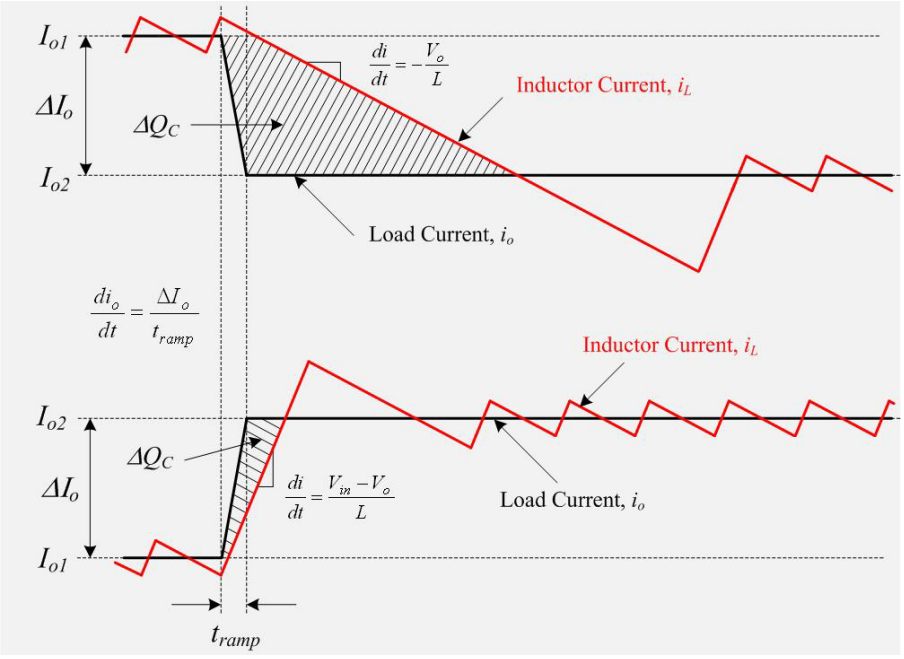


*Fig. 2. Conceptual representation of the load transient response illustrating surplus or deficit of charge in the output capacitor.*

In a typical POL application of 12-V input to low output voltage (say 1.2 V), it must be emphasized that the load-off transient represents worst-case. Here, the steady-state duty cycle is approximately 10% and the large-signal inductor current slew rate when the duty cycle collapses to zero (u = 0 in Fig. 1) is approximately –Vo/L. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and rein in the voltage overshoot.

Also, the location in the PWM cycle where the transient occurs is important: worst-case for a load-off transient is at the end of the PWM cycle when inductor current is at its peak (as illustrated in Fig. 2.)

## *Polymer Electrolytic Capacitors*

The use of a highly conductive solid polymer electrolyte in place of the more common liquid electrolyte in aluminum and tantalum electrolytic capacitors results in greatly improved electrical properties: reduced ESR, higher ripple-current rating and extended MTBF and operational life. The electrolyte acts as the electrical connection between the negative cathode and the dielectric.

The development of better electrolytes has primarily focused on reducing the ESR and increasing the ripple current rating by using higher conductivity materials. Improving the capacitor's electrical characteristics over temperature (specifically at low temperature) and assuaging concerns related to safety with more benign failure modes and suppression of combustion have also driven R&D in electrolytes. Polymer electrolytic capacitors, like their wet electrolyte counterparts, are polarized with the polarity bar normally designating the positive terminal.

Low ESR and high capacitance are the major design benefits of polymer electrolytic capacitors facilitating reduced board space because of the ability to replace numerous multi-layer ceramic capacitors (MLCCs) with just one, high-capacitance poly device. These features further enable excellent noise suppression, ripple absorption and decoupling abilities. In addition, polymer electrolytics offer capacitance stability at high operating frequencies and with applied voltage and high temperatures. Last but not least, the cost per unit capacitance of polymer devices is typically more favorable than ceramics.

Given the demand for low component profile, several capacitor manufacturers provide polymer capacitors in SMT resin-molded case packages, including but not limited to:

- Sanyo “POSCAP”, e.g. TPLF series [3]
- Panasonic “SP-Cap”, e.g. LX, SX series
- Murata “ECAS” series
- Kemet “KO-CAP”, e.g. T530 series
- Rubycon “PC-CON”, e.g. SXZ series
- NEC Tokin “NeoCapacitor”, e.g. PSG series
- NIC Components, e.g. NSP series and
- Cornell Dubilier, e.g. SPA series.

## *Paralleling Electrolytics And Ceramics*

A polymer electrolytic capacitor in parallel with a multi-layer ceramic capacitor is shown in Fig. 3. The frequency response of each capacitor is complementary and accretive such that each capacitor provides desirable performance over a certain portion of the frequency range of interest. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize switching frequency output ripple, the polymer device with its large bulk capacitance provides low-frequency energy storage to cope with load-transient demands.

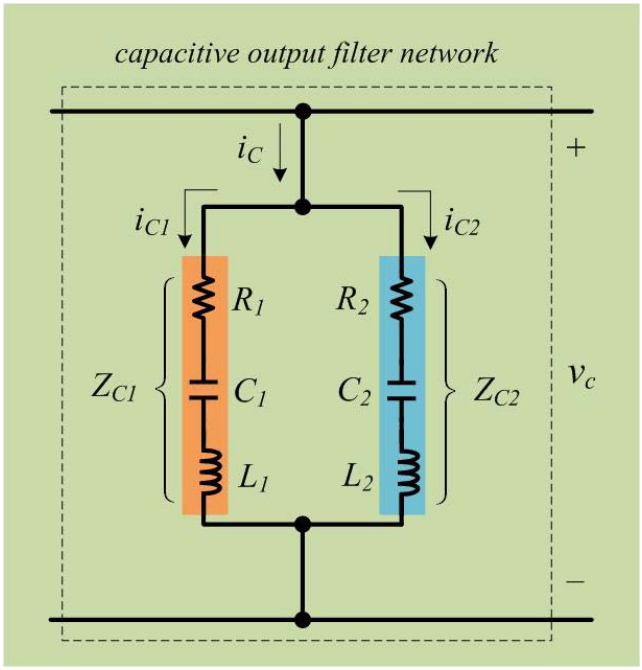


*Fig. 3. Paralleling ceramic and polymer electrolytic capacitor provides complementary performance over a broad frequency range.*

The complex impedance function of the output filter structure in Fig. 3 is given by

$$Z_C(s) = Z_{C1}(s) \| Z_{C2}(s)$$

$$= \left( R_1 + \frac{1}{sC_1} + sL_1 \right) \Bigg\| \left( R_2 + \frac{1}{sC_2} + sL_2 \right)$$

$$= \frac{\left(1 + sR_1C_1 + s^2L_1C_1\right)\left(1 + sC_2R_2 + s^2L_2C_2\right)}{s(C_1 + C_2)\left(1 + s(R_1 + R_2)\frac{C_1C_2}{C_1 + C_2} + s^2(L_1 + L_2)\frac{C_1C_2}{C_1 + C_2}\right)} \quad (1)$$

The magnitude and phase of the impedance of the output filter capacitor bank is given by

$$|Z_C(s)| = \frac{|Z_{C1}(s)| \cdot |Z_{C2}(s)|}{|Z_{C1}(s) + Z_{C2}(s)|}$$

$$= \frac{\sqrt{R_1^2 + X_1(s)^2}\sqrt{R_2^2 + X_2(s)^2}}{\sqrt{(R_1 + R_2)^2 + (X_1(s) + X_2(s))^2}}$$

$$\text{where } X_{1,2}(s) = \frac{1}{sC_{1,2}} + sL_{1,2} \quad (2)$$

$$\angle Z_C(s) = \angle Z_{C1}(s) + \angle Z_{C2}(s) - \angle\left(Z_{C1}(s) + Z_{C2}(s)\right)$$

$$= \tan^{-1}\left(\frac{X_1(s)}{R_1}\right) + \tan^{-1}\left(\frac{X_2(s)}{R_2}\right) - \tan^{-1}\left(\frac{X_1(s) + X_2(s)}{R_1 + R_2}\right) \quad . \qquad (3)$$

The effective ESR and capacitance at a particular angular frequency, $\omega$, are expressed as

$$ESR_{eff}(\omega) = \mathrm{Re}\left(Z_C(j\omega)\right) = \left|Z_C(j\omega)\right|\cos\left(\angle Z_C(j\omega)\right)$$

$$C_{oeff}(\omega) = \frac{-1}{\omega\,\mathrm{Im}\left(Z_C(j\omega)\right)} = \frac{-1}{\omega\left|Z_C(j\omega)\right|\sin\left(\angle Z_C(j\omega)\right)} \quad . \qquad (4)$$

The total current distributes in each capacitor depending on the relative impedance of each capacitor at a given frequency and can be found using the current-divider rule. The capacitor voltage ripple, vC(t), is found by taking the FFT of the triangular capacitor current waveform, iC(t), convolving it with the complex impedance function of the output filter network and then performing an inverse FFT to yield the time-domain waveform. A brick-wall filter function can be applied to the FFT to act as an anti-alias filter above, for example, nine harmonics of the fundamental.

Practical choices of capacitors to investigate in more detail are described as follows; the relevant specifications and ratings are outlined in Table 1 [3,4].

- TDK 100-µF X5R 6.3-V 1206 multilayer class-II ceramic capacitor [4]. Fine ceramic material layers are sintered with highly accurate internal electrode material laminations. Capacitance derates significantly with applied dc bias (large capacitance voltage coefficient). ESR is very low. Susceptible to the piezoelectric effect.
- Sanyo 270-µF POSCAP [3] TPSF series “B case” capacitor with conductive polymer electrolyte and tantalum dioxide dielectric. Face-down construction is provided to facilitate low ESL. Multi-anode construction and high-conductivity electrolyte provide low ESR. Capacitance and ESR are relatively stable over the operating voltage and temperature range. Allowable RMS ripple current is limited by ESR power dissipation and, importantly, operating temperature.

Table 1. Polymer electrolytic and ceramic capacitor parameters and specifications [3,4].

| Capacitor Vendor | TDK | SANYO |
|---|---|---|
| Vendor P/N | C3216X5R0J107M | 2TPSF270M9G |
| Family | Class-II Ceramic | POSCAP Polymer Electrolytic |
| Capacitor Dielectric | BaTi03 | Tantalum-oxide film |
| Voltage Rating | 6.3 V | 2 V |
| Current Rating | 4 Arms at 500 kHz<br>10°C temp. rise | 2.4 Arms at 45°C<br>100 to 500 kHz |
| Temperature Rating | -55°C to +85°C<br>(X5R ±15%) | -55°C to +105°C |
| Package Size | 3.2 x 1.6 x 1.6 mm<br>(EIA 1206) | 3.2 x 2.8 x 1.9 mm<br>(B2) |
| Co | 100 µF ±20% | 270 µF ±20% |
| ESR | 2 mΩ at 300 kHz | 6 mΩ (typ.)<br>9 mΩ (max) at 300 kHz |
| ESL | 0.5 nH | 0.7 nH |
| Estimated Cost<br>(EAU 10 million pcs) | $0.30 (MOQ 2k/reel) | $0.31 (MOQ 2k/reel) |

Using equations (1) through (3), Figs. 4 and 5 plot the impedance magnitude and phase of the TDK and Sanyo capacitors and the same parameters when both components are in parallel.

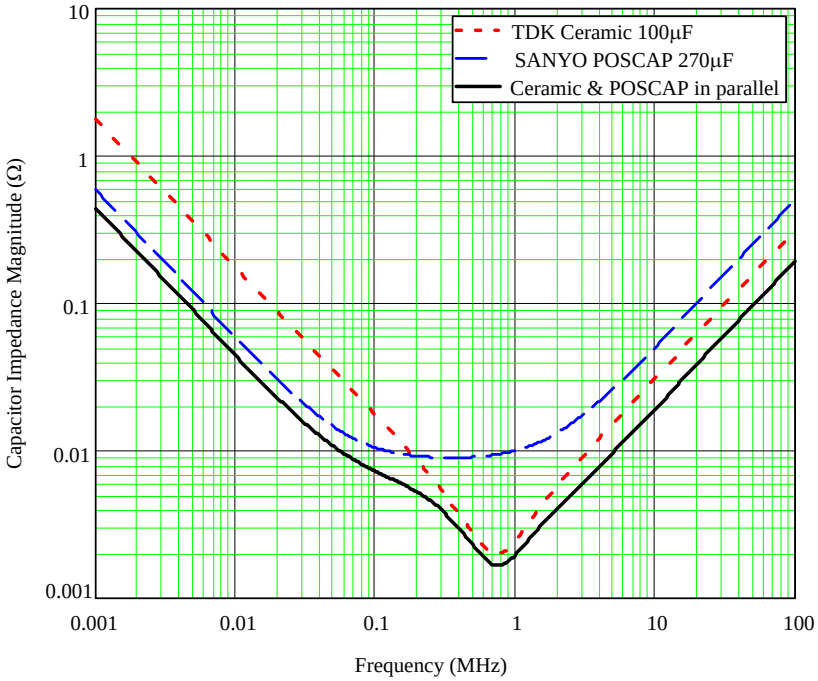


*Fig. 4. Output capacitor impedance magnitude vs. frequency plots.*

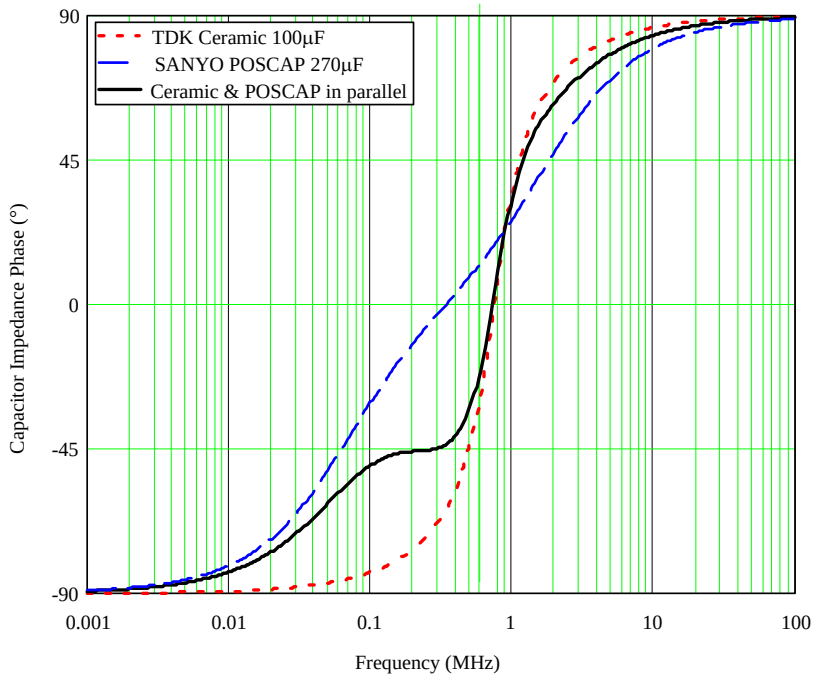


*Fig. 5. Output capacitor phase vs. frequency plots.*

Tantamount to the lower impedance in the low-frequency range (below 100 kHz) is the large bulk capacitance of the POSCAP. The low ESR and ESL of the ceramic optimize the impedance characteristic between 100 kHz and 2 MHz whereas the impedance above 2 MHz is effectively the components' ESLs in parallel. To assist with the control-loop compensation, the equivalent ESR zero frequency occurs when the phase is -45° and the real and reactive impedance components are equal. Using equation (4), the effective ESR is plotted versus frequency in Fig. 6.

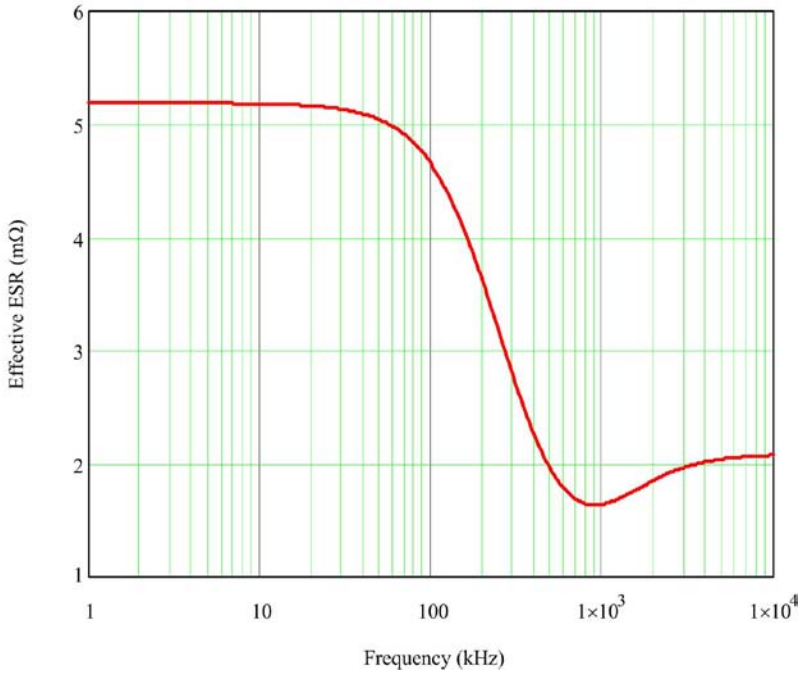


*Fig. 6. Effective ESR vs. frequency.*

## *Simulation*

With the circuit operating conditions and key component values listed in Table 2, a SIMPLIS circuit simulation is presented in Fig. 7 to inspect the output-voltage transient-response characteristic.

Table 2. Specification and nominal values of the POL simulation.

| | | |
|---|---|---|
| **Line and Load Conditions** | | |
| $V_{in}$ = 12V | $I_{o1}$ = 5 A | $I_{o2}$ = 15 A |
| Slew Rate $I_{out}$ = 25 A/μs | | |
| **Power-Stage Components** | | |
| $R_{DSon(HS)}$ = 5 mΩ | $R_{DSon(LS)}$ = 1.5 mΩ | |
| $L$ = 0.68 μH | $R_{dcr}$ = 5 mΩ | |
| $C_1$ = 90 μF | $R_1$ = 2 mΩ | $L_1$ = 0.5 nH |
| $C_2$ = 270 μF | $R_2$ = 9 mΩ (max.) | $L_2$ = 0.7 nH |
| **PWM-Controller Parameters** | | |
| $f_c$ = 55 kHz | Type-III voltage-mode compensation | |
| **Static and Dynamic Regulation Requirements** | | |
| $V_{out}$ = 0.9 V | $\Delta V_{out(max)}$ = 0.1 V | $f_s$ = 300 kHz |

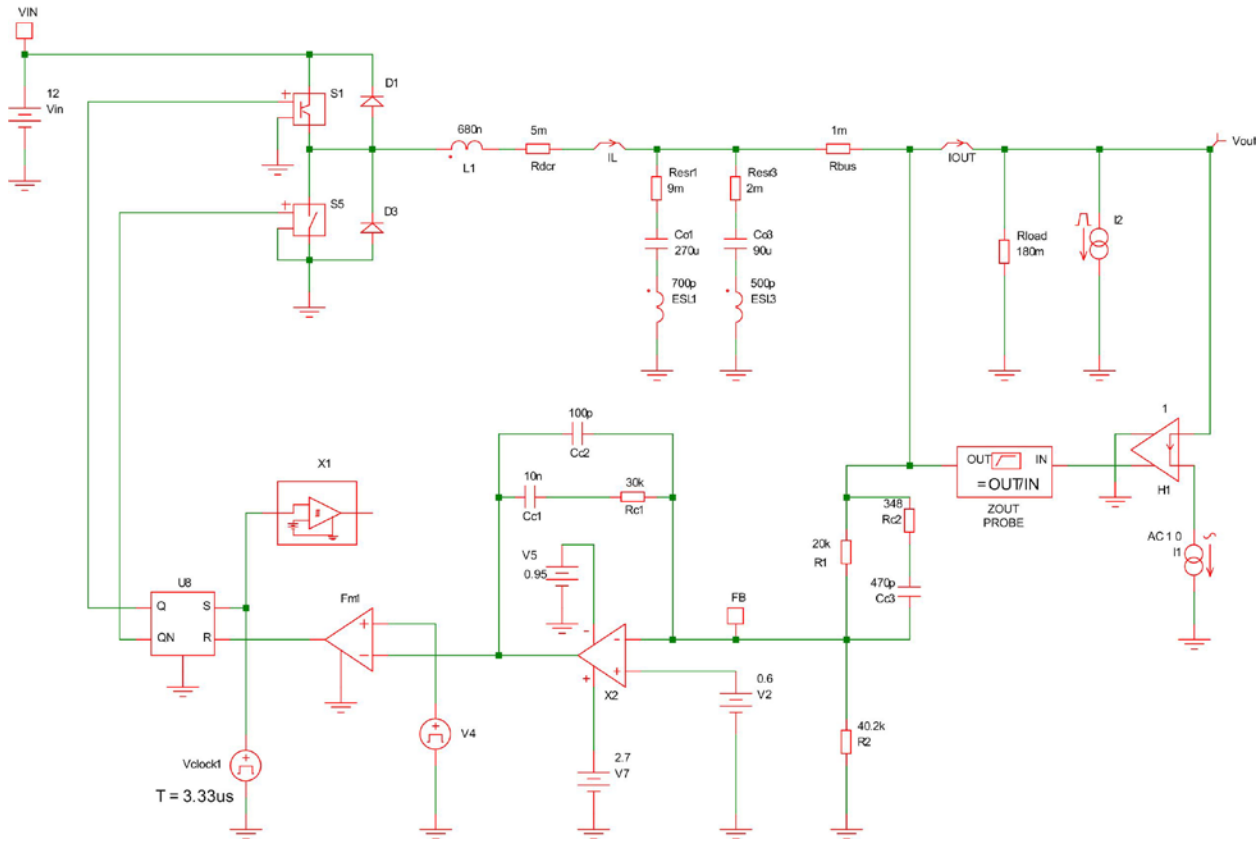


*Fig. 7. LM27402-based buck converter transient analysis simulation schematic.*

Load-on and load-off transient responses are obtained with current slew rates of 25 A/μs. Using type-III voltage-mode loop compensation with the crossover frequency set at 50 kHz, the results are plotted in Fig. 8. Two output-capacitor configurations are simulated:

Cout #1: one 270-μF SANYO POSCAP in parallel with one 100-μF TDK ceramic;
Cout #2: two 100-μF TDK ceramics in parallel.

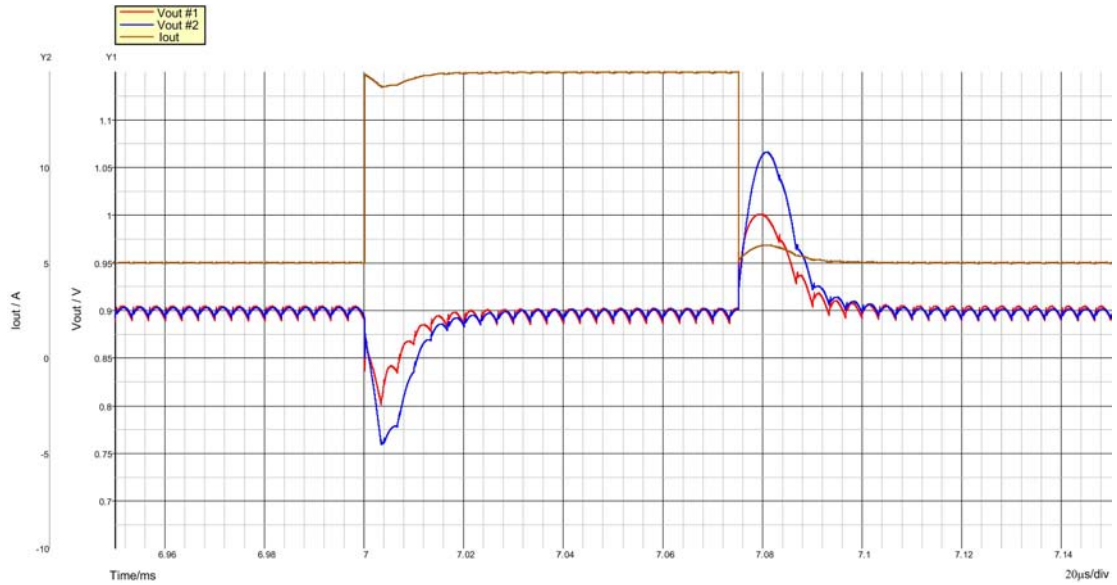


*Fig. 8. Simulated 10-A load-step transient response with two output-capacitor configurations.*

Interestingly, the total capacitor solution footprint is similar in both cases. As indicated in Table 2, the ceramic capacitance is derated by 10% on the basis of its capacitance voltage coefficient at 0.9 Vdc bias. Figs. 7 and 8 show the simulation schematic and transient response results, respectively. The loop bandwidth is held approximately constant by changing compensation resistor Rc1 in Fig. 7 from 30 kΩ to 15 kΩ, hence ensuring similar loop performance with both capacitor configurations.

It is evident from Fig. 8 that the paralleled POSCAP and ceramic of configuration #1 provides better performance (see red voltage trace) with approximately 40 mV and 65 mV reduction in peak deviation during the load-on and load-off steps, respectively. In percentage terms, those reductions in peak deviation equate to a 30% and a 40% improvement, respectively. During the load-off transient, the duty cycle becomes saturated at zero and the open-loop output impedance, plotted in Fig. 9, determines the response. Implicit with the lower output peak deviation of the POSCAP configuration is that the open-loop output impedance between 11 kHz and 100 kHz in Fig.9 is lower (by as much as 9 dBΩ) relative to the arrangement with two ceramics.

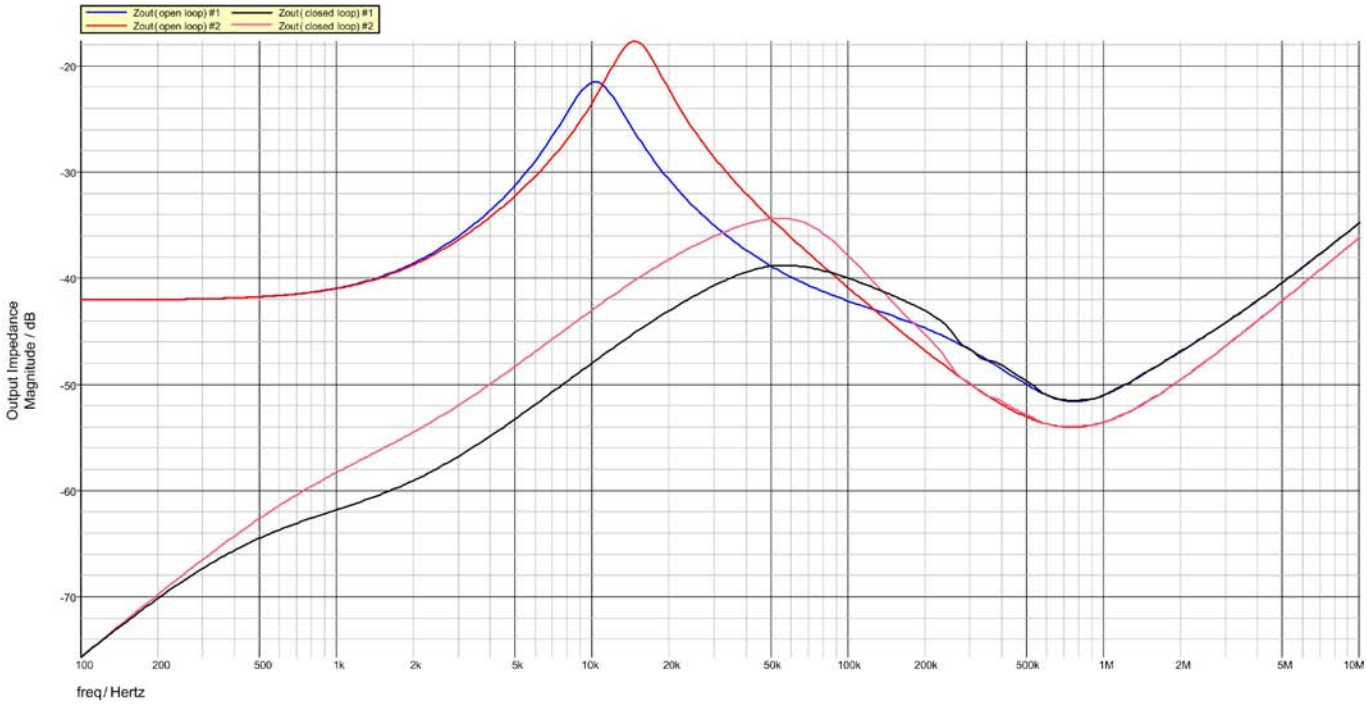


*Fig. 9. Simulated open- and closed-loop output impedance plots with two output capacitor configurations.*

## POL Module Implementation

Let's use the quantitative information captured up to now and consider a design and implementation based on the parameters of Table 2. The double-sided PCB of an LM27402[1]-based POL regulator is shown in Fig. 10. This module provides high current and power densities with dimensions of 0.85 in. x 0.73 in. x 0.24 in. To capture a multiplicity of intermediate bus rails, a wide input voltage range of 3 V to 20 V is available.

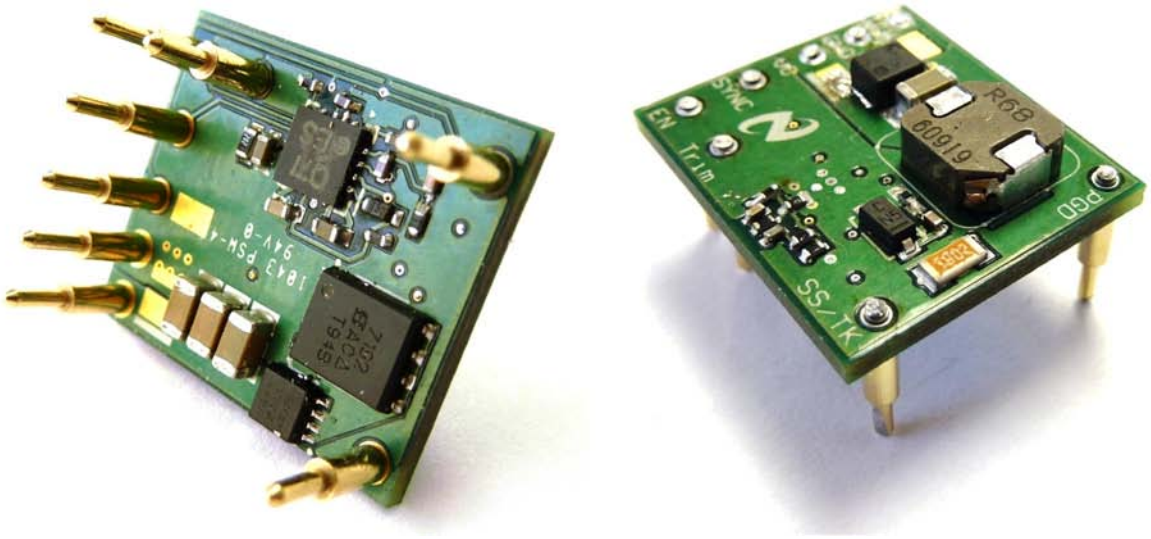


*Fig. 10. A POL module implementation based on the LM27402 buck controller—PCB top and bottom sides.*

The scope shot of load transient response in Fig. 11 demonstrates the lower peak deviation attainable with the POSCAP capacitor configuration, albeit with slightly longer settling time. There is some subjectivity related to when the oscilloscope is triggered as the load-off peak deviation varies somewhat depending on where in the switching cycle the transient occurs. The voltage waveforms in Fig. 11 represent the response when the transient occurs midway through the switching cycle (i.e. when the inductor current approximately equals the load current).

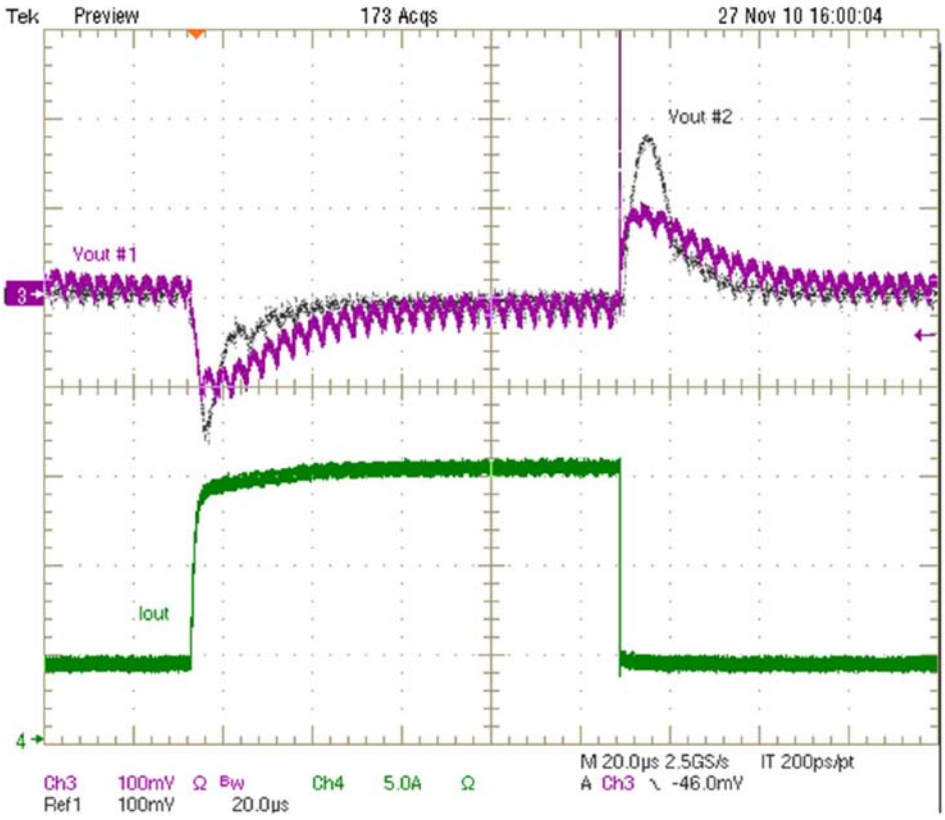


*Fig. 11. Measured POL module 10-A load step transient response with two output capacitor implementations.*

## References

1. National Semiconductor, LM27402 High Performance Synchronous Buck Controller with DCR Current Sensing from the PowerWise Family, http://www.national.com/pf/LM/LM27402.html.

2. National Semiconductor, LM21215 High Performance 15-A Synchronous Buck Regulator from the PowerWise Family, http://www.national.com/pf/LM/LM21215.html.

3. Sanyo Electric Capacitors General Catalog 2010-7, http://us.sanyo.com/Electronic-Devices-Components/POSCAP.

4. TDK SEAT Ceramic Capacitor Technical Guide, http://www.tdk.com/cap_technotes.php#.

## About the Author

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For more on transient response of point-of-load regulators, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category, and select “Transient Response” in the Design Area category.