Voltage-Mode Control Scheme Improves Buck Converter Performance At High Frequencies

by Suresh Kariyadan and Parviz Parto, International Rectifier, El Segundo, Calif.

The typical mother board used in today's netcom, server, embedded telecom, and storage applications contains up to fifteen different point-of-load regulators (POLs) that deliver anywhere from less than 1 A up to 30 A of output current. These POLs, which typically step down an intermediate voltage bus to the supply voltages required at the chip level, are generally implemented using synchronous buck converter ICs.

Requirements such as small size, low cost, fast transient performance, and power sequencing, have driven the development of synchronous buck converter ICs with enhanced capabilities. Some of the advanced features expected on newer-generation POL ICs are jitter-free operation at higher switching frequencies, higher closed-loop bandwidth, input-voltage feed forward, and built-in drivers along with MOSFETs contained inside the same package. Some IC vendors have also added a voltage-tracking function to be used for a memory V_{tt} rail power supply with source-and-sink current capability. End customers benefit from this function because they can use the same IC for many different functions on the mother board.

Higher operating frequency combined with jitter-free operation allows the design to run at higher closed-loop bandwidth, which results in the use of fewer output capacitors, saving board space and system cost. This article will explain the theoretical details of a new pulse-width modulator scheme for achieving jitter-free operation at high frequency and narrow duty cycle using a voltage-mode controller. This modulator scheme has been implemented in International Rectifier's IR3899 synchronous buck regulator, which also contains built-in features that provide enhanced flexibility in implementing POL designs. Test results obtained with the IR3899 will be presented to demonstrate the performance advantages of the new modulator scheme versus a traditional voltage-mode controller. In addition, the special features found on the IR3899 will described.

Voltage-Mode Control

The traditional voltage-mode control scheme is widely used in dc-dc power conversion for point-of-load buck converters (POLs). This scheme can be used to step down a dc voltage to a lower dc voltage efficiently and accurately. The pulse width determines how long the power from input source is applied to the converter circuit through a switch. Then an LC filter is used to get a smooth dc voltage and current at the output. It regulates output voltage by regulating the pulse width. Pulse width is the required on-time for the switch to be kept on to regulate the output voltage. We can write duty cycle (D) as

$$D = \frac{V_{out}}{V_{in}} = \frac{T_{on}}{T_{period}} = T_{on} \times F_s$$

where V_{out} is the output voltage, V_{in} is the input voltage, T_{on} is the on-time and F_s is the switching frequency.

Fig. 1 shows the block diagram for a voltage-mode controller in a synchronous buck converter. The error amplifier receives a sample of the output voltage and compares it with a precision reference voltage, producing an error voltage (Verror) at the output. The high-speed PWM comparator receives two inputs—the output of the error amplifier and a ramp signal (Vramp). Then, the output of the PWM comparator is fed to a latch like the S-R flip flop at the Reset input and the other Set input is driven from a periodic clock signal generated internally.

This periodic clock is generated at a fixed frequency and is usually user programmable with an external resistor or a capacitor. Whenever the output voltage changes due to any reason such as variations in input voltage, load, temperature etc., the Verror signal amplitude changes, thereby changing the PWM comparator threshold and the pulse width of the PWM output. By adjusting the pulse width (duty cycle), the output voltage can be kept constant for any variation in input voltage, temperature, load, etc. The control FET and synchronous FET (Sync.Fet) are driven by HDrv and LDrv pulses, respectively from their driver section.

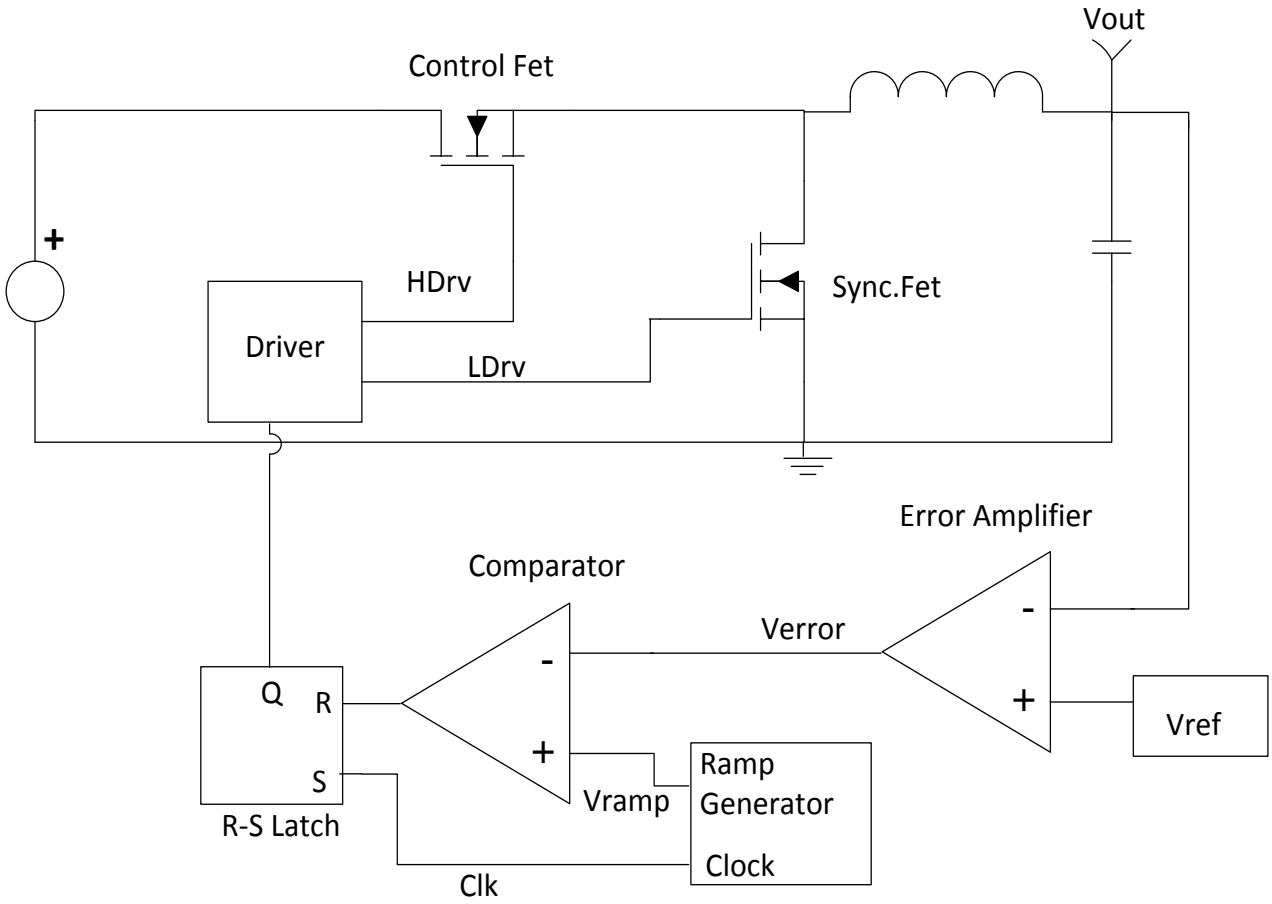


Fig. 1. Block diagram of a voltage-mode PWM controller.

In the traditional voltage-mode controller, the ramp starts at the rising edge of the PWM signal, and intersects the Verror signal at a low-voltage level (the non-linear region of the ramp) for narrow duty-cycle operation. Being nonlinear, this region can produce more jitter. In the new proposed control method, the Ramp starts earlier than the falling edge of the Set signal and the Ramp intersects Verror in a more linear region, producing a minimum amount of jitter. It can even produce zero duty cycle if the reset signal rises before the set signal falls. The theoretical waveforms are shown in Fig.2.

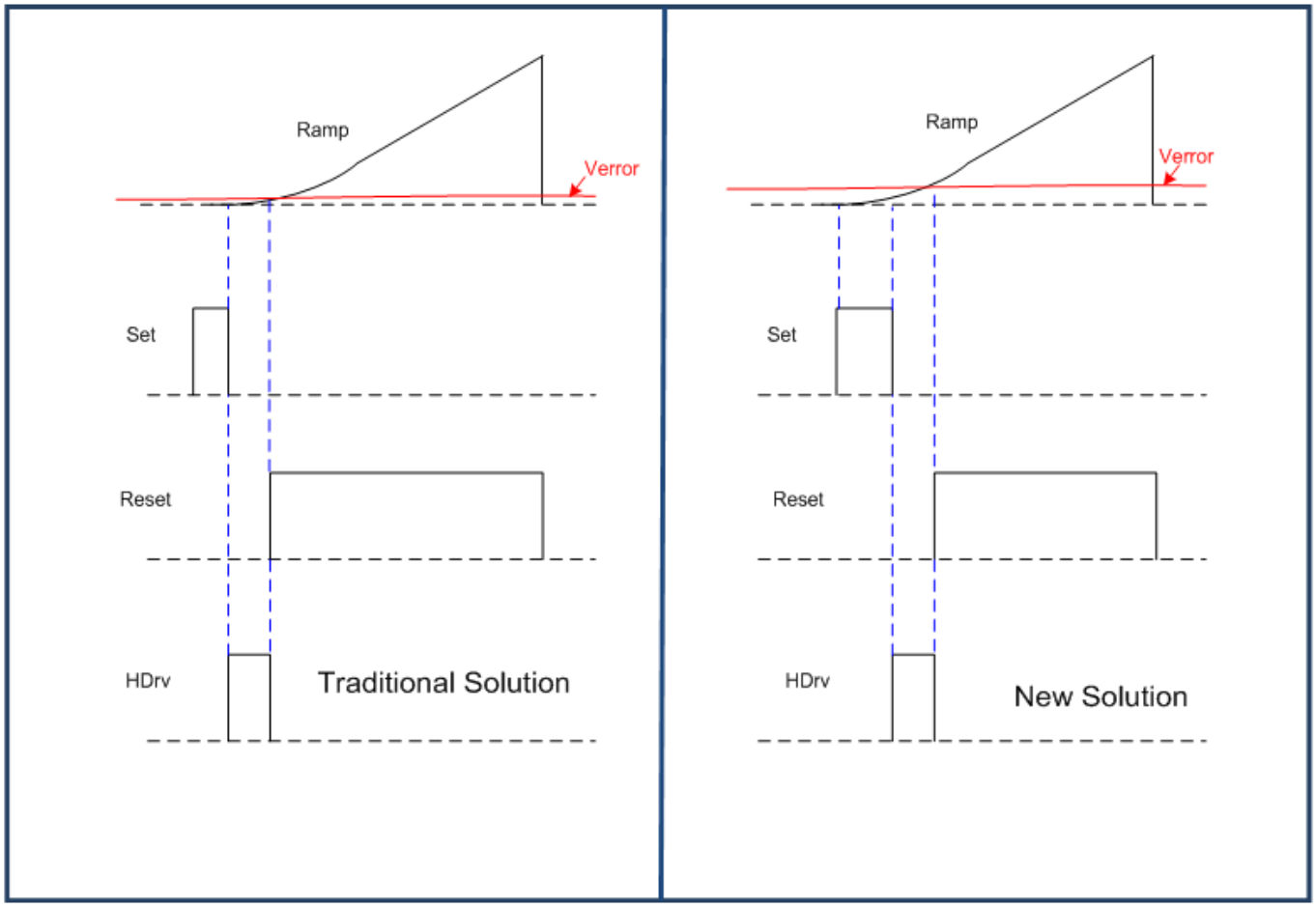


Fig. 2. Theoretical waveforms for a voltage-mode controller operating the traditional way (left) versus a controller using the proposed modulator scheme (right).

The experimental switch-node waveforms taken using the traditional voltage-mode regulator IC, and the new patented (Patent # US 7,777,587) voltage-mode regulator IC (the IR3899 from International Rectifier) are shown in Figs. 3, 4, 5, and 6. The advantage of the new scheme is clearly visible in the waveforms taken from the demo boards. At a 1.5-MHz frequency and pulse width of 50 nsec, the switch-node waveform shows very low jitter.

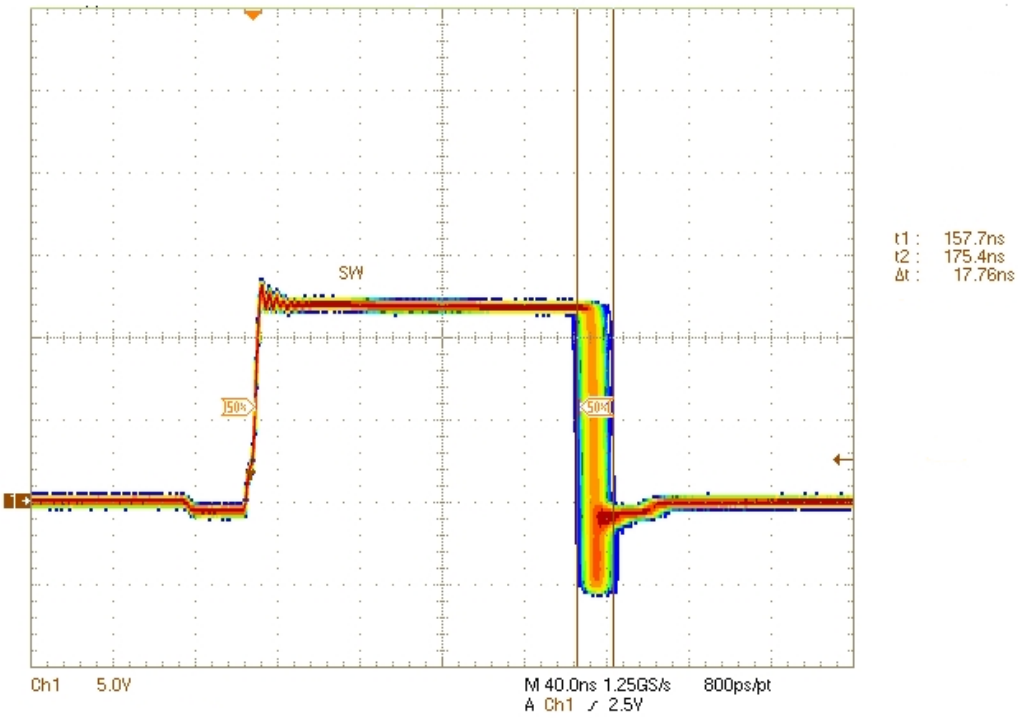


Fig. 3. Traditional solution. Vin =12 V and Vout =1.0 V/9 A at 600 kHz. The jitter measured is 17.6 ns.

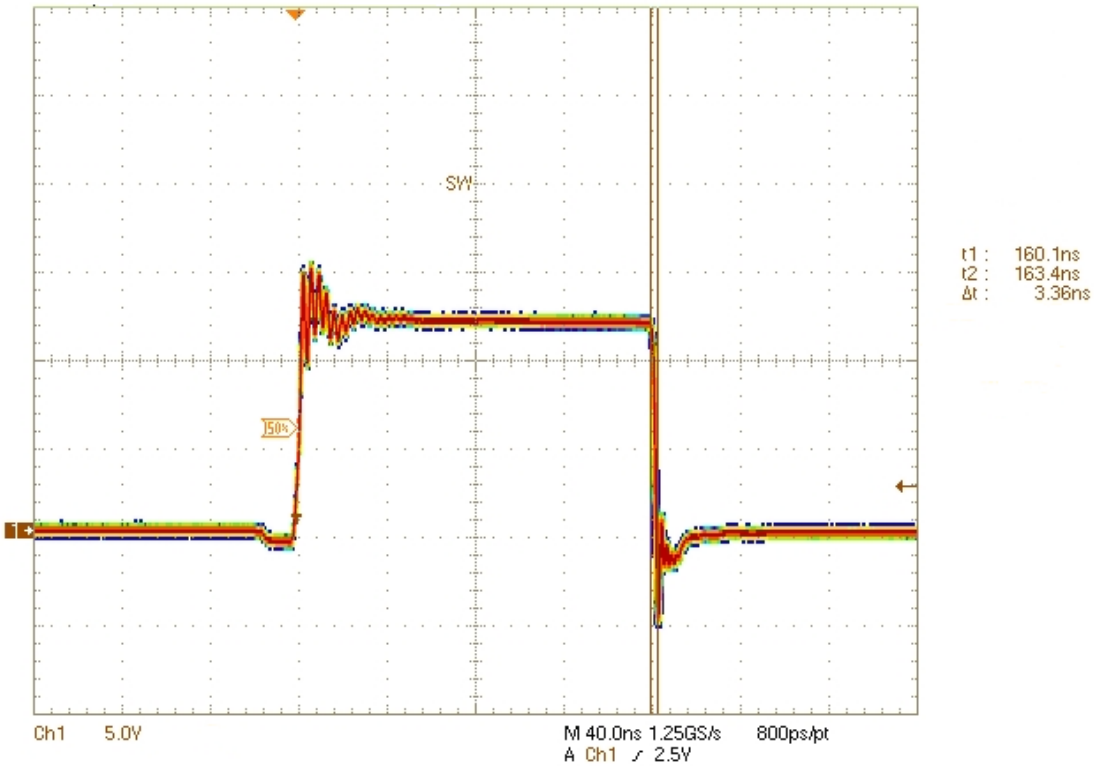


Fig. 4. New solution. Vin =12 V and Vout =1.0 V/9 A at 600 kHz. Jitter measured is 3.3 ns.

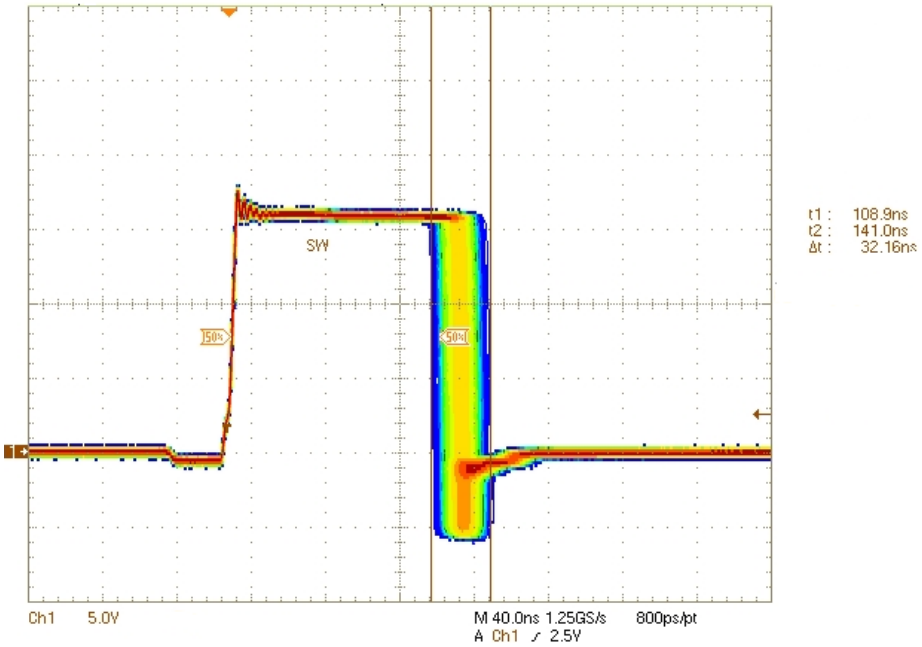


Fig. 5.Traditional solution. Vin = 16 V and Vout = 1.0 V/9 A at 600 kHz. Jitter measured is 32 ns.

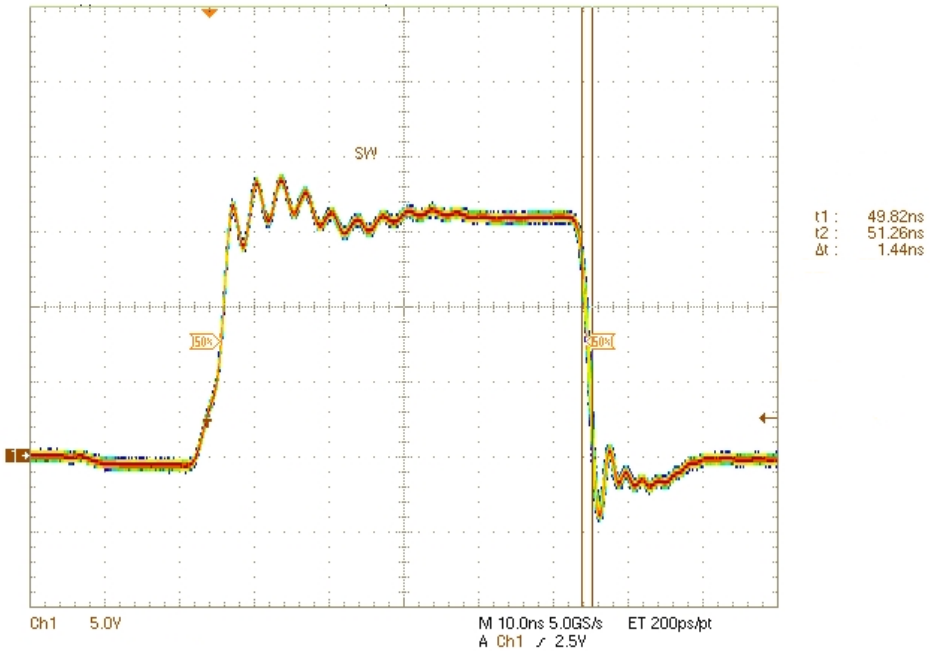


Fig. 6. New solution. Vin =16 V and Vout = 1.0 V/9 A at 1500 kHz. Jitter measured is 1.3 ns.

Another advantage of the new modulator scheme is that it guarantees a monotonic startup of the output voltage without any glitches and steps at the beginning (Fig. 7.) To get a startup waveform like this, first we need to get zero duty cycle, and then progressively increase the duty cycle until the output voltage ramps up to its final value. Since the new scheme is capable of generating very narrow pulse width close to zero, a clean start up is ensured. Since the reset signal can rise before the set signal falls, zero duty cycle can be generated without any dc offset in the ramp signal. Practically measured dc offset is only 150 mV in the new scheme and can operate with higher closed-loop bandwidth. So during startup, the Verror signal can take over the control of the duty cycle much earlier.

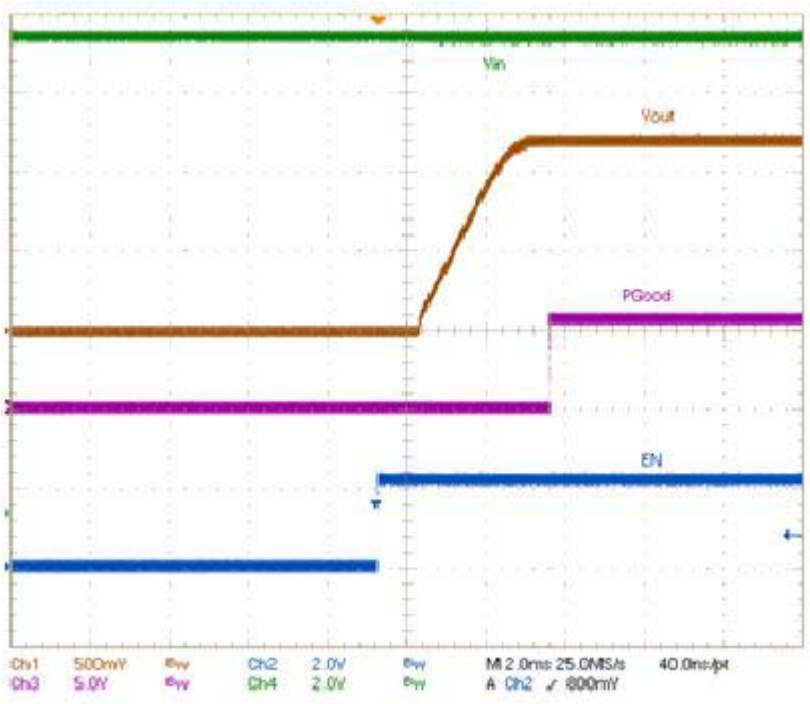


Fig. 7. Monotonic startup of output voltage for new solution. Vin = 12 V and Vout =1.2 V/9 A.

Next, consider the transient response improvement with the new scheme. This is achieved by operating at a higher switching frequency and higher closed-loop bandwidth. To demonstrate the effects of switching frequency and bandwidth on transient performance and capacitor requirements, a prototype buck converter is designed to operate at Vin =12 V and Vout = 1 V at a 1-MHz switching frequency. The inductor used is 0.33-µH surface-mount device (Vishay IHLP2525CZER0R33M01), and the output capacitor used is a 22-µF, X5R, 6.3 V, 0805 ceramic type (TDK C2012X5R0J226M).

In test case 1, six of the 22-µF capacitors have been installed on the prototype and the closed-loop bandwidth has been set at 90 kHz. In test case 2, the same number of capacitors are employed, but the bandwidth has been increased to 180 kHz. Finally, in test case 3, only three 22-µF capacitors are installed and bandwidth is set to 180 kHz.

From the waveforms Figs. 8a, 8b, and 8c, it can be concluded that for the same transient response, three output capacitors can be eliminated by running at a higher frequency and higher closed-loop bandwidth. This reduces the board size, which is another advantage of the new scheme.

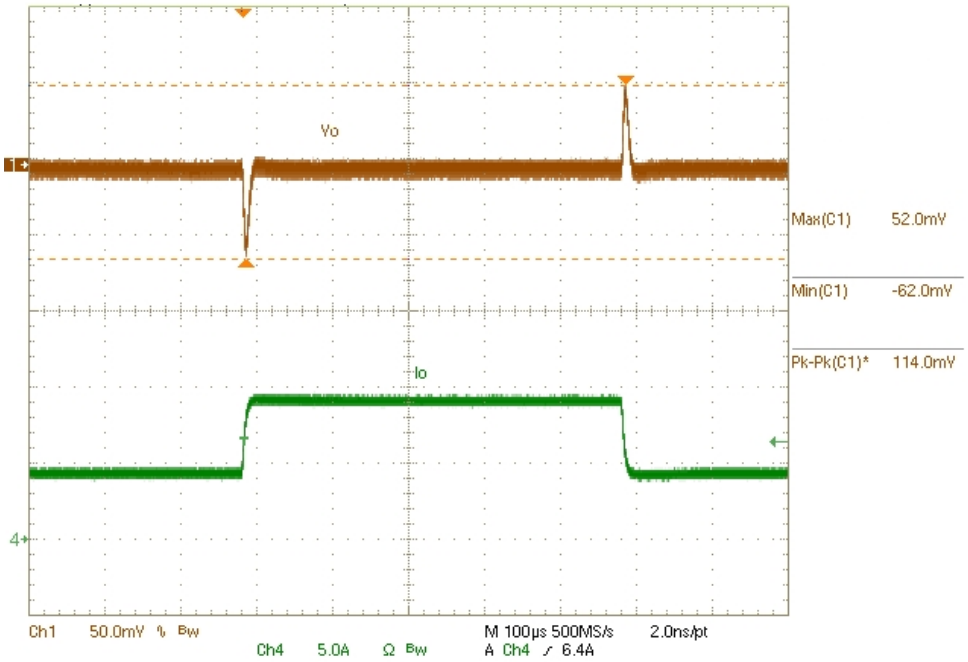


*Fig. 8a. Test case 1: Cout = 6 x 22 µF and bandwidth = 90 kHz. Vout pk-pk deviation measured on Ch1 is 114 mV. (Ch1 is set to 50 mV/div.)**

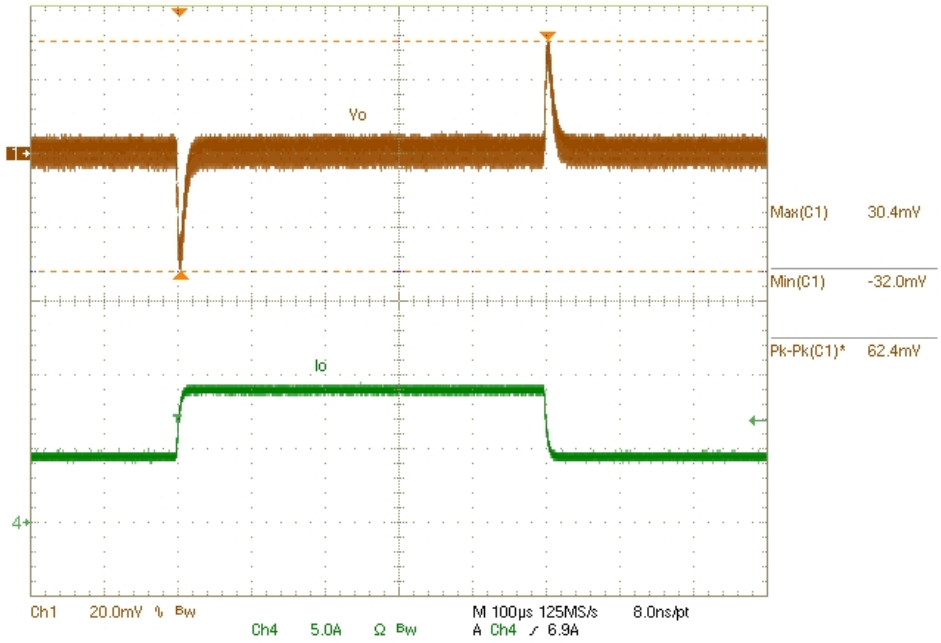


*Fig. 8b. Test case 2: Cout = 6 x 22 µF and bandwidth = 180 kHz. Vout pk-pk deviation measured on Ch1 is 62.4 mV. (Ch1 is set to 20 mV/div.)**

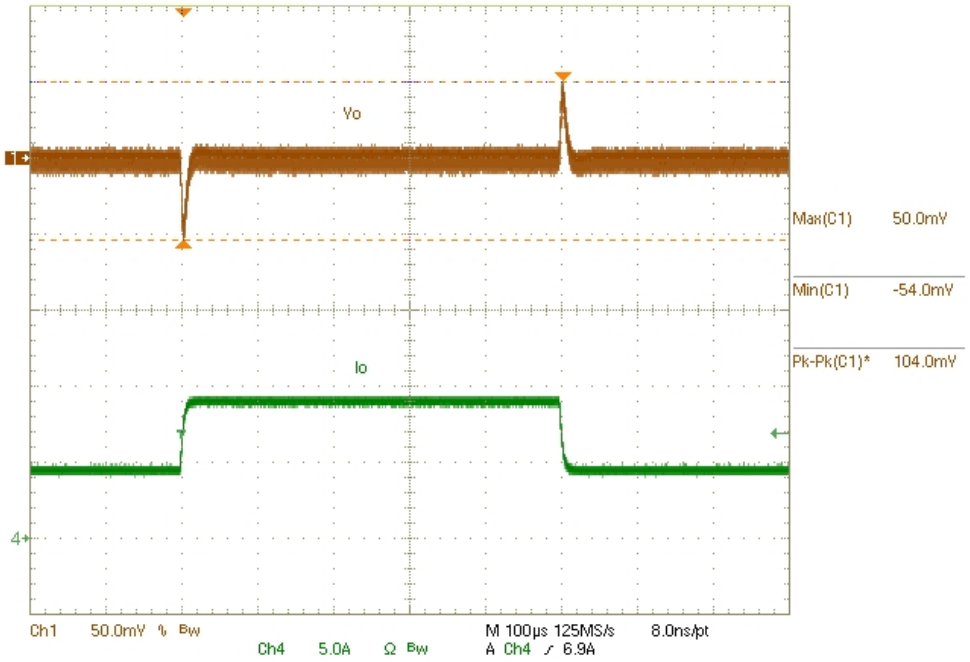


*Fig. 8c. Test case 3: Cout = 3 x 22 µF and bandwidth = 180 kHz. Vout pk-pk deviation measured on Ch1 is 104 mV. (Ch1 is set to 50 mV/div.)**

** Transient loading is at a 2.5-A/µs slew rate with Iout transitioning from 4.5 A to 9 A to 4.5 A as shown on Ch4. (Ch4 is set to 5 A/div.)*

Feed-forward (F.F.) is an important feature that can be integrated inside the voltage-mode controller IC because it can keep the converter stable and preserve its load-transient performance over a wide variation of the input voltage. The PWM ramp amplitude (Vramp) changes proportionally with respect to input voltage to maintain a constant ratio of Vin/Vramp as shown in Fig. 9. This will keep modulator gain constant for the input-voltage change, maintaining the control-loop bandwidth and phase margin constant. Feed-Forward function can also minimize output voltage deviation for a fast input-voltage change as shown in Fig. 10.

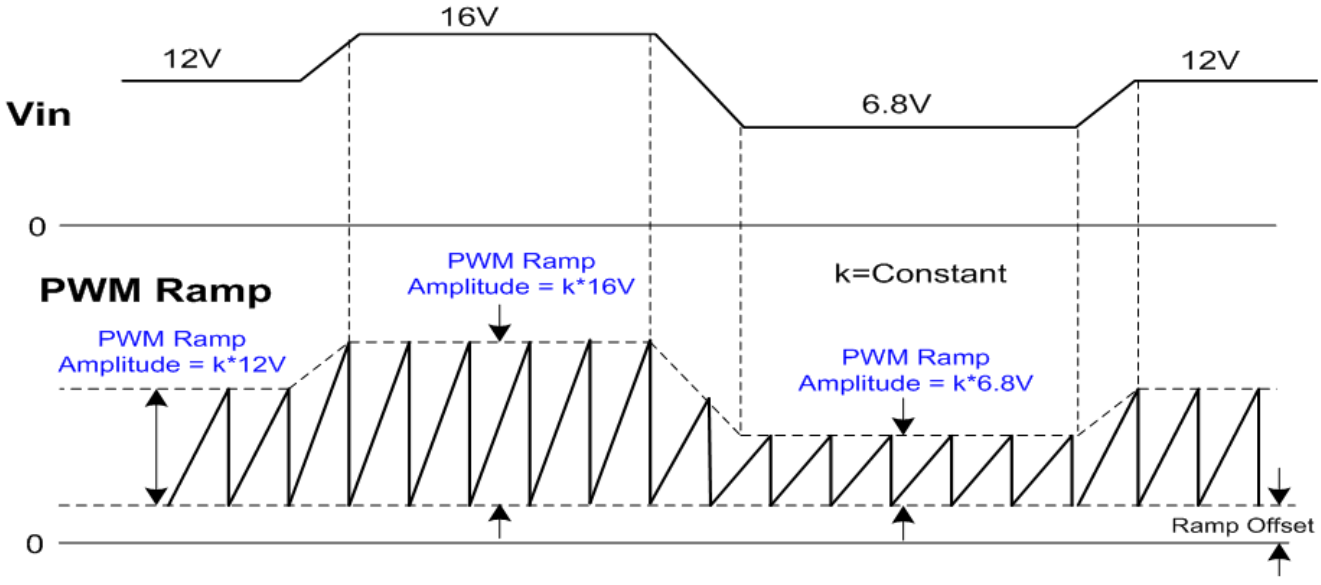


Fig. 9. Feed-Forward concept showing ramp amplitude variation relative to Vin .

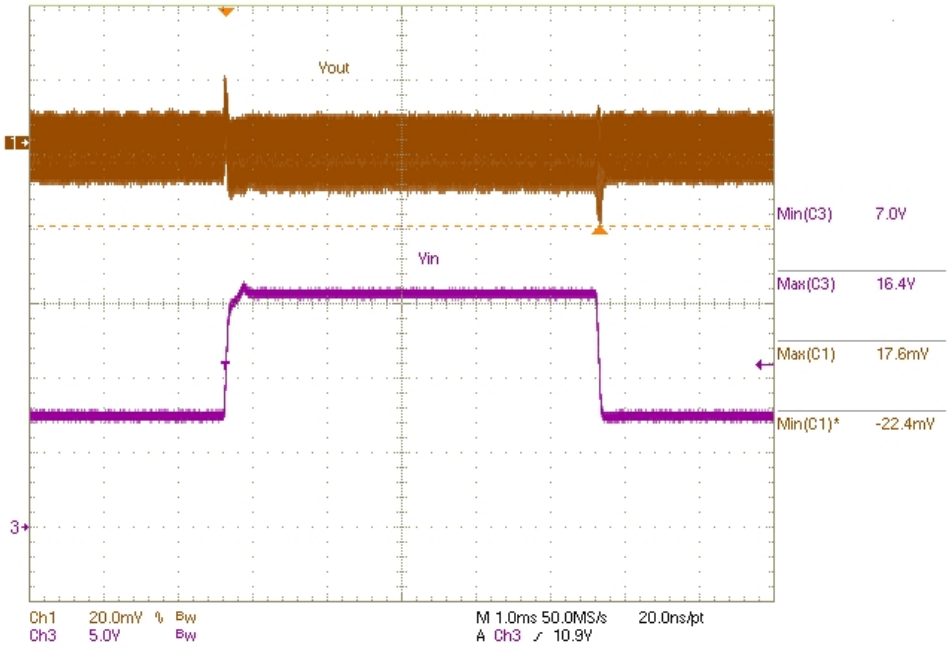


Fig. 10. Feed-forward waveform for Vin change. Vout variation as measured on Ch1 is <±25 mV. Vin is shown on Ch3.

Efficiency is an important aspect of a POL converter. A higher frequency can bring down solution size, but thermal management should be handled properly. For a given physical size, ambient temperature, and available air flow, there is a maximum limit on the dissipated power. In order to minimize the total dissipated power, efficiency has to be maximized by reducing losses.

MOSFET losses include conduction and switching losses. The gate-drive voltage can be optimized to minimize those losses. Driving the MOSFET gate at lower voltage during light-load conditions can reduce gate-drive losses. During medium- and heavy-load conditions, the MOSFETs can be driven using higher gate-drive voltage to improve conduction losses. This can be achieved by having a smart low dropout regulator (LDO) integrated on the controller chip.

The smart LDO can select its output voltage according to the load condition by sensing the switch-node voltage Vsw. Under light-load conditions when part of the inductor current flows in the reverse direction, the switch-node voltage is positive. If this case happens for a certain number of switching cycles, the smart LDO can reduce its output to a lower voltage level. If in any of those switching cycles, the switch node voltage is negative during the LDrv falling edge, the counter can be reset, and the LDO voltage will not be changed.

On the other hand, if Vsw < 0 on the LDrv falling edge, the LDO output is increased to a higher level immediately. A hysteresis band can be added to the Vsw comparison to avoid chattering. This is a smart way to improve efficiency across the full load range.

Fig. 11 shows the waveforms for a practical implementation of this scheme. LDO output is at 4.4 V under a light load condition, and it goes to 6.4 V when load current increases.

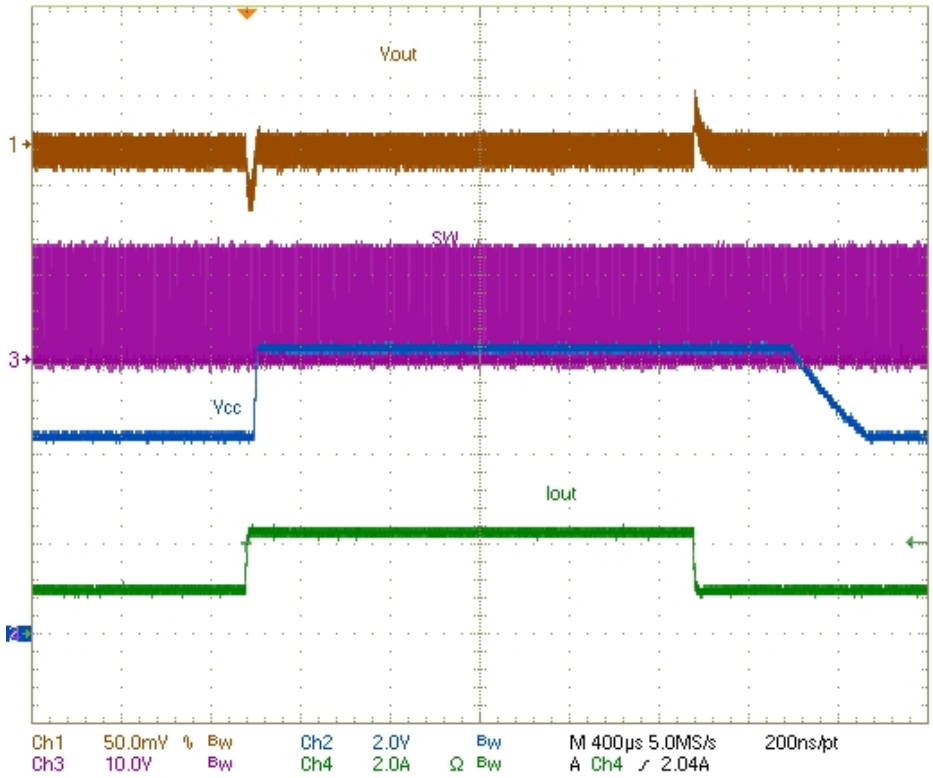
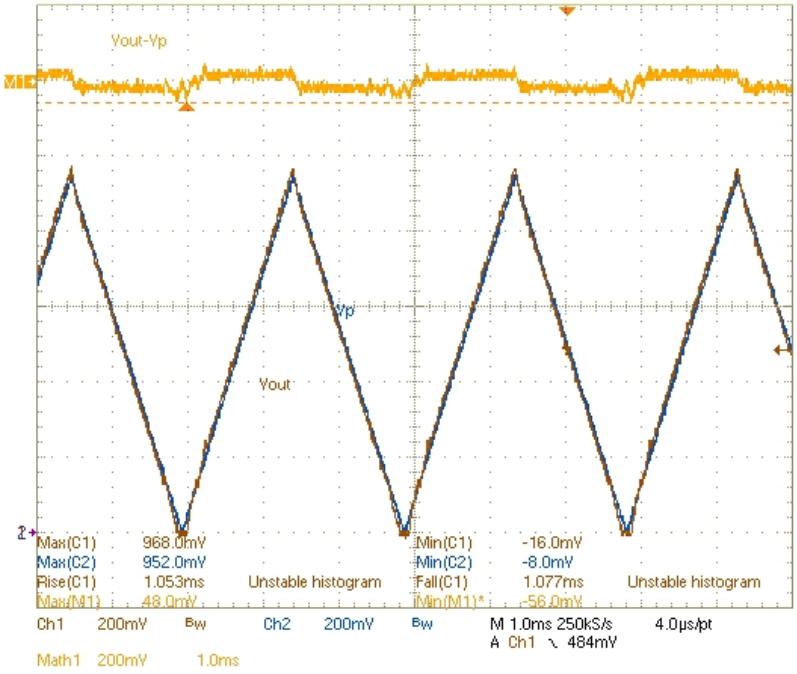


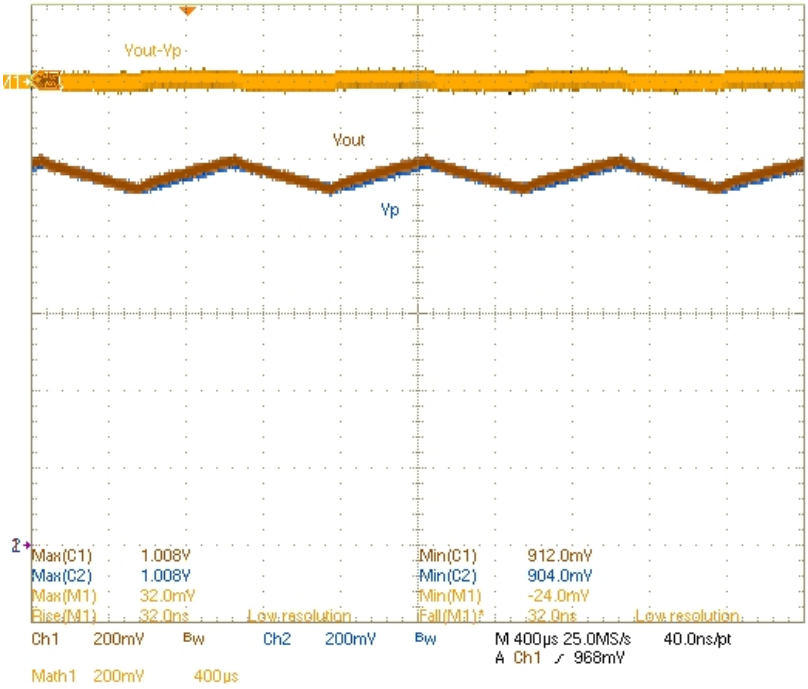
Fig. 11. Smart LDO output-voltage change when load current changes from 1 A to 2.3 A to 1 A. Ch1 = Vout, Ch2 = Vcc, Ch3 = SW Voltage and Ch4 = Iout. (Ch4 is set to 2 A/div.)

Another important feature of the regulator IC is its tracking capability. This can be implemented by having one more noninverting input to the error amplifier. The tracking feature is required for a Vtt memory power supply. It must also have current source and sink capability.

Fig. 12a shows start up and shutdown waveforms with 1-ms rise/fall time for the tracking voltage Vp. The Math waveform shows Vout-Vp, which is the tracking error. Fig. 12a shows Vout and VP track very close to each other. Fig. 12b shows a 100-mV variation of the Vp voltage to simulate tracking accuracy during a transient load condition.



(a)



(b)

Fig.12. Tracking mode operation. Ch1 = Vout, Ch2 = Vp, and Math1 = Vout-Vp.

Conclusion

The traditional voltage-mode controller can be modified to intersect the voltage error signal in a more linear region of the ramp signal, thereby reducing jitter and noise considerably. This allows operation of the PWM circuit at a higher frequency with narrow pulse width, which reduces the overall size of the solution. Higher operating frequency also allows higher closed-loop bandwidth and reduction of the number of output capacitors.

The new modulator scheme can produce zero duty cycle pulses due to the fact that the rising edge of the reset signal can be generated before the falling edge of the set signal. By integrating many additional features as

discussed above for the regulator IC, a full-featured POL converter can be realized using only a few external components saving board space and system cost.

About The Authors

Suresh Kariyadan joined International Rectifier in June 2009 as a senior staff engineer for POL Applications, Enterprise Power Business Unit (EPBU) where he is responsible for all point-of-load customer support for the EPBU. The role involves understanding customer's power supply requirements, providing reference designs, layout of PCBs, design verification tests, troubleshooting customer application boards and evaluating new product performance in application circuits. Prior to joining International Rectifier, Suresh held senior engineering positions with Maxim Integrated Products and Cherokee International. He holds a bachelors degree in Electronics and Telecommunication from Kerala University, India.

Parviz Parto is director of Systems Applications Engineering at International Rectifier where he is responsible for defining and developing power management products for point-of-load (POL) applications. Parviz has more than 15 years of design experience in power electronics. He received his M.S. from Chalmers University of Technology, Gothenburg, Sweden in electrical engineering. Parviz is author or coauthor of many technical papers and holds U.S patents in the area of power management. His interests include high-frequency switched-mode power supplies and ICs for power management applications.

For further reading on buck converter design, see the How2Power Design Guide, search the Popular Topics category and select the Buck Converters subcategory.