ISSUE: April 2012

How To Correct Voltage Imbalance In Half-Bridge Converters Under Current-Mode Control

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One popular topology used in today's power converter designs is the half-bridge topology (Fig. 1). A current-mode, half-bridge converter design has inherent issues that lead to oscillations. These issues are the result of slight imbalances in duty cycle and volt drops in the circuits, which cause the capacitors that terminate the primary winding to move slightly off the mid-point voltage into the converter. The current-mode control then leads to what can best be described as positive feedback to the current signal. This article examines the mechanism that leads to current imbalances in the primary winding in a half-bridge converter topology due to current-mode control, resulting in increased voltage imbalance. This article further explains how to overcome these imbalances while retaining current-signal integrity.

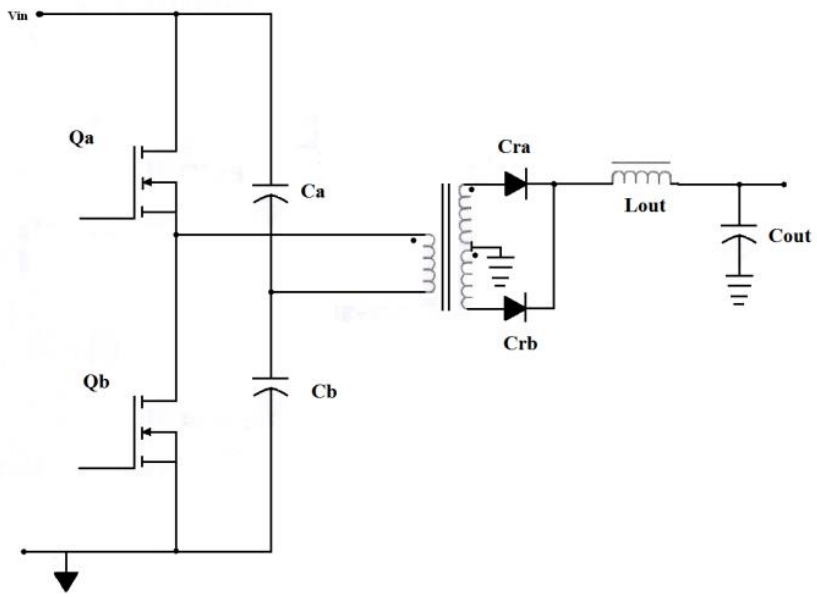


Fig. 1. Simplified half-bridge topology.

Understanding The Problem

The half-bridge topology restricts the voltage seen by the primary-side switches, Qa and Qb, to the peak line voltage. It allows the capacitors, Ca and Cb, to terminate the primary winding used for the primary-side bulk capacitor. This means that the RMS current for these devices must incorporate both these functions.

The design assumes that the capacitor junction voltage is half the input voltage. This means that the voltage across the primary is equal to half the input voltage, which impacts the turns ratio and the primary winding RMS input current.

When compared to a full-bridge converter topology, the voltage across the primary is half that of a full-bridge; while the primary winding current is twice that of a full-bridge current. It has the advantage of only requiring half the number of primary switches. With these exceptions the design is similar to a full-bridge.

One aspect, however, is different from a full-bridge. In current-mode control for a half-bridge without special attention to the current signal, the voltage at the junction of capacitors Ca and Cb tends to "walk", resulting in problems in the converter operation. To understand this we will examine the impact of a slight offset on the midpoint of the voltage. In the interests of KISS (keep it simple and sweet!) we will assume perfect components and zero voltages across switches and diodes.

First we examine the normal current waveform through the output inductor (Fig. 2.) Assume that the red portion of the waveform represents the current through the output inductor during the time that the Qa switch is on. Let's also assume that blue represents the time that the Qb switch is on.

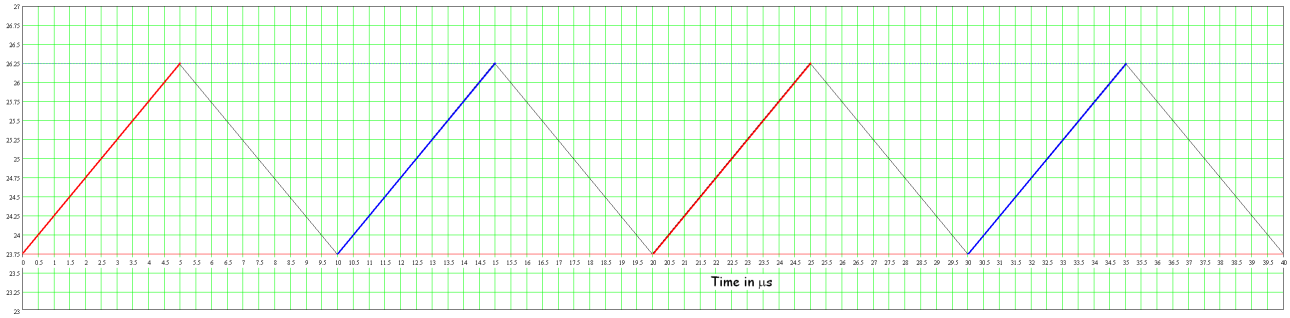


Fig. 2 Current waveform through the output inductor: red is the current while Qa is on; blue is the current while Qb is on.

For this analysis we use a Vin of 20 V and assume that the junction of Ca and Cb is at 10 V. The turns ratio of the transformer is 1:1:1 between the three windings. The output voltage is 5 V, and the output current is 25 A. The inductor Lout is chosen to have a ripple current under these conditions of 2.5 A total (or 10 percent). The transformer primary switching frequency is 50 kHz, or 10 µs maximum on-time for each of the switches. These requirements give a 50 percent duty cycle for the converter.

We assume that the transformer magnetizing inductance is extremely high compared to that of Lout. Also assume that the transformer has perfect coupling so that, during the time either Qa (red) or Qb (blue) is on, the current through the output inductor is equal to the current through the switch and the primary of the transformer.

As long as the duty cycles are equal and the midpoint of the capacitors is equal, then the resulting net current change over a cycle is zero. That is, the sum of the current through Qa (red) into the capacitors Ca and Cb is equal to the sum of the current out of the capacitors (blue) during the time Qb is on. This leaves the net voltage on Ca and Cb over a cycle equal to zero and, therefore, no net voltage change at the junction of Ca and Cb.

In practice, in half-bridge current-mode control, a current transformer is placed in series with the transformer's primary winding (Fig. 3.)

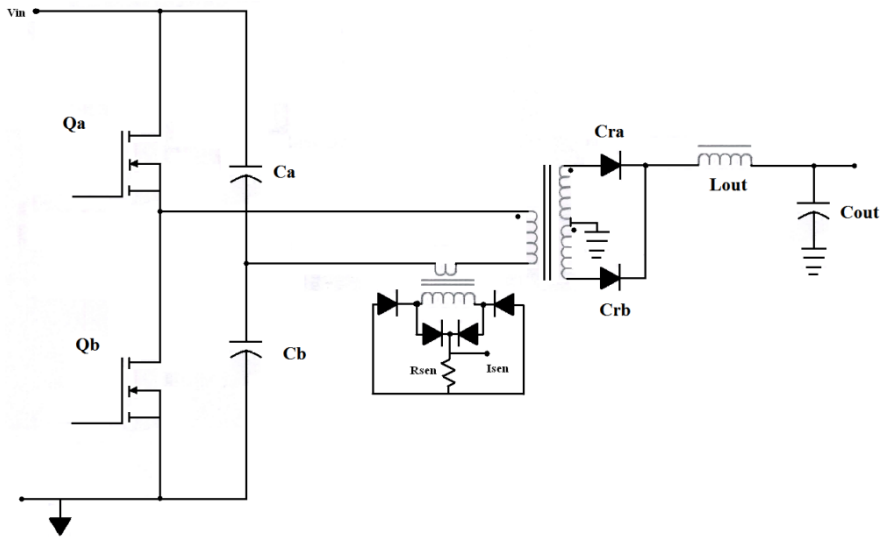


Fig. 3. Half-bridge converter showing current-sensing circuitry.

This transformer's associated diodes and resistor provides the current signal necessary for the control IC, for example the UCC2824, to provide the necessary pulse-width modulation (PWM) to control the output voltage. The output voltage is monitored by the control IC and it generates an error signal. Control is achieved by taking

the error signal and using that to set the point on the current signal where the switches turn off. Fig. 3 shows the half-bridge topology with the current transformer and associated monitoring diodes and resistors in place.

The conditions change as soon as the voltage on Ca and Cb are no longer equal. If the voltage on the Cb capacitor increases or Ca decreases so they are no longer equal and the junction is no longer at $V_{IN}/2$, the circuit enters a runaway condition that results in circuit failure.

To demonstrate this, we look at the impact of having our specific case, but have the voltage on the junction of Ca and Cb increase by 1 V. Then we look at the effect of this occurring just as Qa is turning on.

Assume that Ca and Cb are infinitely large, so for our demonstration there is no change in voltage on Ca and Cb. Also assume that the output voltage does not change over the course of this discussion.

Because the voltage at the capacitor junction is higher by 1 V, the voltage across the output inductor is lower while Qa is on. The di/dt across the output inductor decreases and takes longer to reach the current trip point. This results in more charge time for the output inductor to increase the current through the output inductor to the trip point.

Since it took longer for Qa to drive the current to the trip point, the available duty cycle before Qb turns on is less, and the residual current in the output inductor will be higher than in the balanced case. When the end of the cycle at 10 μs is reached and Qb turns on, the residual current in the output inductor is higher than in the balanced case because the Qa switch was on for a longer time. Hence, the output inductor did not have as long to discharge as in the balanced case (see Fig. 4 at 10 μs 24.37 A verses 23.75 A.)

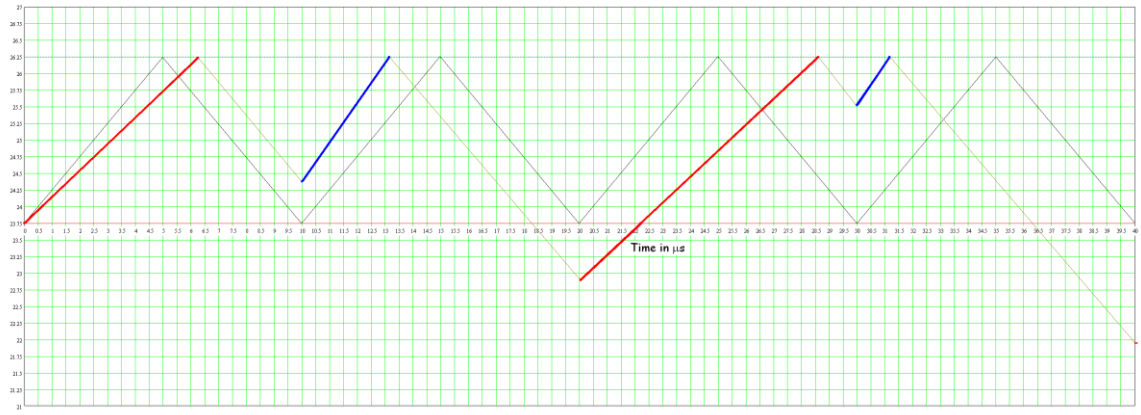


Fig. 4. This figure shows the current through the output inductor for two cycles. The red line represents the current through L_{OUT} when Qa is on, and the blue line represents the current through the output inductor when Qb is on.

Now when Qb turns on, the voltage across the primary is the voltage at the junction of Ca and Cb and is 1 V higher than previously. Therefore, the voltage across the primary is higher, and the slope of the current is higher than in the balanced case.

With the initial current being higher (24.37 A verses 23.75 A) and the di/dt higher than in the case where Qa is turned on, the resulting peak current is reached in a much shorter time. Fig. 4 shows that on the first cycle more charge is going into the capacitors than coming out. If Ca and Cb are not "infinite" capacitors, the junction voltage will be even higher at the end of the first cycle.

Now with the on time of Qb shorter, it leaves more time for the output inductor to be in a freewheeling state (the time when Qb has turned off but Qa has not turned on). The result is that by the time the period for the Qb pulse ends, the current in the output inductor is lower still than the previous cycle (22.9 A verses 23.75 A.)

The next cycle is even worse and, by the third cycle, Qa is on for the entire 10 μs and Qb is only on for an instant. Saturation of the transformer and oscillations are bound to follow.

Since the transformer is a one-to-one-to-one turns ratio, the current through each of the transistors can be represented as shown in Fig. 5.

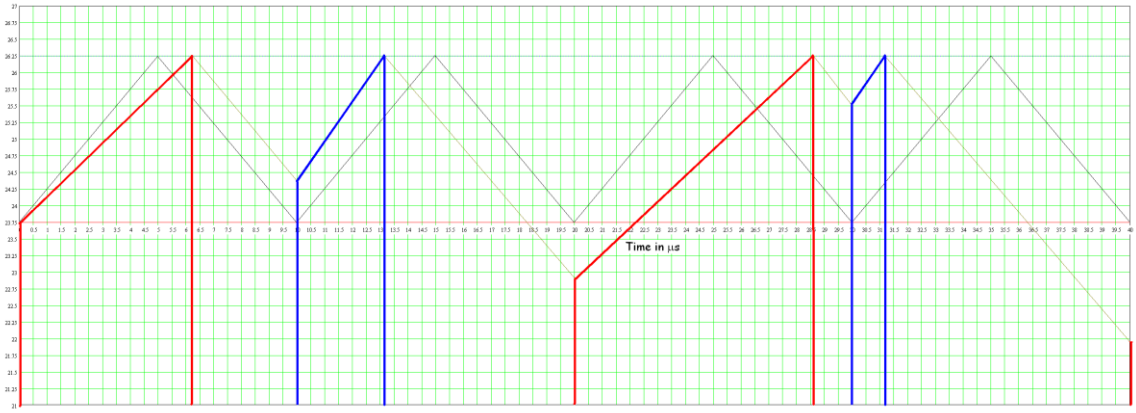


Fig. 5. The currents through the Qa transistor are much higher than current through Qb. This means that there is more net current going into the junction of Ca and Cb.

In a real circuit where Ca and Cb are not infinite, the net current flowing into the junction of Ca and Cb result in the voltage at the junction of Ca and Cb increasing even further and the converter failing even faster.

This demonstrates that even a slight imbalance in the currents result in a positive feedback type situation and unit failure.

Fixing The Problem

The accepted solution is to add an additional winding to both the power transformer and current transformer, and an additional two diodes (CrQa and CrQb). These additional diodes and windings only handle small currents. The schematic showing the new circuit is in Fig. 6.

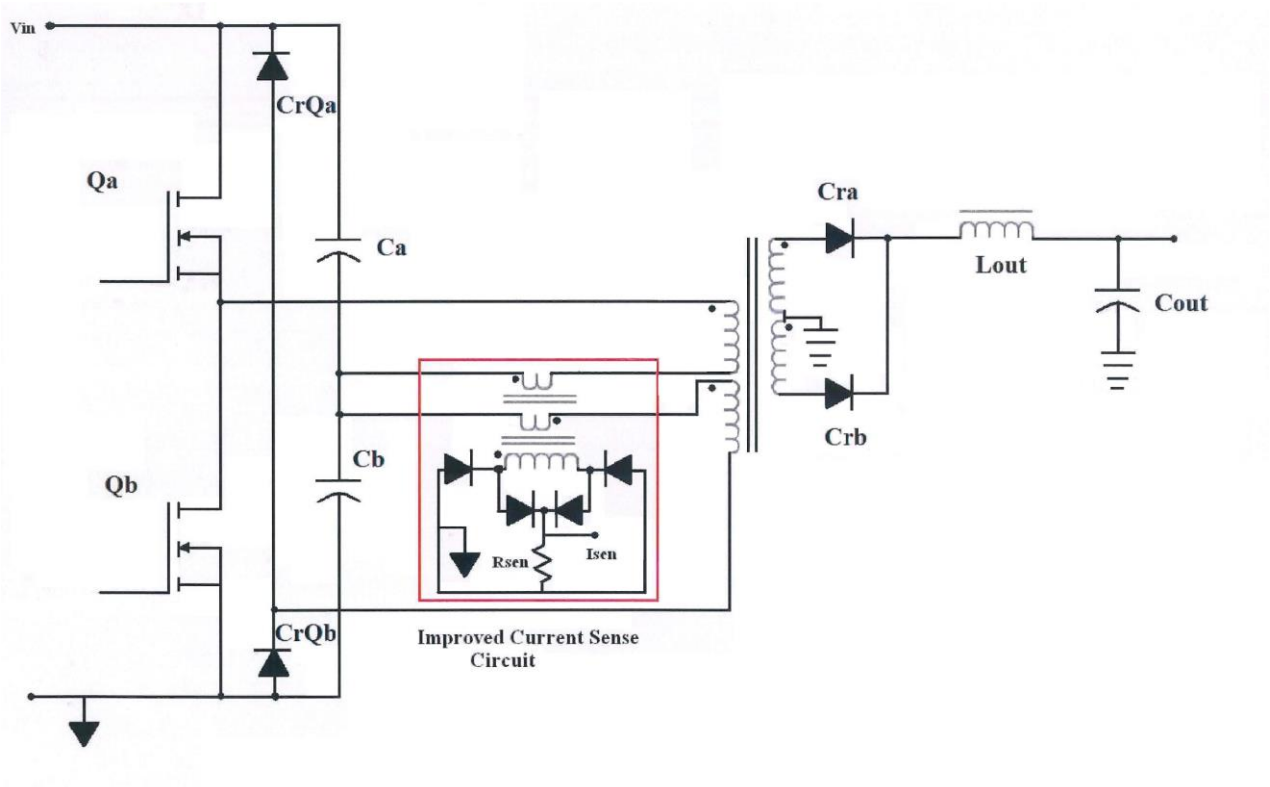


Fig. 6. Modification to the power transformer and current-sense transformer prevent the output capacitors from walking and circuit failure.

The winding on the power transformer is a finer gauge wire, but coupled to the primary. It has the same number of turns as the primary with the polarity as shown in Fig. 6. The current transformer has windings so

that any currents through the diodes CrQa and CrQb are subtracted from the current conducted by the transistors Qa and Qb.

To explain the operation of this circuit, assuming the same conditions as in the previous case, when Qa turns on, the voltage across the new power transformer winding is the same voltage. However, polarity drives the junction of the diodes CrQa and CrQb towards ground. But there is insufficient voltage to drive CrQb low enough to conduct.

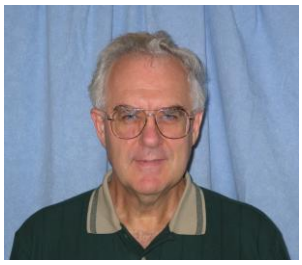
However, when Qb turns on, the voltage across the primary winding results in a voltage opposite in polarity from the voltage appearing across the new winding. This adds to the voltage on the junction of Ca and Cb, driving the voltage on the CrQa and CrQb junction above Vin by more than a diode drop. Now a current flows through the new winding out of the two capacitors to the source Vin, and a complementary current flows through the primary and Qb out of the capacitors to ground. Both currents act to reduce the voltage at the junction of Ca and Cb. Additionally, the current through the diode to the input voltage through the current transformer cancels the same magnitude of the current through the primary winding that flows through the current transformer.

This leaves the current signal from the current-sensing resistor equal to the difference in these two currents. This current is the signal that represents the output current of the power transformer.

In reality, the junction of the capacitors never gets that far out of balance as in this theoretical case. They are automatically adjusted on every cycle through the natural circuit operation, and the problem with the voltage on the capacitors in a half-bridge imbalance or "walking" is solved.

Reference

Andreycak, Bill. "Practical Considerations in Current Mode Control Power Supplies," Page 1-15, Texas Instruments, SEM500 1986.



About the Author

John Bottrill is a senior applications engineer at Texas Instruments, Manchester, New Hampshire. John supports customers and evaluates new ICs before release. In doing so, he has produced more than 20 technical papers and has two patents to his credit. He received his B. Sc. in Electrical Engineering from Queen's University at Kingston, Ontario, Canada. You can reach John at ti_johnbottrill@list.ti.com.