HOW2POWER TODAY
Your Power Design Newsletter

Special Report

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Workshop Underscores Importance of Power Supplies To Burn-in And Test of Latest Integrated Circuits

by Kevin Parmenter, Contributor, How2Power Today

I had the good fortune of attending the Burn-in and Test Strategies (BiTS) workshop that was held March 3-6 in Mesa, Arizona. At first glance, you might wonder what's the connection between a conference such as this and the power electronics field? The short answer is that power supplies play a critical role in the burn-in and test of both semiconductor and system-level products. This workshop gave me a greater appreciation of the importance of power supplies in burn-in and test applications as well as the issues that are driving development of these power supplies.

First, power supply development is driven by the need for clean, reliable power. This is a requirement of both the companies that build burn-in and test equipment and their customers (i.e. the equipment users.) This requirement is driven largely by integrated circuit (IC) developments.

Some of the latest ICs, especially the mixed-signal and analog ICs are pushing the state of the art when it comes to reliability and performance. Moreover the VLSI and memory devices continue to have VCC levels that are dropping, while at the same time imposing tighter tolerances on supply regulation, accuracy and precision.

In listening to the talks, the need for reliable interconnects and test systems was a message that came across loud and clear. The power electronics within these test systems must be able to keep up with the needs for reliability, low voltage drop and overall signal integrity.

Why are these needs so important? A burn-in test may cost millions of dollars to set up, collect data and run to completion. If a power supply failure occurs during the test, the parts will have to be scrapped and the test restarted. As if these costs are not enough, there will be further cost penalties stemming from any associated delays in product release and time to market.

Clearly, the stakes are high for power supplies used in burn-in and test, particularly in the semiconductor industry. But this was not my only takeaway from the BiTS workshop. It also gave me some perspective on trends in the semiconductor industry, which ultimately reverberate in the power supply world.

For example, in the BiTS keynote speech, Bill McClean, president of IC Insights, described how the semiconductor industry is tied to the global economy. In his talk, "The Dramatic Restructuring of the Integrated Circuit Industry," McClean noted that throughout 2012, the expectations for global economic growth consistently deteriorated and global GDP expanded by only 2.6%. It's worth mentioning that 2.5% or less worldwide GDP growth is typically considered a global recession.

However, as McClean pointed out, IC Insights' forecast for worldwide GDP growth in 2013 is 3.2%, with the expectation of increasingly higher growth for the global economy through 2016. So today, the IC industry is poised to emerge from a difficult five-year period of minimal growth. From 2007-2012, the IC market grew at an average annual rate of just 2.0%. According to IC Insights' analysis, the "bottom" of the current cycle in the worldwide economy and IC industry was reached in 2012 and 2013 will mark the beginning of the next cyclical upturn. IC Insights predicts that the CAGR of the IC industry will more than triple to 7.4% over the next five years.

Overall, semiconductor industry cycles are becoming increasingly tied to the health of the worldwide economy. While poor semiconductor industry growth has occurred during periods of strong worldwide economic growth, primarily due to semiconductor industry overcapacity and the resulting IC price declines, it is rare to have strong semiconductor industry growth without at least a "good" worldwide economy to support it. Thus, over the next five years, annual global semiconductor market growth rates are expected to gain significant momentum and closely mirror the performance of worldwide GDP growth.

Following the keynote speech, the workshop proceeded with the presentation of the individual papers and discussions in the various sessions, all of which were informative and topical. To give you a further sense of the technical issues addressed at the workshop, the titles of the various talks and their presenters are listed below.

In summary, the conference highlighted the importance of test and burn-in along with interconnect signal integrity and power supply quality. The latter issue encompasses power supply reliability and low-noise performance, both conducted and radiated. All of these issues affecting signal and power integrity must be carefully addressed to successfully implement high-performance burn-in and test.

Don't miss next year's BiTS workshop (BiTS 2014), which returns to Mesa, Arizona. Visit the workshop website to keep track of news about the conference and to sign up for next year's event.

SESSION 1

Kiva Ballroom

STREAMLINING OPERATIONS

Improving Socket Alignment Performance Using Monte Carlo Analysis Techniques and Manufacturing Controls
Daniel DelVecchio, Dustin Allison—Interconnect Devices Incorporated

Tooling Stack-up Process Margin Improvement
Mook Koon Wong, Boon Hor Phee—Intel Malaysia

Zero Cost Virtual Tool Checker
Seong Guan Ooi—Intel Technology Sdn. Bhd.

Enablers for Robust & Fast Online Trouble-shooting for High Parallelism Testing
Benedict Loh—Infineon Technologies
Kohei Hironaka—NHK Spring Co. Ltd.
Michelle Ng—TestPro

TALKING POINTS

Interconnectology: Inspiring a Paradigm Shift
Host:
Françoise von Trapp—Queen of 3D, Founder of 3D InCites

Special Guests:
Scott Jewler—Senior VP, Advanced Nanotechnology Solutions, Inc.
Simon McElrea—President, Invesas Corp.
Tim Olson—President & CEO, Deca Technologies
Ira Feldman—President & CEO, Feldman Engineering Corp.

POSTER SESSION

Kiva Foye

CSH Coating for High Temperature
Ichiro Fujishiro—Yamaichi Electronics

Top Side Probing on Handler
Shaul Lupo—Intel Israel

"Auto-Centering Manual Actuator" — One Manual Lid for Different Package Sizes Testing
Ying Hoe Mah, Shamal Mundiyath—JF Technology Berhad

Novel Approach Of Enabling Customer Shadow EPROM aka "EXTERNAL-EPROM" In HVM Environment
Maroon Maroon, Mouller Keren—Intel Corporation

SESSION 2 *Kiva Ballroom*

TEST TOOLING MADE EASY

3D Package Handling: A Simple Case of Integrating Complex Technologies
Zain Abadin—Advantest America, Inc.

Innovative Way to Prevent Semiconductor Test Tester Coolant Leakage with Hazardous Warning System
Yee Wei Tiang—Intel (Malaysia)

Die-Cracking Failure Analysis of QFN Packages in Manual Test Handler
M.P. Divakar, PhD—Stack Design Automation

Cost Saving Through Homogenous Spring Loaded Pin Tip Implementation in High Volume Manufacturing (HVM) Environment
Chin Siang (David) Chew, Nithya Nandhan Subramaniam—Intel Technology
Chin Chien Tee—Interconnect Devices, Inc.

SESSION 3 *Kiva Ballroc*

AWARD WINNING PERFORMANCE

Design of Experiments Using Spring Probe Parameters for Optimized Socket Bandwidth
Mike Fedde, Ila Pal—Ironwood Electronics, Inc.

Socket Performance vs. Environmental Conditions
Gert Hohenwarter—GateWave Northern, Inc.

Troubleshooting Test Oscillation Problems
Jeff Sherry—Johnstech International Corporation

Optimization of Package, Socket and PC Board for 25 to 40GHz RF Devices
Carol McCuen, Phil Warwick—R&D Circuits, Inc.

SESSION 4

BRING IT TO THE BOARD (PCB)

Building Optimized Test PCB's Starts at the DUT
Joe Birtola—CMR Summit Technologies

High Frequency PCB Material Characterization and Simulation
Ryan Satrom—Multitest

SESSION 5

BETTER BY DESIGN

A Novel Nested Doll Concept in Universal Kit for Test Handler
Yee Wei Tiang—Intel (Malaysia)

Anatomy of a Socket
Paul F. Ruo—Aries Electronics, Inc.

Special Designs and Applications for PoP Device Testing
Siang Soh, Frank Zhou, Jon Diller, James Spooner, Khaled Elmadbouly
—Interconnect Devices, Inc.

SESSION 6

AND, AT THE WAFER LEVEL

Spring Probes and Probe Cards for Wafer-Level Test
Jim Brandes—Multitest

A Comparison of Probe Solutions for an RF WLCSP Product
James Migliaccio—RF Micro Devices

Bridging Between 3D and 3D TSV Stacking Technologies
Belgacem Haba, Ph.D.—Invensas

Wafer-Level Burn-in Decision Factors
Steve Steps—Aehr Test Systems

SESSION 7

PRODUCT AND MATERIAL MÉLANGE

High Temperature Burn-in (Up to 200° C): Are We Ready Yet?
Noriyuki Matsuoka, Kazumi Uratsuji —Yamaichi Electronics Co., Ltd.
Jec Sangalang—Yamaichi Electronics USA
Ryota Takeuchi—NGK Insulators, Ltd.

Development of High Performance Spring Probe Pin and Elastomer Contact by Stamping
Samuel Pak, A.J. Park—IWIN Co. Ltd.

ESD Safe Materials for Test Socket and Encapsulation
Tatsuya Kawasaki—Krefine Co., Ltd.

About The Author

Kevin Parmenter has over 20 years of experience in the electronics and semiconductor industry. Kevin is currently vice president of applications engineering in the USA for Excelsys Technologies. Previously, Kevin has served as director of Advanced Technical Marketing for Digital Power Products at Exar, and led global product applications engineering and new product definition for Freescale Semiconductors AMPD - Analog, Mixed Signal and Power Division based in Tempe, AZ.

Prior to that, he worked for Fairchild Semiconductor in the Americas as senior director of field applications engineering and held various technical and management positions with increasing responsibility at ON Semiconductor and in the Motorola Semiconductor Products Sector. Kevin also led an applications engineering team for the start-up Primarion where he worked on high-speed electro-optical communications and digital power supply semiconductors.

Kevin serves on the board of directors of the PSMA (Power Sources Manufacturers Association) and was the general chair of APEC 2009 (the IEEE Applied Power Electronics Conference.) Kevin has also had design engineering experience in the medical electronics and military electronics fields. He holds a BSEE and BS in Business Administration, is a member of the IEEE, and holds an Amateur Extra class FCC license (call sign KG5Q) as well as an FCC Commercial Radiotelephone License.