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The Small-Signal Model Of An Active-Clamp Forward Converter (Part 1): Basics Of The Forward Converter And Its Transfer Function

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The forward converter is a popular topology found in ac-dc and dc-dc power supplies where low voltage and high output current are required. Typical examples are converters found in so-called ATX silver boxes where 5-V and 3.3-V outputs can deliver tens of amps.

In these applications, an active pre-converter shapes the input power factor but also regulates a high-voltage dc rail. The latter action is particularly necessary because the forward converter does not cope very well with wide input ranges given its limited duty-ratio dynamics—below 50% most of the time. If you want to shrink magnetics, for more compact converters, increasing the switching frequency in the forward converter is not an option given the losses incurred during the hard switching of the primary-side power switch.

Introduced more than 20 years ago, the active-clamp architecture elegantly solves these issues by sizing the magnetizing current to force a discharging of the drain-source parasitic capacitance prior to turn-on of the power switch. Among other benefits, such as a widened range of duty ratio and self-driven synchronous rectification, the active-clamp architecture makes possible zero-voltage switching (ZVS), which in turn enables an increase in switching frequency and the associated shrinking of magnetic components.

As with any dc-dc converter, you need to obtain the power stage's small-signal response before attempting to stabilize the loop. The purpose of this articles series is to show how to build a small-signal model of the active-clamp forward converter operating in voltage mode and derive its ac transfer function. We will open this series with the study of the classical single-switch forward converter and see how we can obtain its transfer function.

The Forward Converter

A simplified schematic for a forward converter appears in Fig. 1. It is a classical buck converter associated with an isolation transformer, hence its classification as *buck-derived* converter.

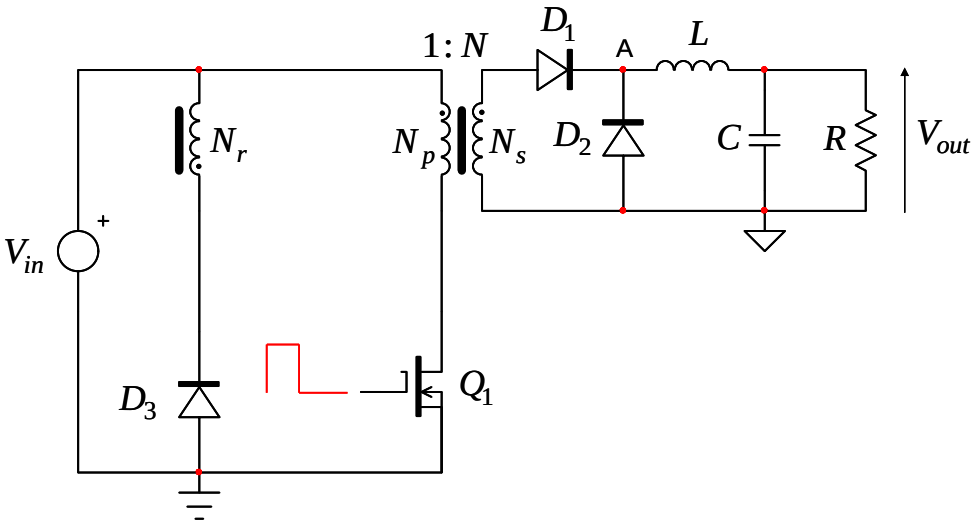

Fig. 1. A forward converter requires a means of demagnetizing its transformer, a function usually performed by a tertiary winding, labelled here as N_r.

In a buck converter, a power switch chops the input voltage V_{in} to one of the inductor terminals while the other terminal connects to the dc output voltage V_{out}. In the forward architecture, V_{out} is still connected to one of the inductor terminals but the other one receives the pulsating input voltage scaled by the transformer turns ratio via a series diode, D_1. This is point A in Fig. 1. Simply put, the square-wave signal available at that point is further filtered out by the *LC* network to deliver a clean dc signal V_{out} equal to the point A average voltage.

In this converter, the input voltage is interrupted by power transistor Q_1, which is turned on and off at a pace imposed by the pulse width modulation (PWM) controller. When the controller instructs this device to turn on, a current i_D flows in the MOSFET drain as shown in Fig. 2. This current is made up of the reflected inductor current $i_L(t)$ plus the magnetizing current $i_{mag}(t)$. It circulates during the on-time t_{on}:

$$i_D(t) = i_{mag}(t) + Ni_L(t)\,. \tag{1}$$

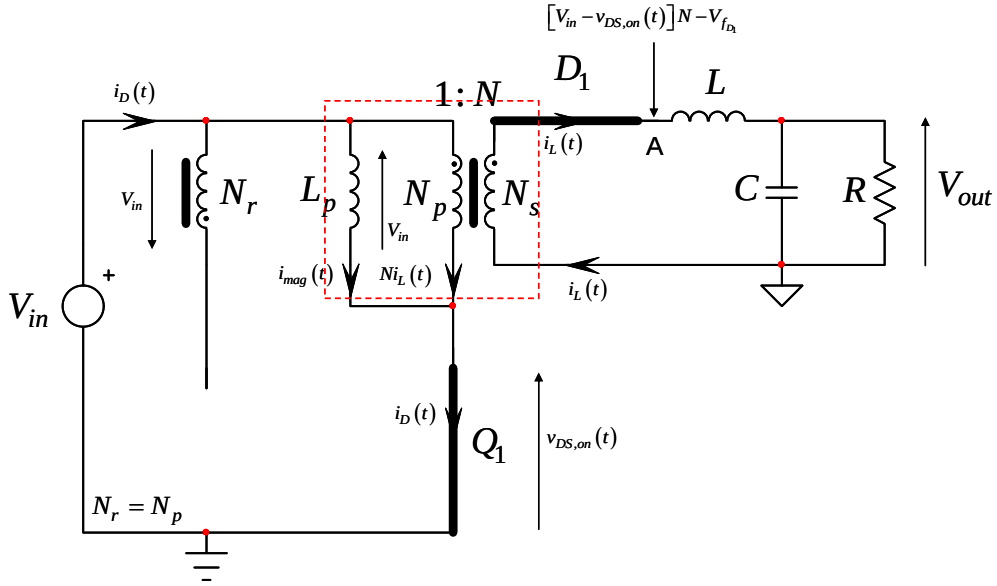

Fig.2. During the on-time, Q_1 conducts while D_1 is forward biased (D_2 and D_3 are blocked).

As MOSFET Q_1 offers a resistive path between its drain-source terminals, it creates a voltage drop as shown in Fig. 2. This drop equals:

$$v_{DS,on}(t) = r_{DS(on)} i_D(t)\,. \tag{2}$$

This drop subtracts from the input voltage applied to the transformer primary v_p:

$$v_p(t) = V_{in} - v_{DS,on}(t)\,. \tag{3}$$

While a voltage is applied across the primary side of the transformer, the magnetizing current i_{mag} grows with a slope depending on the primary inductance L_{mag}. Neglecting the MOSFET drop, we have:

$$S_{mag} \approx \frac{V_{in}}{L_{mag}}\,. \tag{4}$$

The transformer scales down the primary voltage by its turns ratio $N = N_s/N_p$. On the cathode of series diode D_1, you have

$$v_A(t) = v_p(t)N - v_{f_{D_1}}(t) = \left[V_{in} - r_{DS(on)} i_D(t)\right]N - V_{f_{D_1}} \tag{5}$$

in which $V_{f_{D_1}}$ is the diode forward voltage drop that we consider constant at the given output current. Please note that during the on-time, given the reset winding polarity N_r, diode D_3 is blocked.

On the secondary side, the current in the output inductor *L* grows with a slope given by the voltage applied across its terminals. This voltage is $V_A - V_{out}$, imposing an on-slope obeying:

$$S_{L,on} = \frac{V_A - V_{out}}{L} = \frac{\left(\left[V_{in} - r_{DS(on)} i_D(t)\right] N - V_{f_{D_1}}\right) - V_{out}}{L} \approx \frac{NV_{in} - \left(V_{out} + V_{f_{D_1}}\right)}{L}. \quad (6)$$

This inductive current also circulates in the network made of the output capacitor and the load. The inductor average current is actually the output dc current absorbed by the load while ac ripple flows in the capacitor.

When the PWM circuit gives the corresponding signal, Q_1 blocks and opens the primary mesh as shown in Fig. 3. At the switch opening, the primary current no longer flows through Q_1 and finds a path through the parasitic drain-source capacitor C_{lump}: the voltage on the drain rises up with a slope given by:

$$S_D = \frac{I_{peak}}{C_{lump}} [\text{V/S}] \quad (7)$$

where I_{peak} is the current at the switch turn-off event and S_D is expressed in V/s. The equivalent current generator charging C_{lump} is made of the magnetizing current i_{mag} plus the reflected output inductance current Ni_L.

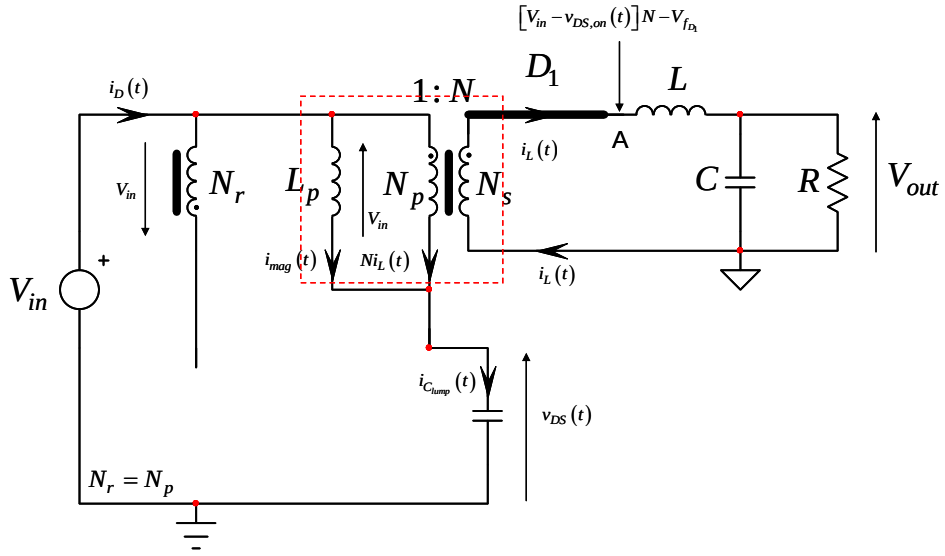

Fig. 3. Immediately at the switch opening, the drain current finds its way through the parasitic drain-source capacitance: $v_{DS}(t)$ quickly increases at a pace determined by equation 7.

When the drain voltage reaches V_{in}, the voltage across the primary inductance goes to zero (Fig. 4.) Diode D_1 starts to block since its anode voltage is zero and the current reflection on the primary side Ni_L stops. The current circulating in D_1 commences its transfer to freewheeling diode D_2. Both components conduct together for a short time: this is the so-called overlap period. It will re-appear when the primary-side power MOSFET switches back on again, forcing D_2 to fully block and D_1 to conduct. During this short period of time as both secondary-side diodes conduct, the primary-side magnetizing current pauses since the primary voltage is 0 V.

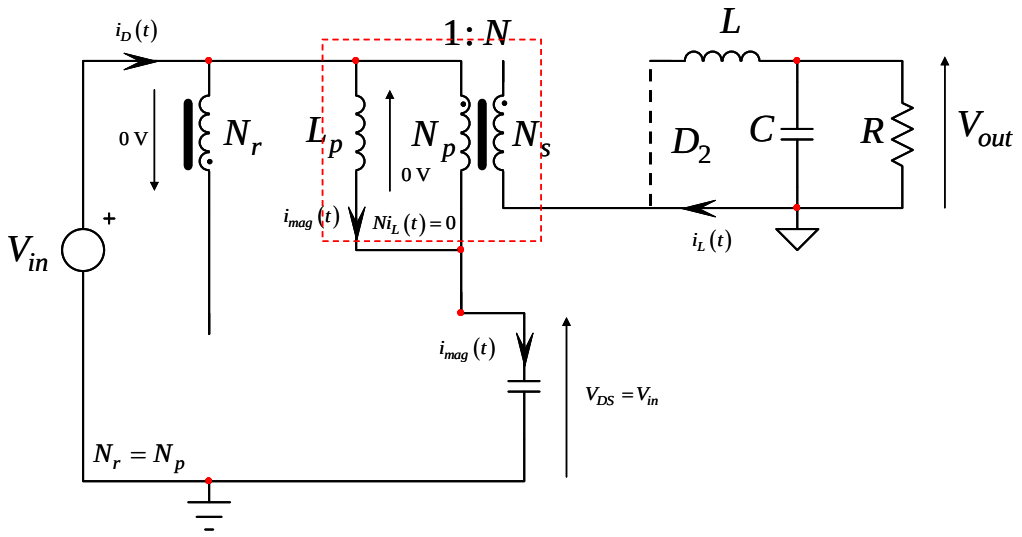

Fig. 4. When the drain voltage reaches V_{in}, the secondary diode D_1 blocks and freewheeling diode D_2 starts to conduct. $v_{DS}(t)$ keeps increasing, reversing the voltage across the primary side.

The C_{lump} voltage continues to increase due to the magnetizing current alone: the voltage across the transformer primary reverses and a negative voltage builds across N_r. As N_r and N_p are coupled—usually by a 1:1 turns ratio in a "flyback" way—when this negative voltage reaches the input voltage V_{in}, diode D_3 conducts. A low-impedance voltage clamps the drain-voltage excursion. This excursion is actually equal to the input voltage source in series with the tertiary winding also imposing V_{in} since D_3 conducts. The drain is thus clamped to twice V_{in} as depicted in Fig. 5.

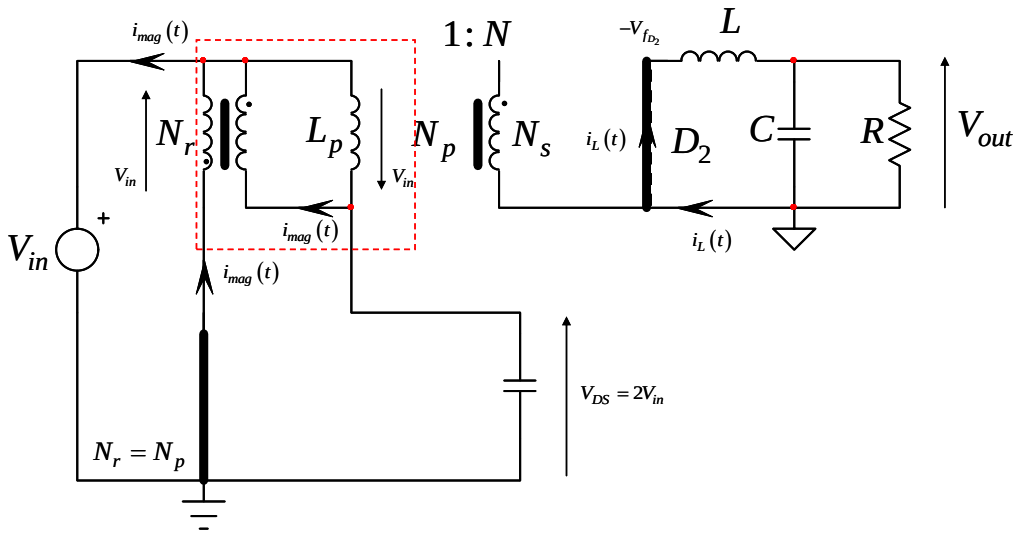

Fig. 5. D3 now conducts and imposes –Vin across the primary inductance, forcing the magnetizing current to decrease. D2 is fully conducting.

As D_2 now conducts, point A drops to a negative voltage caused by the forward drop of the free-wheeling diode:

$$V_A = -V_{f_{D_2}} . \tag{8}$$

The inductor current is falling with a slope imposed by the output voltage V_{out}:

$$S_{L,off} = \frac{-\left(V_{f_{D_2}} + V_{out}\right)}{L} . \tag{9}$$

Because the drain rises to twice V_{in}, the voltage applied across the primary side of the transformer is $-V_{in}$, forcing the magnetizing current to decrease with a new slope equal to:

$$S_{mag}(t) = -\frac{V_{in}}{L_{mag}} . \tag{10}$$

As indicated in Fig. 5, the energy stored in the magnetizing inductance returns to the source, improving the converter efficiency. When the magnetizing current eventually reaches 0 A, after a so-called demagnetization period t_{dem}, diode D_3 blocks and the circuit in Fig. 5 updates to Fig. 6.

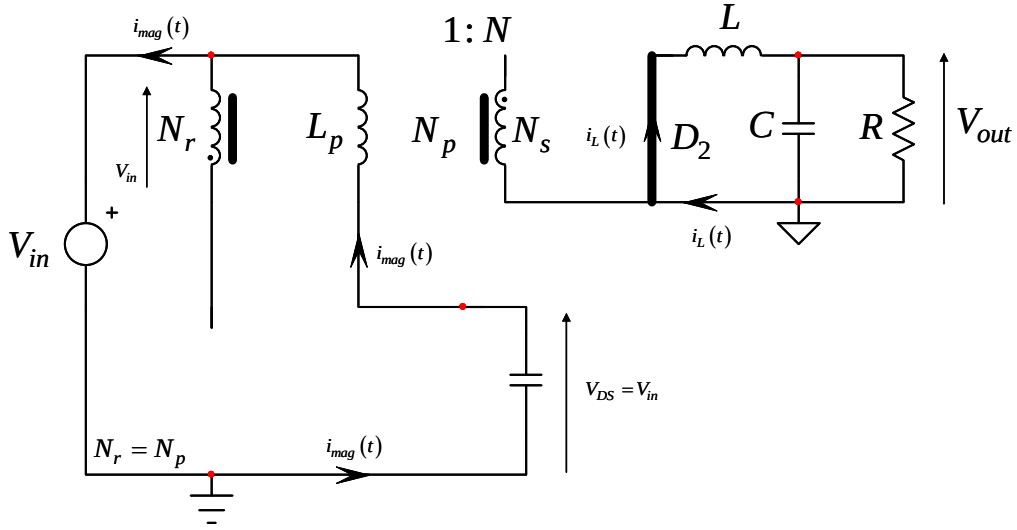

Fig. 6. The transformer is now reset and all primary-side semiconductors are blocked.

D_3 being blocked, we are left with a capacitor charged to $2V_{in}$ while the magnetizing inductor is no longer energized. This resonating network natural response (no excitation, only initial conditions are considered) is a sinusoidal waveform of the following frequency:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{mag}C_{lump}}} . \tag{11}$$

The resonating current circulates backwards through the source and discharges the lump capacitor: $v_{DS}(t)$ goes down towards V_{in}. At this point, the drain would like to dip further down, but as you start to build a positive voltage across the transformer primary side, D_1 activates. However, as D_2 is still conducting, the primary sees a short circuit, so the drain cannot drop further down and is stuck at V_{in}.

After a dead-time period, when the controller turns the power switch back on again, the drain-source parasitic capacitor discharges through the power switch, which transforms the stored energy into heat. Efficiency suffers, especially at a high operating frequency. D_1 enters conduction and blocks D_2, which is now the source of a reverse-recovery loss. Again, both diodes are simultaneously conducting for a short period, the time current through D_2 transfers to D_1. This is the second overlap.

In Fig. 7, we have captured the schematic of a simplified forward converter operating open loop. Sub-circuit X2 represents the power transformer affected by its magnetizing inductance L_{mag} and a turns ratio N of 0.1. The tertiary winding is represented by sub-circuit X3 and features a turns ratio of 1. The operating frequency driving power MOSFET X4 is 50 kHz.

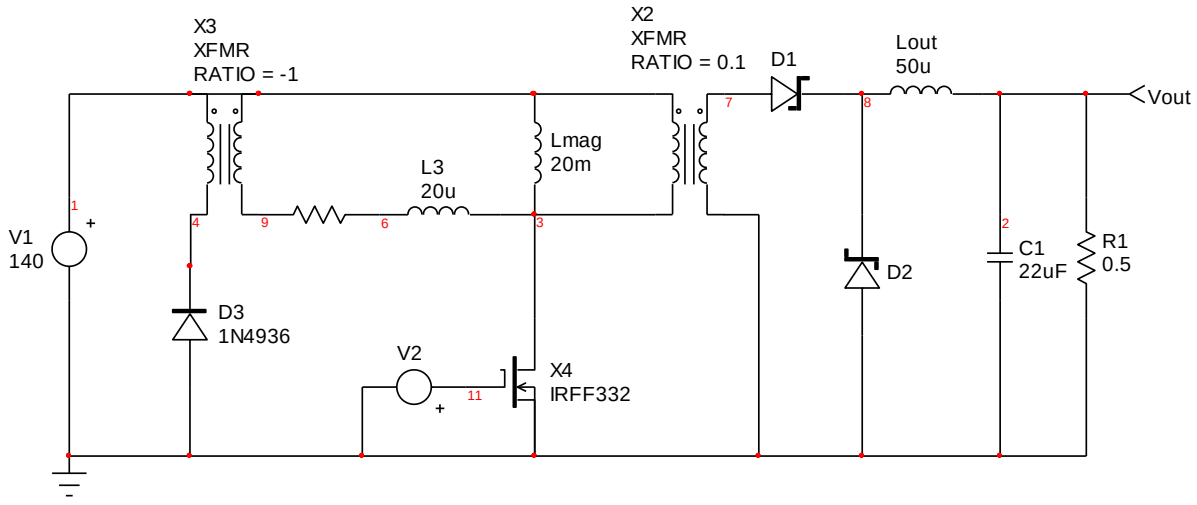

Fig. 7. A simplified forward converter simulation model is enough to reveal key waveforms.

A simulation of the circuit shown in Fig. 7 produces the key operating waveforms shown in Fig. 8. The second waveform represents the voltage on the MOSFET drain whose gate is driven by the upper square-wave signal. The voltage is low during turn-on and energy taken from the source is transmitted to the output. When the MOSFET turns off, it drain-source voltage peaks to twice the input voltage and stays there while the core is energized: the magnetizing current flows back to the source until the transformer core is said to be reset.

This is what you see with the current in D_3 being discontinuous. As expected, the voltage in point A pulses between NV_{in} and $-V_{f_2}$. The output inductor current goes up and down with slopes respectively defined by equations 6 and 9. The output voltage establishes to around 5 V with a low ripple. The output capacitor sees a non-pulsating low-rms current, typical of a buck-derived topology. Let's now have a quick look at the transformer as we need to demagnetize it cycle by cycle.

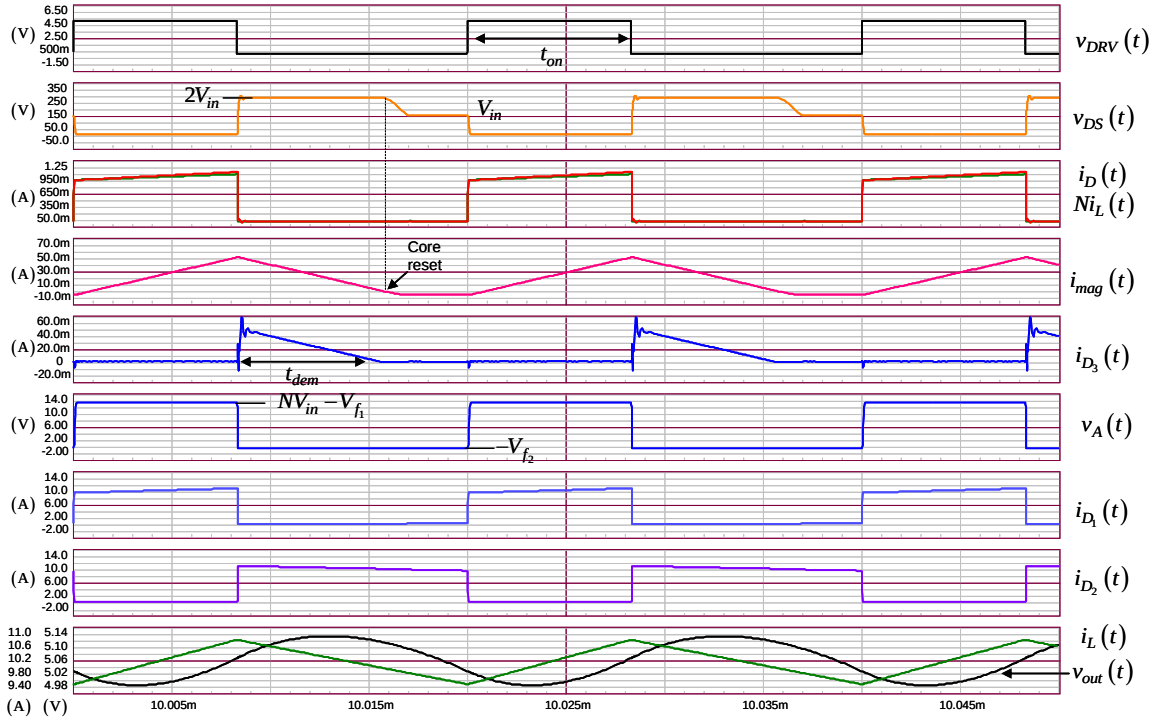

Fig. 8. Classical operating waveforms of a forward converter.

Magnetizing Current

The primary current is made of two components: the magnetizing current i_{mag} and the reflected output inductor current i_L. The magnetizing current is inherent to any transformer construction. As soon as you wind turns in the air or around a magnetic material, you create an inductance. In a transformer, this inductance is modeled on the primary side and is designated as the magnetizing inductance L_{mag}, as shown in the simplified representation of Fig. 9.

When magnetizing current circulates—the core is said to be energized—it aligns the material magnetic domains and allows coupling between primary and secondary sides. In the absence of the magnetizing current—the core is said to reset—voltage and current circulation in the secondary simply disappears.

The important point to capture here is that core saturation only depends on magnetizing current: you can pass tens of amps in a transformer with a magnetizing current not exceeding 500 mA peak for instance. If for any reason magnetizing current runaway occurs, you can saturate the transformer with all its associated problems. It is also interesting to note that iron losses are solely attributed to the magnetizing current, not the output current.

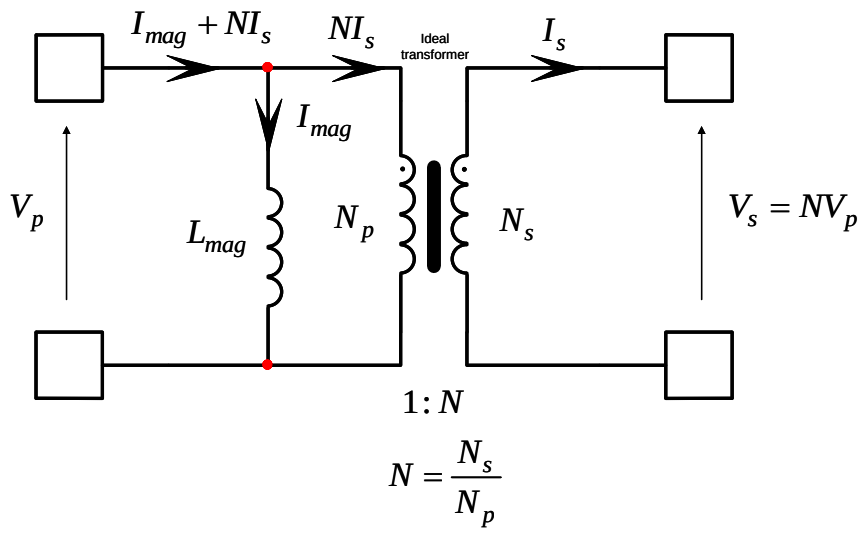

Fig. 9. Any transformer hosts a magnetizing inductance noted L_{mag} in this picture.

When a voltage V_p is applied across the transformer primary in Fig. 9, it appears across the secondary side translated by the transformer turns ratio *N:*

$$V_s = NV_p \,. \tag{12}$$

If the secondary side is loaded, a current simultaneously circulates on the secondary and primary sides. On the primary side, you observe:

$$i_p(t) = Ni_s(t) \,. \tag{13}$$

In the forward converter, when the switch turns on during t_{on}, the input voltage V_{in} is applied across the transformer primary (neglecting $R_{DS(on)}$ losses). The current ramps up in the magnetizing inductance L_{mag} with a slope defined by equation 4. As a result, we can write the following equation:

$$\frac{di_{L_{mag}}(t)}{dt} = \frac{V_{in}}{L_{mag}} \,. \tag{14}$$

If we integrate both sides we have:

$$\int_0^{t_{on}} \frac{di_{L_{mag}}(t)}{dt}\, dt = \int_0^{t_{on}} \frac{V_{in}}{L_{mag}}\, dt \,. \tag{15}$$

Rearranging, we obtain:

$$[\text{Wb}]\, L_{mag} \Delta I_{L_{mag}} = V_{in} t_{on}\, [\text{V-s}] \,. \tag{16}$$

This equation shows that volt-seconds (V-s) applied across the magnetizing inductor have the dimension of a flux (Weber or Wb). The longer the switch is turned on, the higher the flux density (flux by core unit area, *B*, in Telsa) that is built up in the core. The energy stored in the magnetizing inductance $\frac{1}{2} L_{mag} I_{L_{mag},peak}{}^2$ does not contribute to the energy transfer between the source and the output. However, if this stored energy is not

released somewhere during the off-time, the flux density *B* will accumulate and eventually, the transformer core will saturate. This is what is drawn in Fig. 10 where the on-time induces a flux density excursion of ΔB_{on} .

In general, if the off-time volt-seconds equals the on-time volt-seconds, the flux density will return to its starting point. But in this example, the off-time volt-seconds are too weak and an incomplete core reset occurs. So, when a new switching cycle begins, the core flux density starts from a pedestal and its final peak increases. The flux density "walks away" for several switching cycles until the material saturates. At this point, the material permeability μ_r drops to 1 and the magnetizing inductance value collapses. If no precautions are taken to limit the current at turn-on, the primary switch will immediately be destroyed.

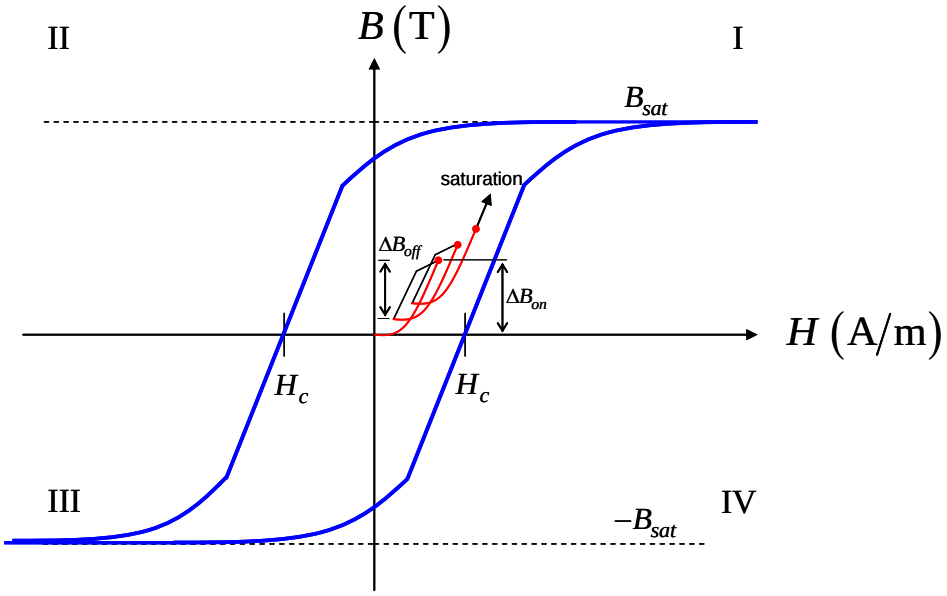

Fig. 10. If a core reset is not implemented, the flux density grows until saturation occurs.

The third reset winding serves this demagnetization purpose. It ensures a complete core reset from cycle to cycle by applying the same voltage V_{in} during the on and demagnetization times. For this reason, the on-time volt-seconds must not exceed the demagnetization time volt-seconds:

$$V_{in}t_{on} \le V_{in}t_{dem} . \quad (17)$$

Since the total switching period T_{sw} is $t_{on} + t_{off}$, a forward converter featuring a third demagnetization winding having a 1:1 turns ratio with the primary cannot operate with a duty ratio larger than 50%. Accounting for some design margin, a dead-time period denoted DT, usually the maximum duty ratio is safely clamped to 45%.

You can operate the converter at a higher duty ratio if you change the third winding ratio by allowing a reset voltage greater than V_{in}. But you pay for it with a higher drain-source voltage excursion at turn off. Fig. 11 shows the simulated voltage across the transformer primary and the associated magnetizing current that is operated in the discontinuous conduction mode (DCM). The driving voltage $v_{DRV}(t)$ is represented and shows that the off-time is comprised of the demagnetization portion plus the dead time.

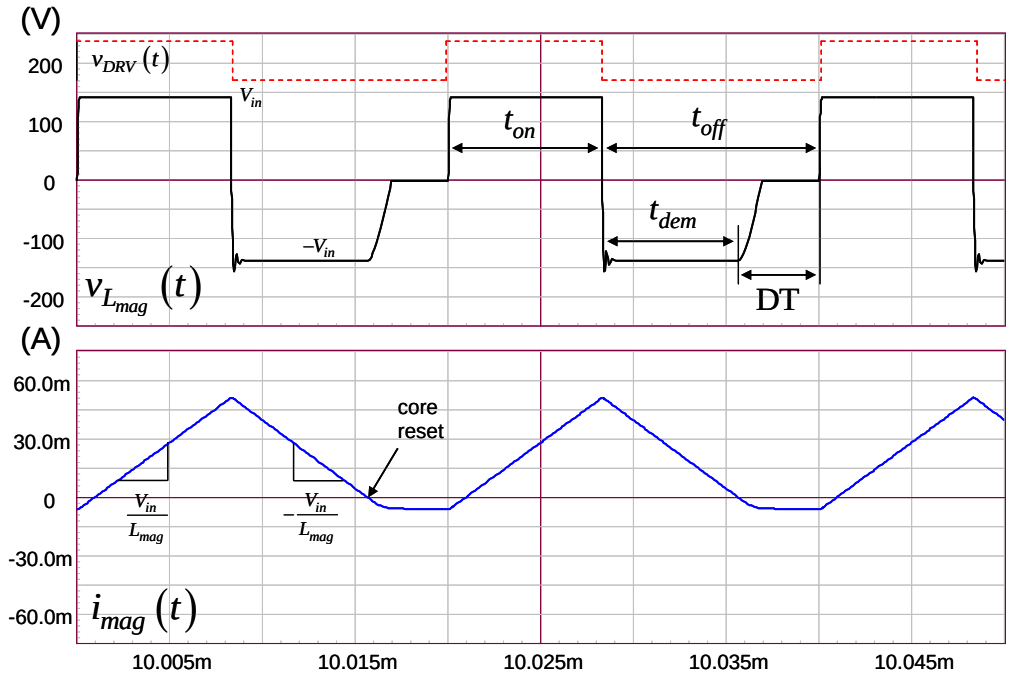

Fig. 11. The simulated primary voltage and the associated magnetizing current. As a resonance takes place between the primary inductance and the drain lumped capacitance, the current can swing negative.

We have seen in equation 11 that the magnetizing current resonates at core reset. This is the reason why it swings below zero during the dead time. However, given the conducting diode D_2 on the secondary side, the drain cannot drop lower than the input voltage. The primary voltage is zero, forcing a pause in the magnetizing current before the next turn-on cycle occurs.

Small-Signal Analysis

There are several ways to obtain the small-signal response of a power converter: state-space averaging (SSA), linearized large-signal equations, the PWM switch model and simulation to cite the most-known methods. SSA is a powerful means but you have to consider the totality of the converter circuitry while you identify state variables. For instance, should you derive the transfer function of a buck converter and afterwards consider adding an input filter or extra losses, you will have to re-start your analysis from scratch. This is one of the SSA drawbacks besides matrix manipulations.

Linearizing large-signal equations implies that you identify voltages and currents circulating in the converter at steady-state and average them over a switching cycle. Then you perturb these equations (or apply partial differentiation) to extract small-signal ac responses. Even if this method does not require matrix manipulations, it is still describing the converter at a given state. Adding extra elements or slightly changing the configuration will require that you extract new equations again.

The PWM switch model is an elegant approach mimicking what has been done with Ebers-Moll models for bipolar transistors. Considering the power switch and the freewheeling diode guilty of non-linearity in the circuit (other elements such as *L*, *C* and *R* are linear devices), only these devices are considered in the small-signal approach and subject to a linearization process. This is the principle of the PWM switch model introduced in the 1990s by Vatché Vorpérian. Therefore, should you later add a resistance somewhere in the circuit or an input filter, the small-signal model of the switch-diode couple remains the same and no extra linearization is required.

Simulation is another way to obtain the small-signal response of your converter. It is fast and quite easy to implement given the abundant literature on the subject. If parasitic components are well modeled (and this is the most difficult part), the overall ac answer can be close to what a bench experiment will confirm. However, despite an accurate response, you still do not know how poles and zeros affecting the power stage will vary with respect to stray and parasitic elements. This knowledge is fundamental to ensure design robustness when

production spreads kick in: parasitic elements change with temperature but are also subject to lot-to-lot variations, new component selection (your buyer identifies a new lower-cost source for the output capacitor for instance) and so on.

If you do not know what part of the ac response these hidden elements affect, there is no way you can shield your design against their unavoidable variations. Only a complete transfer function analytically derived can tell you where they are and how you can counteract them. Simulation comes as an intermediate step in small-signal analysis, as a quick means to test your design ruggedness against parasitic element changes for instance. The final step in your analysis is always given by a prototype response measurement on the bench.

Large And Small-Signal Equations

Now let us see what our forward converter looks like in terms of elements pertaining to small-signal analysis. Fig. 12 shows the time-domain representation of our circuit. The left side depicts the pulse-width modulator that links the duty ratio value, $D = t_{on}/T_{sw}$, to the error voltage v_{err} coming from the compensator. The source $v_A(t)$ expresses the voltage at node A as described by equations 5 and 8 respectively during the on and off times. Finally, the right side is the *LC* filter typical of the buck-derived topology. What we want is the ac transfer function linking V_{out} to the control variable, V_{err}.

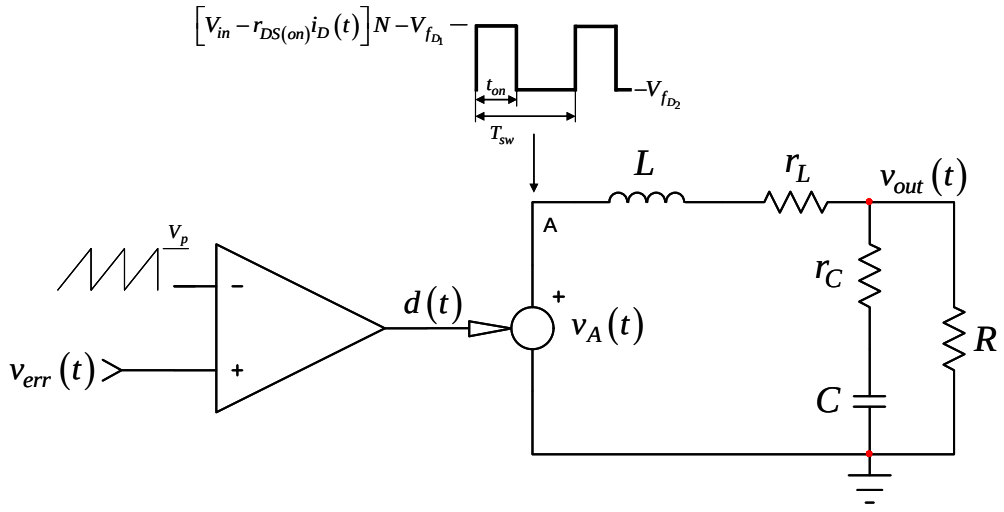

Fig. 12. A simplified representation of the forward converter shows a controlled source followed by an LC filter. On the left side, the pulse width modulator is represented.

In equation 5, the magnetizing current combines with the power switch $R_{DS(on)}$ and creates a voltage drop that subtracts from the input voltage during the on-time. This drop is then transmitted to the output, scaled down by the transformer turns ratio *N*. This is what Fig. 12 shows.

During the design of a forward converter transformer, the magnetizing current is minimized because it has no role other than energizing the transformer. It does not play a role in the power transfer and designers purposely keep it to a minimum, ensuring the absence of saturation in the worst case. However, that situation is no longer the case with the active clamp converters as we will see in a future part of this articles series.

In the active clamp version of the forward converter, designers need the magnetizing current and purposely grow it. In our present case, given its low value, it has no small-signal role and can be neglected in equation 5. The forward voltage drops of diodes D_1 and D_2 play a role in the dc operating point and their dynamic resistances r_d affect the impedance driving point A, respectively during DT_{sw} and $(1-D)T_{sw}$. If considered equal, they can easily be lumped in the ohmic element affecting the inductor, r_L. Finally, for the sake of simplicity, the voltage at point A can be further reduced to what is shown in Fig. 13.

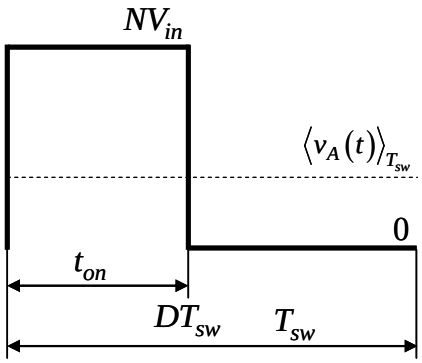

Fig. 13. The voltage at point A toggles between NV_{in} and 0 V if we neglect the diode forward drops.

This waveform is discontinuous in time at the transition between the on and off times. To work with linear networks and apply Laplace transforms, we need linear and continuous-time functions. As explained in reference 1, we can transform this switching waveform into a continuous-time function by the process of averaging. What matters is to find the relationship that links the signal averaged value to its control variable, the duty ratio *D*.

The average value of a periodic signal is found by integrating the representative function *f*(*t*) along the considered period:

$$\langle f(t)\rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_0^{T_{sw}} f(t)\cdot dt \,. \tag{18}$$

In our case, the average voltage at point A is simply:

$$\langle v_A(t)\rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_0^{DT_{sw}} NV_{in}\cdot dt = \frac{NV_{in}}{T_{sw}}[t]_0^{DT_{sw}} = DNV_{in} \,. \tag{19}$$

This is a so-called time-continuous large-signal (read non-linear) equation. It is nonlinear because *D* and V_{in} are separate variables that can independently vary. As explained previously, to extract the small-signal transfer function of our converter, we need linear equations. In other words, a *linearization* process must be applied to equation 19 to make it a linear expression. In this expression, we have two variables, *D* and V_{in}. To check the response of this equation to perturbations, we associate each variable with a small ac ripple modulation noted with a caret (^). This ac ripple is considered small enough to keep the whole converter in a linear mode[1] while sweeping frequencies:

$$V_A \rightarrow V_A + \hat{v}_A$$

$$V_{in} \rightarrow V_{in} + \hat{v}_{in}$$

$$D \rightarrow D + \hat{d} \,.$$

Now, if we rewrite equation 19 with these new elements:

$$V_A + \hat{v}_A = N\left(D + \hat{d}\right)\left(V_{in} + \hat{v}_{in}\right). \tag{20}$$

Developing and rearranging equation 20 gives us:

$$V_A + \hat{v}_A = N\hat{d}\hat{v}_{in} + DNV_{in} + ND\hat{v}_{in} + NV_{in}\hat{d}\,. \tag{21}$$

In the above expression, we have dc terms (no caret symbols), ac terms (terms associated with one caret) and ac cross-products. Because we want linear, small-signal terms only, all ac cross-products ($N\hat{d}\hat{v}_{in}$) are suppressed. We end up having an expression combining dc and ac terms. If we sort them out, we have:

$$V_A = DNV_{in} \tag{22}$$

$$\hat{v}_A = N\left(D\hat{v}_{in} + \hat{d}V_{in}\right). \tag{23}$$

With these equations on hand, we can now update the right half of the Fig. 12 schematic as shown in Fig. 14. It is a continuous-time linear circuit.

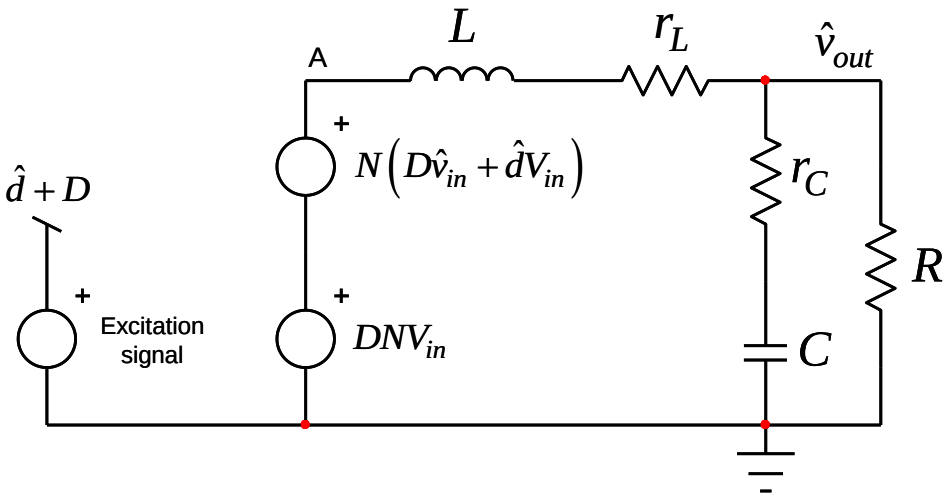

Fig. 14. The time-domain source $v_A(t)$ has been replaced by continuous-time voltage sources. One of these sources fixes the dc point while the second brings the ac signal in.

Pulse Width Modulator Transfer Function

The PWM block converts the error voltage $v_{err}(t)$ into a duty ratio D. At its negative input, a comparator receives a sawtooth signal ramping from 0 V to a peak value, V_p. Its positive input receives the error voltage v_{err}. When the sawtooth signal is below the error voltage, the comparator output is high and biases the power transistor to its on-state (Q_1 in Fig. 1). The sawtooth keeps ramping up and when both pins levels coincide, the comparator toggles low and ends the switching cycle. This is what is called trailing-edge modulation.

Cycle by cycle, the duty ratio varies through a succession of discrete values. This is what we represented in Fig. 15 in which you can see the duty ratio at different moments. This is the illustration of what is designed as a *naturally sampled* pulse width modulator. At the toggling point t_1, we can write:

$$v_{err}\left(t_1\right) = \frac{V_p}{T_{sw}} t_1\,. \tag{24}$$

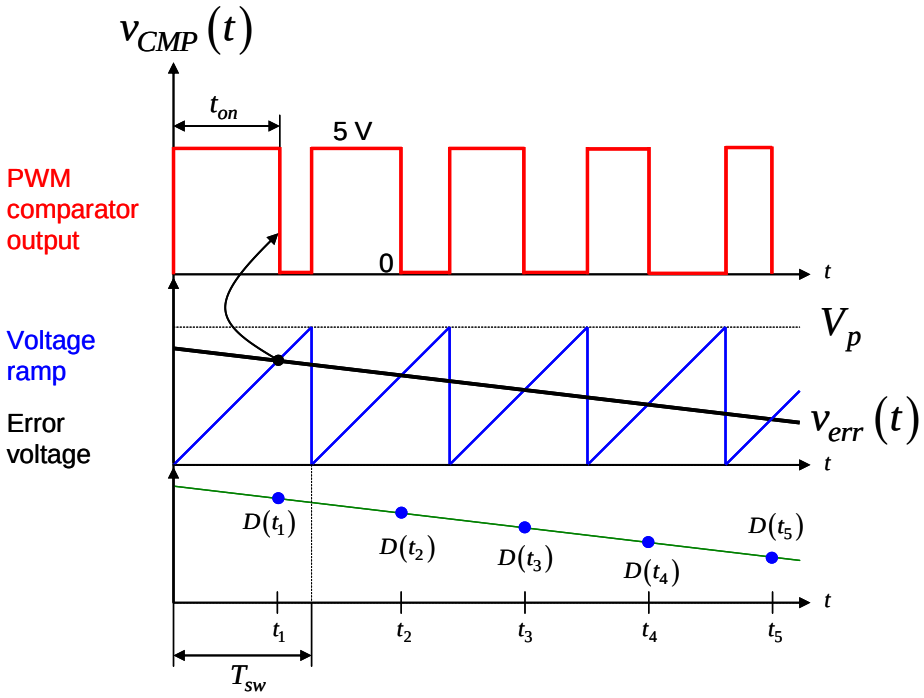

Fig. 15. The duty ratio is a discrete value that changes cycle by cycle.

Duration t_1 is nothing else than the transistor on-time. Divided by T_{sw}, it becomes the duty ratio at the instant t_1:

$$v_{err}(t_1) = V_p \frac{t_{on}(t_1)}{T_{sw}} = V_p D(t_1) . \tag{25}$$

Now, if we consider the modulation frequency of the perturbation f_{mod} that we superimpose on v_{err} during ac analysis to be much smaller than the switching frequency F_{sw}, otherwise stated $f_{\mathrm{mod}} << F_{sw}$, then all discrete duty ratio points can be considered very close to each other, making the discrete-time function described by equation 25 a continuous and ripple-free function defined as:

$$D(V_{err}) = \frac{V_{err}}{V_p} . \tag{26}$$

This is the averaged expression of the duty ratio generated by the naturally sampled PWM block. The small-signal gain can be extracted by perturbing D and the error voltage:

$$V_{err} \rightarrow V_{err} + \hat{v}_{err}$$

$$D \rightarrow D + \hat{d} .$$

Once substituted in equation 26 and rearranged, we have:

$$D + \hat{d} = \frac{V_{err} + \hat{v}_{err}}{V_p} . \tag{27}$$

From equation 27 we extract the ac relationship linking the duty ratio to the error voltage. This is our PWM small-signal gain G_{PWM}:

$$G_{PWM} = \frac{\hat{d}}{\hat{v}_{err}} = \frac{1}{V_p} . \tag{28}$$

This is it, we now have the complete transmission chain from the error voltage to the forward output voltage. The final ac-only model appears in Fig. 16.

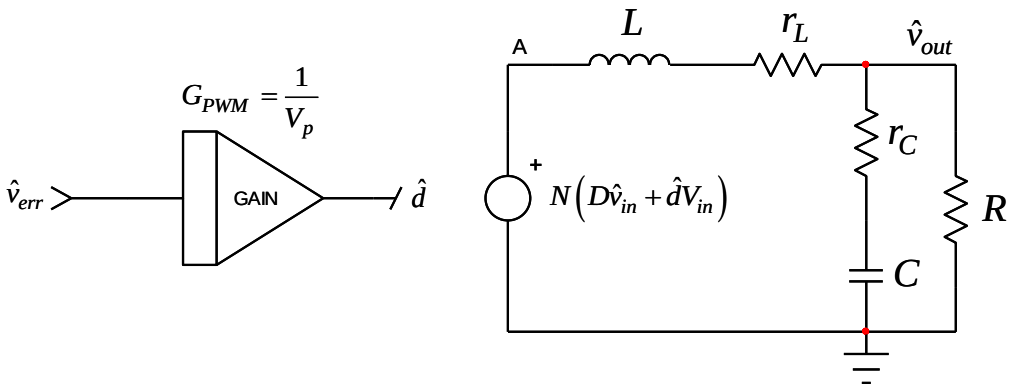

Fig. 16. The complete forward converter small-signal model from the error voltage to the output voltage.

Final Transfer Function

With the help of Fig. 16, the transfer function of the forward converter operating in voltage mode can be obtained quite quickly. The output voltage is that of node A going through a second-order *LC* filter. Using Laplace notations, the voltage at node A is simply:

$$V_A(s) = N\left(V_{in}V_{err}(s)G_{PWM} + V_{in}(s)D\right) . \tag{29}$$

Since we want to study $V_{out}(s)/D(s)$ at a constant input voltage, $V_{in}(s) = 0$ and equation 29 simplifies to:

$$V_A(s) = NV_{in}V_{err}(s)G_{PWM} . \tag{30}$$

The *LC* transfer function can be derived using fast analytical techniques[2] and put under the well-known second-order polynomial form as:

$$\frac{V_{out}(s)}{A(s)} = H_0 \frac{1 + s/\omega_{z_1}}{1 + \frac{s}{\omega_0 Q} + \left(\frac{s}{\omega_0}\right)^2} \tag{31}$$

in which we have:

$$H_0 = \frac{R_{load}}{R_{load} + r_L} \tag{32}$$

$$\omega_{z_1} = \frac{1}{r_C C} \tag{33}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \sqrt{\frac{r_L + R_{load}}{r_C + R_{load}}} \tag{34}$$

$$Q = \frac{LC\omega_0 \left(r_C + R_{load}\right)}{L + C\left[r_L r_C + R_{load}\left(r_L + r_C\right)\right]}. \tag{35}$$

The final transfer function is thus obtained by combining equations 29 and 31:

$$\frac{V_{out}(s)}{V_{err}(s)} = G_{PWM} N V_{in} H_0 \frac{1 + s/\omega_{z_1}}{1 + \frac{s}{\omega_0 Q} + \left(\frac{s}{\omega_0}\right)^2}. \tag{36}$$

In this expression, G_{PWM} can be replaced by equation 28.

We can now plot these Laplace transfer functions using Mathcad for which we have used the following component and operating values:

L = 0.5 µH, r_L = 5 mΩ, C = 1.2 mF, r_C = 1.5 mΩ, V_p = 2 V, R_{ramp} = 75 kΩ, C_{ramp} = 390 pF, F_{sw} = 500 kHz, N = 1/6, V_{in} = 36 to 72 V, V_{out} = 3.3 V and R_{load} = 0.11 Ω. Results appear in Fig. 17.

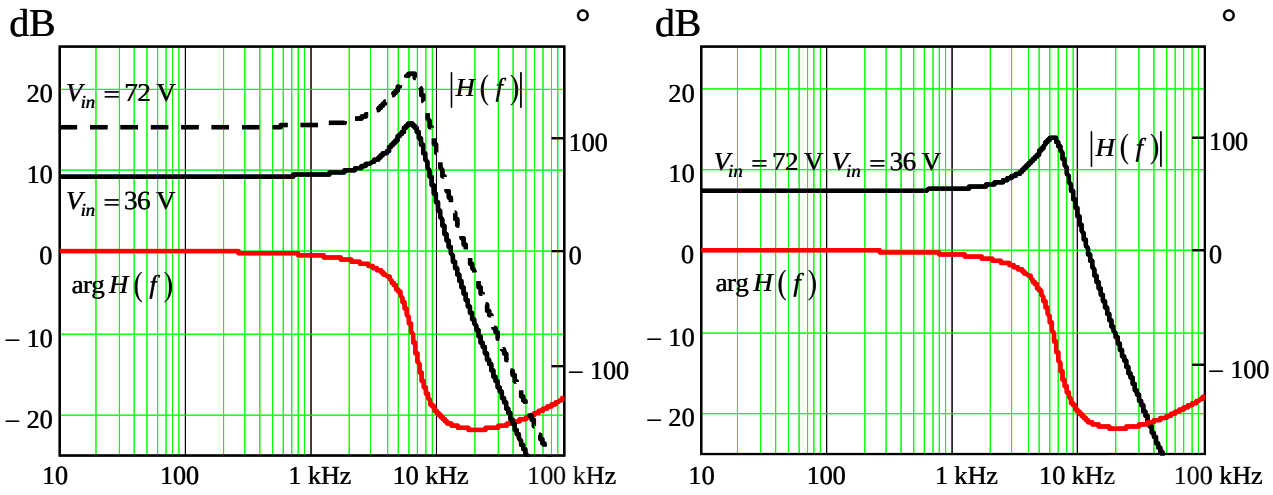

Fig 17. The graph on the left shows the dependency of the transfer function on the input voltage. However, in the graph on the right, thanks to feed forward, the transfer function is immune to changes in input voltage.

In Fig. 17, the graph on the left plots the transfer function at two different input voltages, both under full load. You can see how the gain changes depending on the input line voltage. A 36-V to 72-V change (a ratio of 2) is simply a 6-dB translation. This change will impact the crossover frequency, perhaps at a point where the phase margin is degraded. Therefore, you must be careful when designing your compensator to account for this crossover change.

A better way is to implement feedforward and cancel the input voltage contribution. Feedforward is a means to implement a corrective action on D as V_{in} changes *before* the disturbance propagates and affects the output. More details on feedforward are given in reference 3. As the right side of Fig. 17 confirms, despite input voltage changes, the transfer function does not undergo any shift.

Conclusion

The small-signal study of the voltage-mode forward converter equipped with a demagnetization winding reveals a second-order system in which dc gain varies depending on the input voltage. Such a contribution can be canceled by using feed forward. In part 2 of this article series, we will investigate the active-clamp forward converter structure and learn how it operates before we tackle its small-signal response later on.

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About The Author

Christophe Basso is an application engineering director at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide."

Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 30 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on the design of forward converters, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Forward" in the Topology category.