

Synchronous Zeta Converter Outperforms The SEPIC

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The SEPIC converter has become increasingly popular because of its ability to regulate an output voltage by bucking or boosting equally well. The Zeta converter, on the other hand, while functionally similar to a SEPIC, has not seen quite as much usage.

A traditional Zeta power stage requires a high-side power switch, lending itself nicely to basic buck controllers that directly drive p-channel FETs. Additionally, using an output rectifier diode limits the output current to a maximum of 3 A to 4 A because of the rectifier's limited power dissipation capability. Toss in limited documentation, and it's easy to see why it's rarely used.

However, the Zeta's usefulness can be extended by converting it to fully synchronous operation and broadening the range of controllers capable of driving it. As a result, its efficiency and flexibility can be significantly improved beyond that of a traditional SEPIC converter. Applications for both Zetas and SEPICs can be found in automotive, LED drivers, and anywhere it's desirable to have a single converter tolerate various input rails without needing to be redesigned as system requirements change.

Circuit Comparison

Fig. 1 shows simplified circuits for a traditional diode-rectified Zeta with p-channel FET, a fully synchronous Zeta with dual n-channel FETs and a diode-rectified SEPIC converter for comparison. All three are shown using coupled one-to-one ratio inductors, but two individual inductors also can be implemented without changing the idealized voltage and current waveforms. It is easy to see that the basic components in a traditional Zeta and a SEPIC are essentially the same, with the differences being the Zeta's p-channel FET versus the SEPIC's n-channel FET and a slight rearrangement of parts.

To improve the efficiency of the traditional Zeta, the synchronous Zeta replaces its p-channel FET and diode with two n-channel FETs. This is similar to how the components in a basic buck converter are changed for synchronous operation. In fact, to implement this, a sync buck controller is used for the sync Zeta. With the vast number of sync buck controllers available today, this gives the designer many options. However, there are a few restrictions that need to be considered to select the proper controller, but first, let's look at the Zeta's operation.

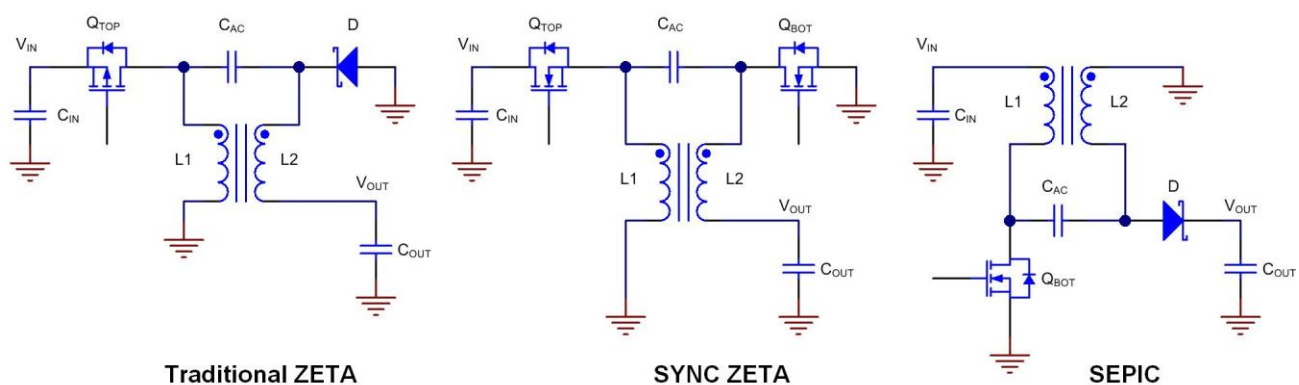


Fig. 1. Zeta and SEPIC converters appear quite similar.

Zeta Circuit Operation

Operation of the sync Zeta^[1] is as follows with waveforms shown in Fig. 2. Its operational duty cycle is $D = V_{OUT} / (V_{OUT} + V_{IN})$ for continuous conduction mode (CCM) operation, which is the same as the SEPIC's.

When the control FET Q_{TOP} turns on, Q_{BOT} will be off. Two paths for the current exist during the time Q_{TOP} is on; current from the input flows through L1 to ground as well as current flowing through C_{AC} and L2 to V_{OUT} . The average current through L1 is equal to the average input current and the average current through L2 is equal to the average output current. Since these two currents simultaneously flow when Q_{TOP} is on, the coupled inductor must be capable of handling a total current of greater than $I_{IN} + I_{OUT}$, which is highest at minimum input voltage.

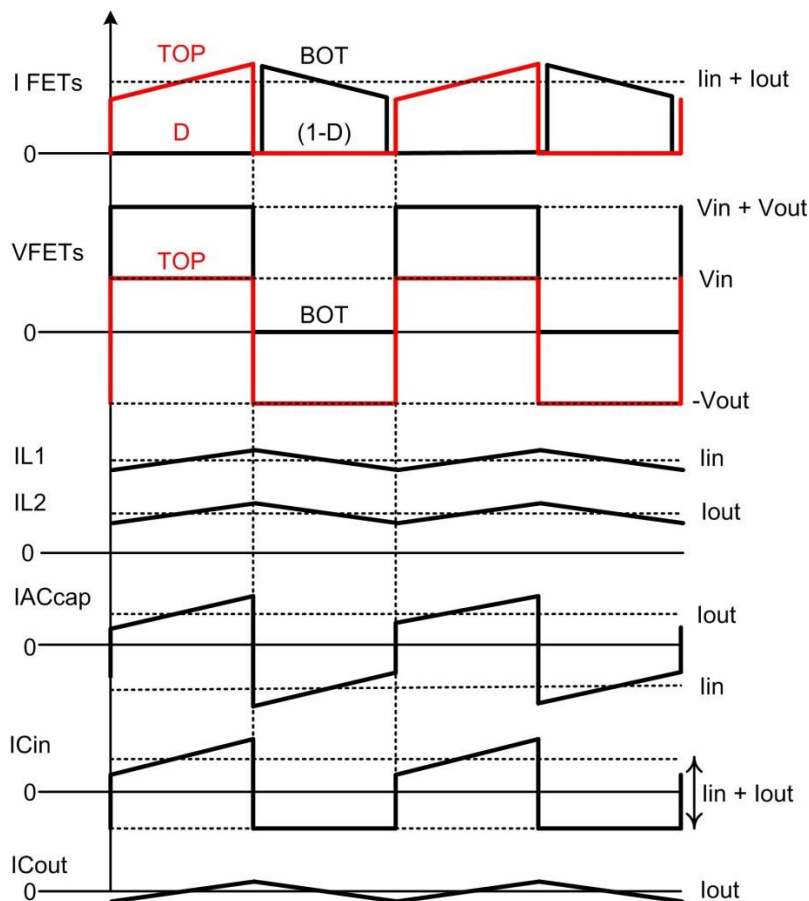


Fig. 2. Zeta converter ideal waveforms.

If individual (non-coupled) inductors are used, each must be capable of handling their respective currents. When Q_{TOP} turns off and Q_{BOT} turns on, the current in each inductor opposes change. The current flowing in L1 must now change paths and flow through Q_{BOT} and C_{AC} and the current flowing in L2 must now flow through Q_{BOT} . This can be seen in the current waveforms of L1 and L2 in Fig. 1, where L1 always conducts I_{IN} and L2 conducts I_{OUT} and Q_{TOP} and Q_{BOT} must each handle $I_{IN} + I_{OUT}$ during their respective on times.

The current flowing in C_{AC} alternates between I_{OUT} and $-I_{IN}$ and generally realizes a large rms current, so proper selection of this capacitor is critical. As the FETs switch states, the voltage across Q_{BOT} alternates between ground and $V_{IN} + V_{OUT}$, while Q_{TOP} 's source voltage switches between V_{IN} and $-V_{OUT}$.

Zeta Versus SEPIC

There are many similarities between the current and voltage stresses of the Zeta and SEPIC. In fact, it may be simpler to just compare the two major differences. The Zeta's ac-coupling capacitor has a voltage of V_{OUT} across it while the SEPIC has V_{IN} . Secondly, the ripple currents between the input and output capacitors are reversed. The Zeta's input capacitor and the SEPIC's output capacitor have a large ripple current, but the Zeta's output capacitor and the SEPIC's input capacitor have a small ripple current.

These small ripple currents (input on the SEPIC and output on the Zeta) are set by the value of the inductance, so in CCM operation, their rms content is typically low. However, the rms content of the Zeta's output capacitor and the SEPIC's input capacitor can be quite large. This may require multiple ceramics, large aluminum or polymer capacitors. Table 1 shows the relative magnitudes of current and voltage stresses between the Zeta and SEPIC. With so many similarities between the two, it begs the question as to which one to use? The goal of this article is to see what advantages and/or disadvantages there are in synchronizing a Zeta.

Table 1. Zeta and SEPIC component stresses mirror each other.

Zeta		SEPIC	
Q_{TOP} current	$I_{IN} + I_{OUT}$	Q_{BOT} current	$I_{IN} + I_{OUT}$
Q_{TOP} voltage	$ V_{IN} + V_{OUT} $	Q_{BOT} voltage	$V_{IN} + V_{OUT}$
Q_{BOT} current	$I_{IN} + I_{OUT}$	D current	$I_{IN} + I_{OUT}$
Q_{BOT} voltage	$V_{IN} + V_{OUT}$	D voltage	$ V_{IN} + V_{OUT} $
L1 current	I_{IN}	L1 current	I_{IN}
L2 current	I_{OUT}	L2 current	I_{OUT}
C_{AC} current	$ I_{IN} + I_{OUT} $	C_{AC} Current	$ I_{IN} + I_{OUT} $
C_{AC} voltage	$ V_{OUT} $	C_{AC} Voltage	V_{IN}
C_{IN} current	$ I_{IN} + I_{OUT} $	C_{IN} Current	ΔI_{L1} pp
C_{OUT} current	ΔI_{L2} pp	C_{OUT} current	$ I_{IN} + I_{OUT} $

Design Example

Table 2 lists the basic requirements for a design comparison, and Fig. 3 shows the Zeta converter schematic. These requirements are typical of an automotive battery voltage. One primary goal of this design is to use all surface-mount components while trying to extract as much output power as possible. This means that power dissipation must be minimized so that no individual component dissipates more than about 1 W, otherwise heat sinks will be required.

Table 2. Prototype design specifications.

Parameter	Specification
Input voltage	6 V to 16 V
Output voltage	12 V
Max output current	4 A min, 5 A typical
Ripple	<1%
Efficiency (max load)	95%

The highest current stresses in this design occur at low input voltage and max load. At this operating point, many of the power stage components will need to handle $I_{IN} + I_{OUT}$. Assuming 90% efficiency at low line, the input current will be 8.9 A and $I_{IN} + I_{OUT}$ will be 13.9 A. Since an input of 6 V occurs as a transient, sustained operation is not required at this point, but the circuit components must be rated to handle this voltage.

The coupled inductor's rms current rating must be greater than 13.9 A as well as its saturation rating, which must also include the additional magnetizing current. An inductance of 12 μ H was chosen (RENCO RL-9426), which allows the circuit to remain in continuous operation for loads above 1.2 A. The maximum rms current in the Zeta top FET and in the SEPIC FET is nearly 13 A, and also occurs at low line where the duty cycle is 0.67.

Low $R_{DS(ON)}$ 60-V FETs were selected to minimize conduction losses, which dominate in this application. The Zeta's bottom FET handles about 30% less rms current than the top FET, so it will have lower overall losses. However, the SEPIC's output rectifier losses will be its forward drop times the output current. This will be the major factor contributing to lower efficiency as the output current increases in the SEPIC.

The limiting factor in the rectifier is its thermal performance, since printed circuit board (PCB) mounting significantly increases its die temperature. The ac capacitor must handle 7.5 A rms in both converters, and should be rated for at least 25 V in the SEPIC, but only 16 V in the Zeta. The capacitance selected was sized to minimize ripple voltage across the capacitor to less than 10% of the minimum input voltage at full load.

Both the Zeta's input capacitor and the SEPIC's output capacitor have rather tough requirements. Each requires at least 150 μ F and must handle 7.5 A rms, so aluminum-polymer capacitors were selected. It's interesting to note that while the output capacitor of the Zeta has low ripple current and only requires about 15 μ F to meet design specifications, polymer capacitors were used on its output to provide good load-transient performance. The loop bandwidth on both converters is rather low, so this is essential if the application is expected to have non-static loads. It's also a good idea to have additional input capacitance on the SEPIC, if the source voltage is not near the converter or if its impedance is high.

Controller Selection

A great benefit of employing synchronous operation in a Zeta is that a sync buck controller can be used.^[2] Since the Zeta has two switching nodes, the connection to the buck controller's high-side drive must be configured differently than a typical buck application. The bottom FET's drain voltage switches between ground and $V_{IN} + V_{OUT}$. The controller's SW pin and the BOOT capacitor need to connect here so that BOOT capacitor C9 can be charged to the controller's internal bias voltage V_{CC} (typically about 7.5 V), through diode D2, when switched to ground.

This connection is necessary to allow the BOOT capacitor to recharge, so that it can drive the top FET, before the FET's attempt to switch. When the bottom FET turns off, and while it is still conducting through its body diode, the source of the top FET will be at $-V_{OUT}$, since the ac coupling capacitors (C6 through C8) always have a $-V_{OUT}$ potential across them. In order to turn on the top FET at this point, its gate voltage must be level-shifted by this amount ($-V_{OUT}$) since the BOOT capacitor is on the other side of the ac cap. Capacitor C4, D1 and R4 accomplish this.

Writing the voltage loop equations for the top FET gate drive shows that the voltage across C4 is equal to V_{OUT} . The function of diode D1 is to clamp the negative transition of the gate voltage to a diode drop, allowing nearly the full BOOT capacitor voltage to be available on the positive turn-on transition while the FET's maximum gate-to-source voltage is limited to no greater than V_{CC} .

Use of a sync buck controller in a Zeta application places higher than typical voltage stresses on it, so care must be taken so that the controller is not overstressed. The SW pin, which can have V_{IN} max applied to it when used in a buck converter, will need to withstand V_{IN} max + V_{OUT} . The user is required to limit the max input voltage to that of the controller's max SW pin rating less the output voltage.

For the circuit shown in Fig. 3, the controller's maximum SW rating is 100 V and the output voltage is 12 V, so this controller can withstand an absolute maximum input voltage of 85 V. This provides a large safety margin and flexibility for use in other applications with little worry of running out of margin. External BOOT diode D2, used to charge BOOT capacitor C9, also should have a reverse voltage rating greater than V_{IN} max + V_{OUT} .

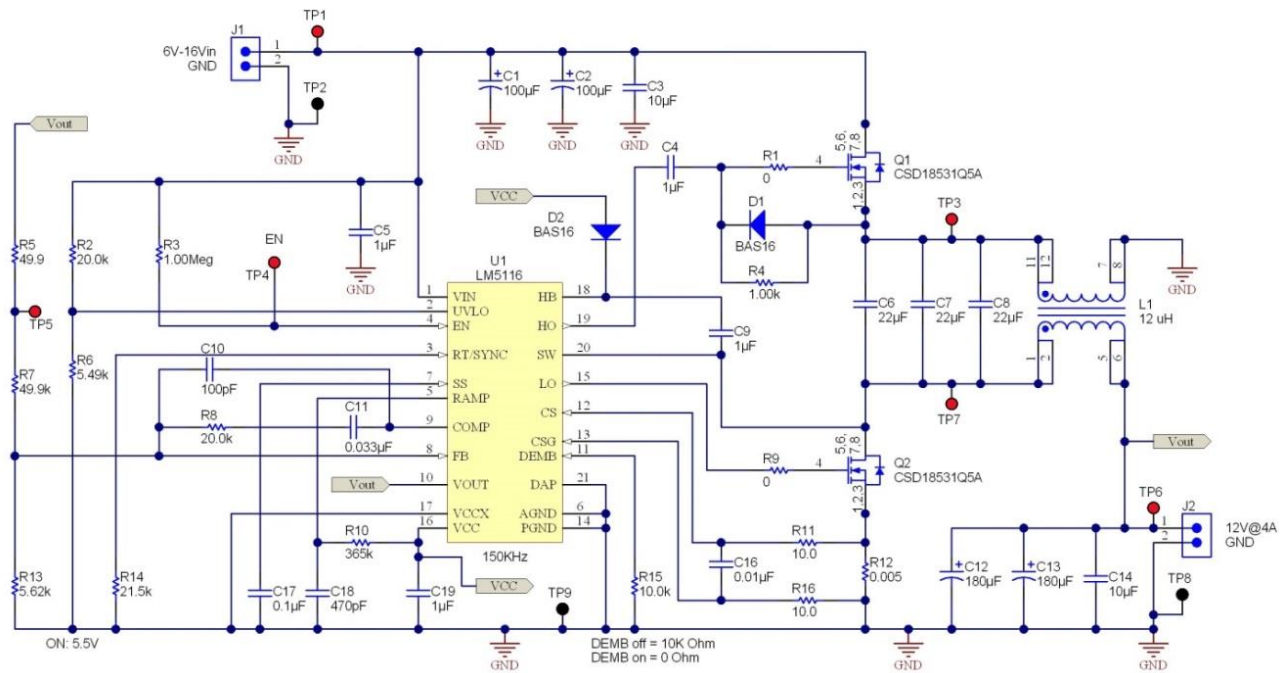


Fig. 3. 12 V at 4 A Zeta converter schematic with coupled inductor.

Prototype Performance

The prototype Zeta and SEPIC converters are shown in Fig. 4. Details of the SEPIC converter design can be found at this [link](#).^[3] To keep the comparison fair, the SEPIC’s FET was changed to a CSD18531Q5A and its output lowered slightly to 12 V, the same as the Zeta’s. The power stage components were kept as common as possible between the two designs. Careful inspection shows that the Zeta circuit requires slightly more PCB area due to the larger control circuit and the additional input capacitors. Output capacitors identical to that of the SEPIC’s were included to maintain similar load transient performance.

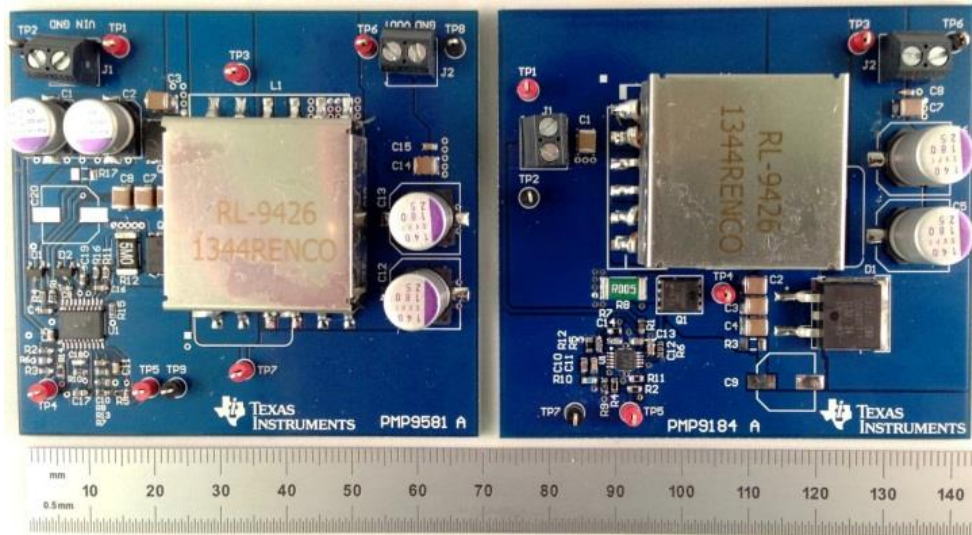


Fig. 4. Zeta (left) and SEPIC (right) converter prototypes occupy similar areas.

In most cases, high-power, low-input-voltage Zetas and SEPICs have low-frequency right-half plane-zeros and complex control loop characteristics that generally dictate a low loop bandwidth. Adding these output capacitors generally benefits circuit performance. If the load is static, these extra capacitors could possibly be eliminated

or greatly reduced. These additional components, as well as a second FET, add cost to the sync Zeta over that of the SEPIC.

Nonetheless, Fig. 5 shows the efficiency benefit realized in the prototype sync Zeta compared to a diode-rectified SEPIC. The higher losses of the SEPIC limit its output power due to the rectifier's elevated temperature. In this example, if the user decided to limit power losses to 3 W, the SEPIC's output current would be limited to a maximum of 3.75 A. However, the sync Zeta can deliver 5 A for the same losses, or an improvement of 33%.

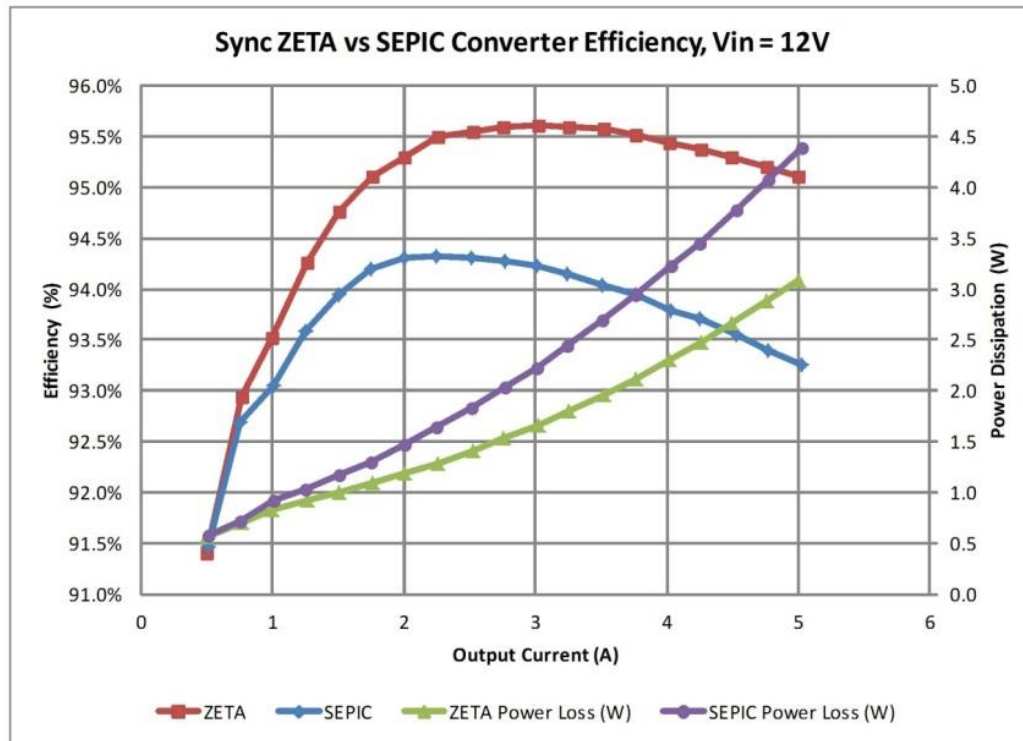


Fig. 5. The efficiency of the synchronous Zeta converter easily beats that of a diode-rectified SEPIC.

Summary

Zeta and SEPIC converters have a similar appearance and similar component stresses, but operate differently from each other. The FET and rectifier placement in the Zeta allow for easy synchronization with n-channel FETs and a synchronous buck controller.

Compared to the performance of a traditional SEPIC, the synchronous Zeta offers higher efficiency and/or higher output current. The circuit's size and cost is slightly greater than that of the SEPIC, but its reduced power losses can provide a higher output current, ease requirements on the input source and possibly eliminate the necessity for heat sinking.

References

1. Jeff Falin, "[Designing DC/DC converters based on ZETA topology](#)," Analog Applications Journal, Texas Instruments, 2Q 2012.
2. Matthew C Kessler, "[Synchronous inverse SEPIC topology provides high efficiency for noninverting Buck/Boost voltage converters](#)," Analog Dialogue, Volume 44 Number 2, May, 2010.
3. TI Design – [40W SEPIC Converter \(with Coupled-Inductor\)-High Efficiency, Operating with Automotive Input Range](#).

4. John Betten, "[Benefits of a coupled-inductor SEPIC converter](#)," Analog Applications Journal, Texas Instruments, 2Q 2011.
5. Datasheets for devices cited in this article: [CSD18531Q5A](#), [LM5116](#).
6. Learn more about the Zeta converter and other power solutions here: <http://www.ti.com/pwr-contrib-006-lp1-en>.

About The Author



John Betten is an applications engineer and a senior member of Group Technical Staff at Texas Instruments, and has more than 29 years of ac-dc and dc-dc power conversion design experience. John received his BSEE from the University of Pittsburgh and is a member of the IEEE.

For further reading on buck-boost and SEPIC converters, see the How2Power Design Guide, select the [Advanced Search option](#), go to Search by Design Guide Category and select "buck-boost" and "SEPIC" in the Topology category.