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Current-Mode Control Stability Analysis For DC-DC Converters (Part 1)

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Current-mode control (CMC) is an extremely popular dc-dc converter loop architecture—and with good reason. Simple operation and dynamics are achieved even though two loops, a wide-bandwidth current loop lurking inside an outer voltage loop, are required. Peak, valley, average, hysteretic, constant on-time, constant off-time, and emulated current-mode are commonly used. Each technique offers plusses and minuses pertaining to the overall design.

In this article, part one in a two-part series, we highlight the fundamentals of loop stability in fixed-frequency, naturally sampled, peak current-mode, buck-derived converters, specifically for industrial and automotive applications. Following a brief review of the operating principles of peak and valley current-mode architectures, the small-signal model for peak current-mode control, including control-to-output transfer function, is set out in detail. Design of the current loop follows, including conditions for slope compensation. The reader solely interested in current-mode control-loop compensation should refer to the upcoming part 2 where an example using a commercially available dc-dc regulator illustrates the design procedure for a current-mode compensator.

Current-Mode Control Schemes

Among the various forms of current-mode control, the most widely used is peak current-mode control with slope compensation, commensurate with its broad adoption by power management IC manufacturers and power supply vendors.[1] Chief among the factors contributing to the popularity of peak current-mode control are its straightforward compensation, inherent cycle-by-cycle overcurrent protection, automatic input-voltage feedforward, and easier implementation of current-sharing for multiphase scalability. Shortcomings are current-loop noise sensitivity and limitation in the switch's minimum on-time, particularly in nonisolated converter applications with high stepdown ratios.

The emulated architecture [2] goes some way to alleviating these flaws. Valley current-mode control [3], on the other hand, has poor line feedforward characteristics and requires a more-difficult implementation of slope compensation. Another option, hysteretic control has excellent transient response, but varies the switching frequency across both line and load. That makes filtering of electromagnetic interference (EMI) more difficult.

Meanwhile, average current-mode control, apropos its high current-loop gain, is perfect for current-source applications. Widely used in PFC boost pre-regulators and battery charging circuits, it benefits from improved noise immunity and better discontinuous conduction mode (DCM) operation while sidestepping the slope-compensation requirement. However, the need to compensate two loops undermines the broader usage of this method.

A Review Of Peak And Valley Current-Mode Control

The converter in Fig. 1 represents a single-phase buck topology operating in continuous conduction mode (CCM) with duty cycle D. Note that the filter inductor DCR and output capacitor equivalent series resistance (ESR) are shown explicitly. Other buck-derived power stage topologies including multiphase buck, isolated forward, full-bridge, and voltage-fed push-pull can substitute here while retaining a similar loop configuration (feedback isolation excepted.)

In such a peak or valley current-mode architecture, the state of the inductor current is naturally sampled by the PWM comparator. The outer voltage loop employs a type-II compensation circuit and a conventional operational transconductance error amplifier (EA) shown with its inverting input, labeled the feedback (FB) node, connected to feedback resistors R_{fb1} and R_{fb2}.

A compensated error signal appears at the EA output, labeled COMP, the outer voltage loop thus providing the reference command for the inner current loop. COMP effectively represents the programmed inductor current level. The current loop converts the inductor into a quasi-ideal voltage-controlled current source: a means by which the inductor is removed from the outer loop dynamics, at least at dc and low frequencies.

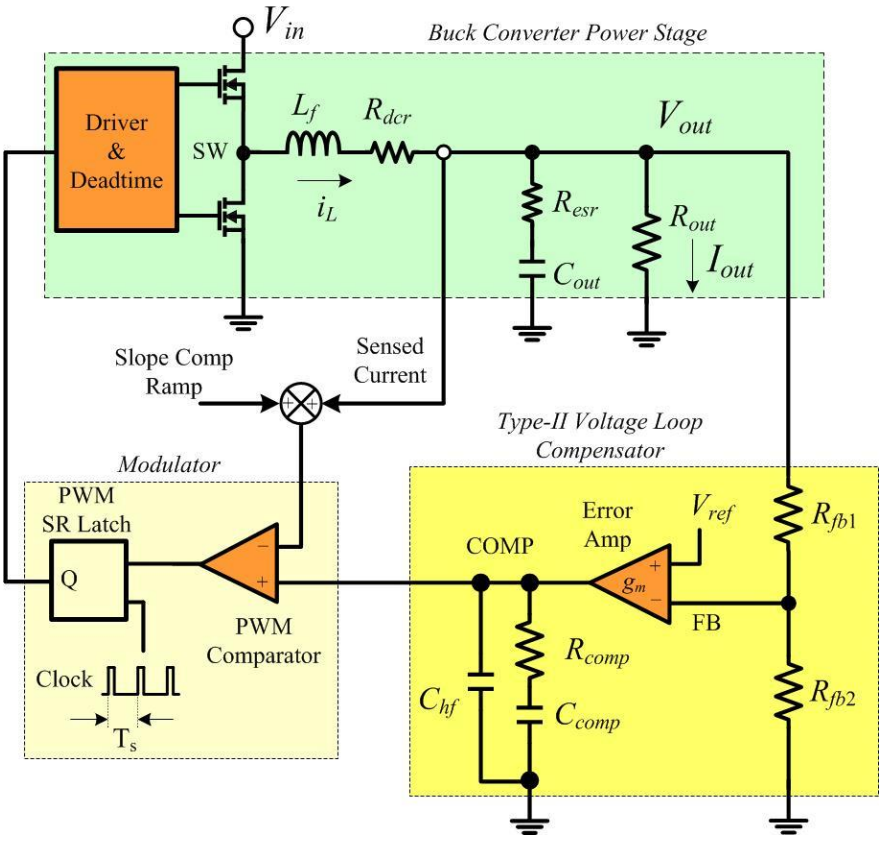

Fig. 1. Dc-dc synchronous buck converter schematic of power train, driver stage and peak/valley current-mode PWM control loop structure with transconductance error amplifier.

The schematic in Fig. 1 positions the current sensor after the inductor. The implementation can be a discrete shunt resistor, or lossless current sensing using MOSFET on-state resistance or inductor DCR.[4] Likewise, co-integrating MOSFETs and controller—using a monolithic die or multiple die co-packaged in a multi-chip module—facilitates lossless current sensing. In any case, the equivalent linear amplifying multiple is given by equation 1

$$R_i = G_i R_s \ [\Omega] \qquad (1)$$

where G_i is the gain of the current sense amplifier (if used), and R_s is the current sensor gain.

A perfect current-mode converter relates only to the dc, or average value of inductor current. In practice, a sampled current-versus-average inductor current error exists in a current-mode implementation. Such error manifests itself as current loop subharmonic oscillation at duty cycles greater or less than 50% for peak and valley operation, respectively. Slope compensation is the well-known and widely used technique of adding a ramp to the sensed inductor current to obviate the risk of subharmonic oscillation.

Fig. 2a illustrates how a turn-on command is activated when the clock edge sets the PWM latch. A turn-off command appears when the sensed inductor current peak plus slope compensation ramp reaches the COMP level. The PWM comparator resets the PWM latch. This is referred to as trailing-edge modulation. S_e is the external slope compensation ramp slope and S_n and S_f are the on-time and off-time slopes of the sensed current signal, respectively.

Similarly, Fig. 2b shows the equivalent waveforms and timing for valley current-mode control with leading-edge modulation. Note that the S and R inputs of the PWM latch in Fig. 1 must be connected as appropriate for the particular implementation.

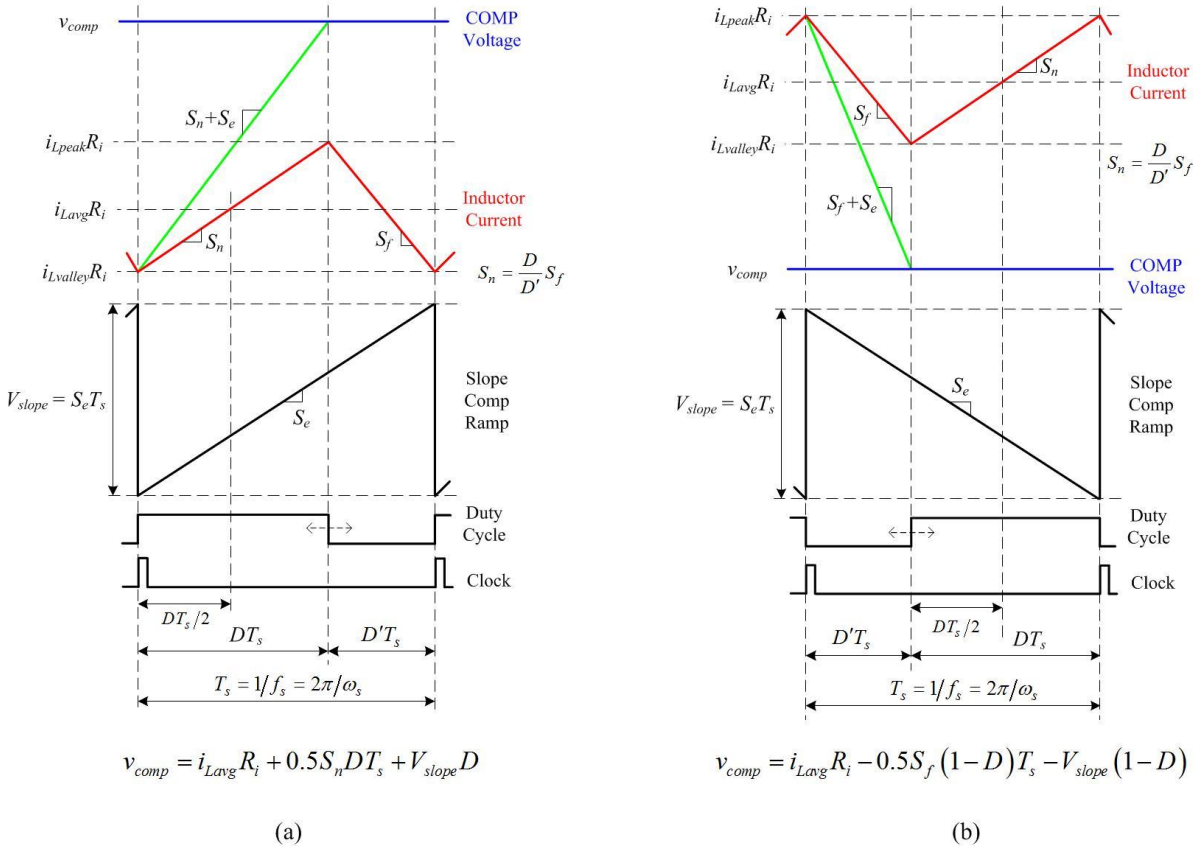

Fig. 2. Modulator waveforms and timing for peak (a) and valley current-mode control (b).

Small-Signal Analysis Of Peak Current-Mode Control

The small-signal dynamic model is derived using Middlebrook and Cuk's state space averaging (SSA) technique and Vorpérian's PWM switch model.[5] Fig. 3 illustrates an intuitive model of the small-signal peak current-mode system in block diagram format.[6]

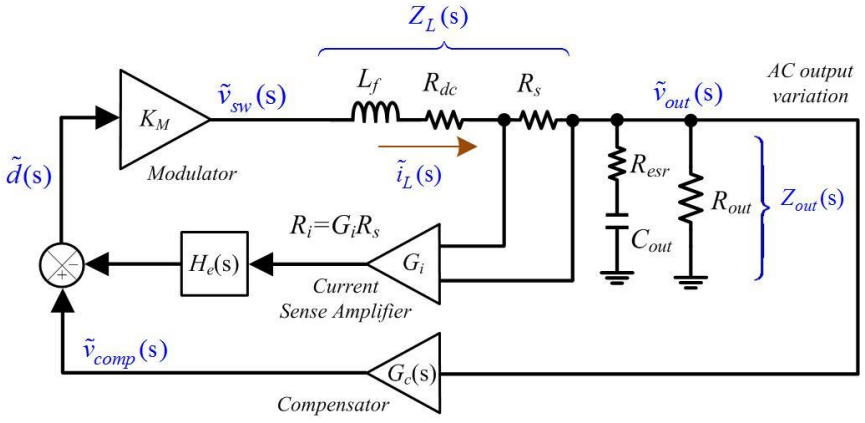

Fig. 3. Simplified small-signal control loop block diagram of a buck converter with peak current-mode control. $H_E(s)$ is the sampling gain block in the current loop.

Modulator gain block K_M is the gain from the duty cycle to the switch-node voltage. Contingent upon the load characteristic, R_{out} represents the small-signal ac load resistance (incremental slope of the load's I-V curve at the dc operating point) given by

$$R_{out} = \begin{cases} R = V_{out}/I_{out} & \text{purely resistive load} \\ R_D & \text{small-signal dynamic resistance, non-linear load, e.g. LED, solar cell} \\ \infty & \text{current source load} \end{cases} .$$

where R represents the load's dc operating point. The component R_{dc} in Fig. 3 is the net series resistance attributed to the inductor DCR, MOSFET on-state resistance, and PCB trace resistance,

$$R_{dc} = DR_{DS(on)hi-side} + D'R_{DS(on)lo-side} + R_{dcr} + R_{pcb} . \quad (2)$$

From Fig. 3, the small-signal ac variations of the switch-node and output voltages are written as

$$\begin{aligned} \tilde{v}_{sw}(\mathrm{s}) &= K_{\mathrm{M}}\left(\tilde{v}_{comp}(\mathrm{s}) - G_i H_e(\mathrm{s}) R_s \tilde{i}_L(\mathrm{s})\right) \\ \tilde{v}_{out}(\mathrm{s}) &= \tilde{v}_{sw}(\mathrm{s}) \frac{Z_{out}(\mathrm{s})}{Z_{out}(\mathrm{s}) + Z_L(\mathrm{s})} \quad . \end{aligned} \quad (3)$$

Thus, the control-to-output transfer function is

$$G_v(\mathrm{s}) = \left.\frac{\tilde{v}_{out}(\mathrm{s})}{\tilde{v}_{comp}(\mathrm{s})}\right|_{\tilde{v}_{in}(\mathrm{s})=0} = \frac{K_{\mathrm{M}} Z_{out}(\mathrm{s})}{Z_{out}(\mathrm{s}) + Z_L(\mathrm{s}) + K_{\mathrm{M}} R_i H_e(\mathrm{s})} . \quad (4)$$

This describes the small-signal behavior of the modulator and power stage when the small-signal input voltage variation is zero. The expressions for impedances $Z_{out}(s)$ and $Z_L(s)$ are substituted into equation 4 to obtain the pole/zero form of the control-to-output transfer function as

$$G_v(\mathrm{s}) = \frac{A_{dc}\left(1 + \frac{\mathrm{s}}{\omega_{esr}}\right)}{\left(1 + \frac{\mathrm{s}}{\omega_p}\right)} H(\mathrm{s}) . \quad (5)$$

H(s), the high-frequency extension in the control-to-output transfer function to model the modulator sampling gain, is discussed in more detail in the next section. The relevant gain coefficients are derived as

$$A_{dc} = \frac{K_{\mathrm{M}} R_{out}}{R_{out} + R_{dc} + R_s + K_{\mathrm{M}} R_i} \approx \frac{R_{out}}{R_i} \frac{1}{1 + \frac{R_{out}}{f_s L_f}\left(m_c D' - 0.5\right)} \quad (6)$$

$$K_{\mathrm{M}} = \frac{1}{\frac{(0.5-D)R_i}{f_s L_f} + \frac{V_{slope}}{V_{in}}}. \tag{7}$$

The dominant filter pole and capacitor ESR zero frequencies are given respectively by

$$\omega_p = 2\pi f_p = \frac{1}{C_{out}\left(R_{out} \| K_{\mathrm{M}} R_i\right)} = \frac{1}{R_{out} C_{out}} + \frac{m_c D' - 0.5}{f_s L_f C_{out}} \tag{8}$$

$$\omega_{esr} = 2\pi f_{esr} = \frac{1}{R_{esr} C_{out}}. \tag{9}$$

Fig. 4 exemplifies a control-to-output transfer function frequency response. The pole and zero locations are denoted by × and **o** symbols, respectively.

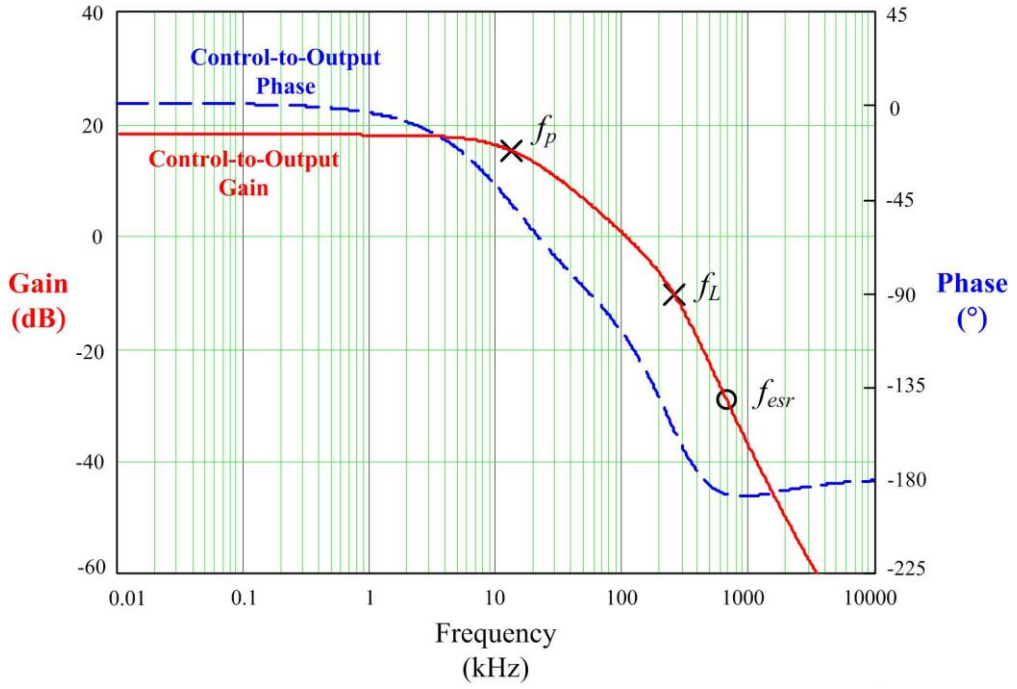

Fig. 4. Typical buck converter control-to-output small-signal frequency response.

Modulator Sampling Gain And Ideal Slope Compensation

A current-mode control system is a sampled system, the sampling frequency of which is equal to the switching frequency. A traditional low-frequency averaged model is modified to include the sampling effect in the current loop. Ridley[5, 6] advised that the sampling action in the peak current-mode loop is an infinite-order system. However, it can be represented in the frequency range of interest by a pair of complex RHP zeros in the current feedback path, denoted using the gain block $H_e(s)$ in Fig. 3, where

$$H_e(\mathrm{s}) = 1 + \frac{\mathrm{s}}{Q_n \omega_\mathrm{n}} + \frac{\mathrm{s}^2}{\omega_n^2}; \quad Q_n = \frac{-2}{\pi}, \ \omega_\mathrm{n} = \frac{\omega_\mathrm{s}}{2} = \pi f_\mathrm{s}. \tag{10}$$

The closed-current feedback loop thus becomes unstable, if it has enough gain leading to subharmonic oscillation. In the control-to-output transfer function, the sampling action is represented as a pair of complex RHP poles located at half the switching frequency such that

$$H(\mathrm{s}) = \frac{1}{1 + \frac{\mathrm{s}}{Q\omega_\mathrm{n}} + \frac{\mathrm{s}^2}{\omega_n^2}}. \tag{11}$$

For any converter, the quality factor is

$$Q = \frac{1}{\pi\left(m_c D' - 0.5\right)} \tag{12}$$

with the slope compensation parameter defined as

$$m_c = 1 + \frac{S_e}{S_n}. \tag{13}$$

For single-cycle damping of an inductor current perturbation, a baseline requirement is that the slope compensation ramp should equal the inductor current down-slope, as given by equation 14,

$$\begin{aligned} S_e = S_f &= \frac{V_{out}}{L_f} R_i \\ V_{slope} = S_e T_s &= \frac{V_{out}}{L_f} R_i T_s \\ m_c D' &= 1 \end{aligned} \tag{14}$$

Accordingly, a perturbed inductor current will return to its original value in one switching cycle. The resultant Q factor, calculated from equation 12, is equal to $2/\pi$ or 0.637. Even though most peak current-mode implementations exploit a fixed-slope compensation ramp amplitude, the ideal slope-compensation level is proportional to output voltage.

Note that excessive slope compensation increases m_c, decreases Q, and reduces the current-loop gain and bandwidth. This portends additional phase lag in the voltage loop and stymies the maximum attainable crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Conversely, insufficient slope compensation decreases m_c and increases Q. This causes peaking in the current-loop gain and ultimately voltage-loop instability as duty cycle approaches or exceeds 50%. Having a Q value in the range of 0.5 to 1.0 is generally satisfactory.

Conclusion

Understanding the operation of a current-mode-controlled dc-dc converter is an important first step for any designer looking to apply current-mode control. This article provides a review of the specific attributes pertaining to peak and valley current-mode architectures. Additionally, the small-signal model shown here illustrates the key considerations required to gain useful insight into the design of a converter using peak current-mode control.

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For further reading on power supply control methods, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Control Methods" in the Design Area category.