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Enhanced OTA Models Improve Design Of Feedback Compensation Networks

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An operational transconductance amplifier (OTA) generates a current-source output that is proportional to a differential input voltage. To achieve ESD robustness in OTAs, a current-limiting series protection resistor (R_{ESD}) and voltage clamp are implemented on the die between the OTA output and the package pinout. Device manufacturers consider the influence of this ESD protection resistor as negligible and the parameter is not described in datasheets.

However, when designing power supply circuits, neglecting to consider the influence of the ESD protection resistor on OTA output impedance may introduce gain and phase errors in the power supply's feedback loop compensation. For example, the presence of the ESD resistor affects the performance of boost converters operating from a low voltage input. Designers can avoid these gain and phase errors by accounting for the effects of the ESD protection resistor in their OTA models.

To support such efforts, this article presents derivations of the transfer functions for power supply OTA compensation that include the effects of the ESD resistor. The three common forms of compensation—types I, II, and III—are considered here. In addition to deriving the corrected transfer functions for each type of compensation, ESD correction factors are derived, which allows the designer to obtain the feedback control transfer functions experimentally.

An Improved OTA Model

An OTA is a voltage-controlled current source amplifier (Fig. 1) whose output current is proportional to the amplifier's differential input. The amplifier transconductance gain is defined as g_m. Requiring less die area than their voltage amplifier counterparts (for equivalent bandwidth), OTAs are frequently implemented as feedback amplifiers in power supply controller and regulator ICs.

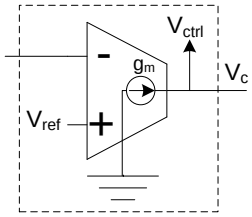

Fig. 1. A simplified OTA model.

When the compensation pin is provided as a package pinout option, die-level ESD protection is implemented by means of a voltage clamp and a current-limiting series resistance at the OTA output (Fig. 2). Furthermore, OTAs have an output impedance consisting of a resistor (R_0) and capacitor (C_0) connected in parallel with one side connected to ground.[2] The amplifier transfer function is determined by the OTA's output impedance structure in combination with an external compensation network.

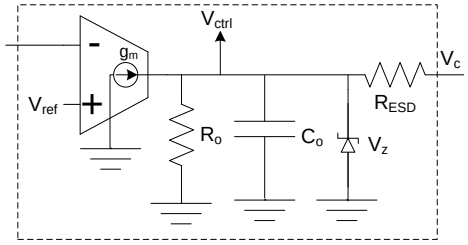

Fig. 2. An improved OTA model including output impedance and R_{ESD}.

The influence of R_{ESD} on the OTA transfer function is negligible for certain applications. Such is the case for PFC boost converters. To illustrate, consider the OTA design examples provided in reference 1 (pp. 359-381). These design examples assume a PFC front end. If we were to take the expressions for OTA transfer functions that

account for the ESD resistor (expressions that will be derived later in this article) and plug in the compensation values given in the reference, we would find that the input voltage feedback divider attenuates the dc gain to the point where the compensation error introduced by R_{ESD} is negligible.

However, boost converter designs operating from a low input-voltage source (such as an automotive battery) do not benefit from significant input voltage gain attenuation by the OTA input-voltage divider. Consequently, the compensation network resistance may require a lower value to achieve desired midband gain attenuation. Consider the cases where a pulse-width-modulator (PWM) IC's control logic uses the V_{ctrl} signal originating from the OTA side of the ESD resistor as the feedback control signal, but the OTA output (V_{ctrl}) is not directly accessible during feedback loop measurements (see Fig. 2 again). If R_{ESD} is of similar magnitude to that of the resistance of the compensation network connected to pin $V_{c,}$ then the simulated response of the power supply feedback loop will contain gain and phase errors when compared to the measured response.

In this article, revised expressions for what the power electronics community describes as Types-I/-II/-III compensation networks are introduced and compared to expressions derived for ideal OTAs.[1] While these revised expressions for the responses of the compensation networks will support analytical approaches to designing these networks, in some cases it may be necessary or desirable to obtain the desired transfer functions experimentally. In those instances, a correction factor may be required to obtain the correct OTA transfer function from empirical measurements obtained from the IC's compensation pin V_c. Correction factors for each type of compensation are derived in this article. The OTA model shown in Fig. 2 is the building block for the Type-I_{esd}/-II_{esd}/-III_{esd} compensation networks that are derived in this article.

In this discussion, parameters from the NCV8871 [4] boost controller IC OTA will be used for supporting design examples. In these examples, the key parameters associated with the NCV8871 are R_o = 3 MΩ, g_m = 1.2 mS, and internal V_{ref} = 1.2 V. In addition, we will need to apply two unpublished parameters—R_{ESD} ≈ 542 Ω and C_o ≈ 10 pF—which were obtained from the NCV8871 IC design group.

Solving Roots Of Second-Order Transfer Functions

The OTA compensation network transfer functions to be derived may be described by the general polynomial expression in equation 1. The orders *m* and *n* of the transfer function are determined by the number of independent storage elements, where $m \leq n$.

When selecting pole and zero placement compensation values, high-order expressions do not offer insight for root identification from the numerator and denominator. An intuitive method for factoring quadratic expressions is described by Middlebrook[3] and is summarized by equations 2 through 7. Roots from equation 2 are defined in equations 6 and 7. For OTA compensation networks, ω_1 and ω_2 are real values.

$$G(s) = -G_0 \frac{1 + a_1 s + a_2 s^2 + \ldots + a_m s^m}{1 + b_1 s + b_2 s^2 + \ldots + b_n s^n} \quad (1)$$

$$1 + a_1 s + a_2 s^2 = 1 + \frac{s}{\omega_0 Q} + \frac{s^2}{{\omega_0}^2} \quad (2)$$

$$\omega_0 = \frac{1}{\sqrt{a_2}} \quad (3)$$

$$Q = \frac{1}{\omega_0 a_1} \quad (4)$$

$$\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)=1+\frac{s}{\omega_0 Q}+\frac{s^2}{{\omega_0}^2} \quad (5)$$

$$\omega_1=\frac{\omega_0}{2Q}\left(1-\sqrt{1-4Q^2}\right) \quad (6)$$

$$\omega_2=\frac{\omega_0}{2Q}\left(1+\sqrt{1-4Q^2}\right) \quad (7)$$

Type-I$_{esd}$ OTA

The Type-I compensation OTA from the simplified OTA model in Fig. 3 is described in reference 1. Capacitor C_1 is located between compensation pin V_c and ground. As a result of the presence of R_{ESD} in series with compensation capacitor C_1, Type-I$_{esd}$ OTAs (Fig. 4) are correctly analyzed as Type-IIa$_{esd}$ OTAs, which are described in the next section.

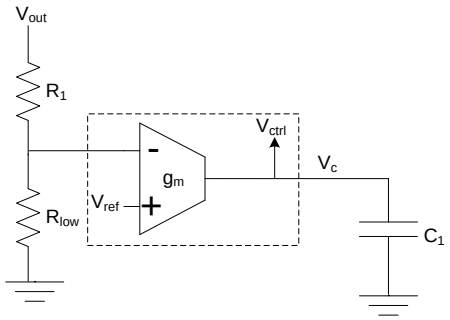

Fig. 3. Simplified Type-I OTA compensation.

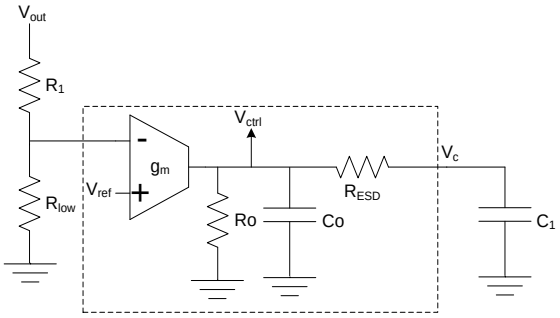

Fig. 4. Type-I$_{esd}$ compensation is correctly modeled as Type-IIa$_{esd}$.

Type-IIa$_{esd}$ OTA

The Type-II OTA compensation from the simplified OTA model shown in Fig. 5 is described in reference 1. A series combination of R_2-C_1 is placed between compensation pin V_c and ground. The corresponding OTA transfer function terms are reproduced in equations 8 through 10. Consideration for placement of a high-frequency bypass capacitor C_2 between V_c and ground will be described in a later section.

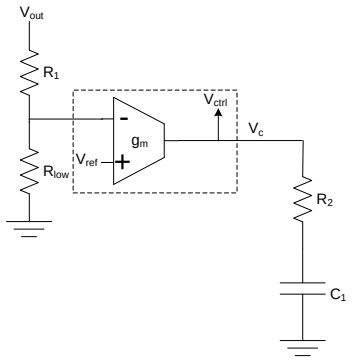

Fig. 5. Simplified Type-IIa OTA compensation model.

$$G(f) = -G_0\left(1 - j\frac{\omega_z}{2\pi f}\right) \tag{8}$$

where,

$$\omega_z = \frac{1}{R_2 C_1} \tag{9}$$

$$\omega_p = \infty \tag{10}$$

$$G_0 = \frac{R_{low}}{R_{low} + R_1} g_m R_2 \tag{11}$$

A Type-IIa$_{esd}$ OTA compensation is shown in Fig. 6. Its transfer function is described by equation 12.

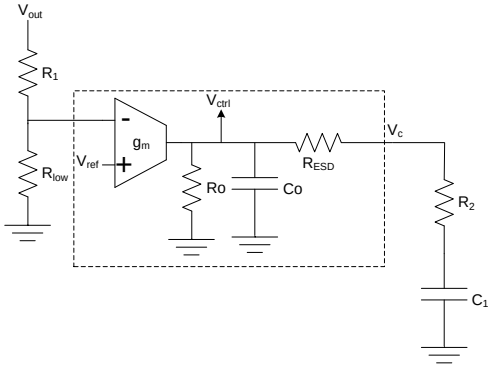

Fig. 6. Type-IIa$_{esd}$ OTA compensation.

$$G_{esd}(s) = -\left(\frac{R_{low}}{R_{low}+R_1}\right) g_m R_0 \left(\frac{1+R_{2eq}C_1 s}{R_0 R_{2eq} C_0 C_1 s^2 + \left(R_0 C_0 + \left(R_0 + R_{2eq}\right)C_1\right)s + 1}\right) \quad (12)$$

where,

$$R_{2eq} = R_2 + R_{ESD} \quad (13)$$

The zero from equation 12 is described in equation 14. By using the root extraction from equations 6 and 7, the poles described by equations 15 and 17 are determined. Given that $C_0 << C_1$ and when $R_0 >> R_{2eq}$, the poles may be further simplified to equations 16 and 18.

$$\omega_{z1esd} = \frac{1}{R_{2eq}C_1} \quad (14)$$

$$\omega_{p1esd} = \frac{1}{2}\left(\frac{R_0 C_0 + \left(R_0 + R_{2eq}\right)C_1}{R_0 R_{2eq} C_0 C_1}\right)\left(1 + \sqrt{1 - \frac{4R_0 R_{2eq} C_0 C_1}{\left(R_0 C_0 + \left(R_0 + R_{2eq}\right)C_1\right)^2}}\right) \quad (15)$$

$$\omega_{p1esd} \approx \frac{1}{2}\left(\frac{1}{R_{2eq}C_0}\right)\left(1 + \sqrt{1 - \frac{4R_{2eq}C_0}{R_0 C_1}}\right) \quad (16)$$

$$\omega_{p2esd} = \frac{1}{2}\left(\frac{R_0 C_0 + \left(R_0 + R_{2eq}\right)C_1}{R_0 R_{2eq} C_0 C_1}\right)\left(1 - \sqrt{1 - \frac{4R_0 R_{2eq} C_0 C_1}{\left(R_0 C_0 + \left(R_0 + R_{2eq}\right)C_1\right)^2}}\right) \quad (17)$$

$$\omega_{p2esd} \approx \frac{1}{2}\left(\frac{1}{R_{2eq}C_0}\right)\left(1 - \sqrt{1 - \frac{4R_{2eq}C_0}{R_0 C_1}}\right) \quad (18)$$

The Type-IIa$_{esd}$ OTA transfer function may now be expressed in the more-intuitive form of equation 19.

$$G_{esd}(f) = -G_{0esd} \frac{1 + j\frac{2\pi f}{\omega_{z1esd}}}{\left(1 + j\frac{2\pi f}{\omega_{p1esd}}\right)\left(1 + j\frac{2\pi f}{\omega_{p2esd}}\right)}. \quad (19)$$

where,

$$G_{0esd} = \frac{R_{low}}{R_{low}+R_1} g_m R_0 \quad (20)$$

As a design example, Type-IIa and Type-IIa$_{esd}$ OTA compensation transfer functions are plotted in Fig. 7 for R_2 = 2.0 kΩ, and C_1 = 33 nF.

For the Type-IIa OTA, f_z = 2.41 kHz and G_o = 0.282. For the Type-IIa$_{esd}$ OTA, f_{z1esd} = 6.26 kHz, f_{p1esd} = 6.23 MHz, f_{p2esd} = 1.61 Hz, and G_{oesd} = 422.

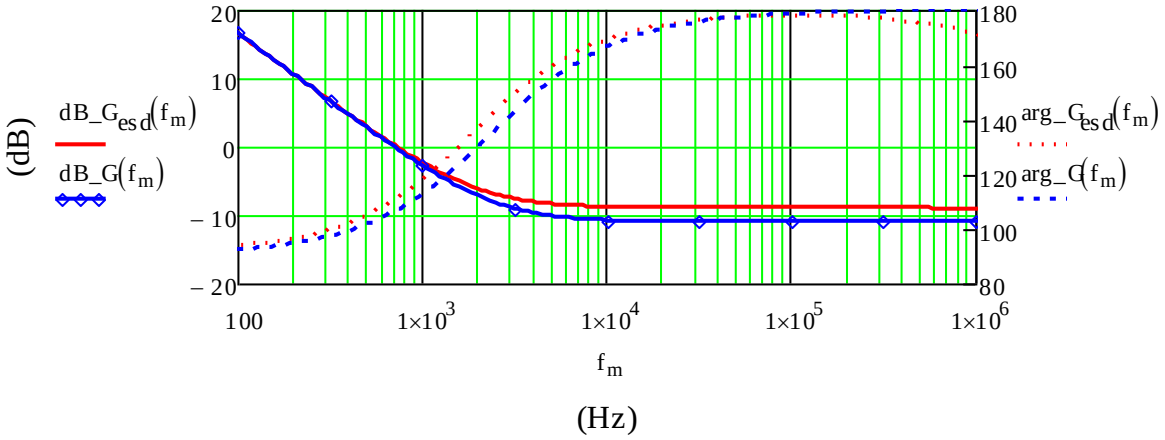

Fig. 7. Type-IIa and Type-IIa$_{esd}$ OTA response.

Type-II$_{esd}$ OTA

A Type-II OTA compensation network (Fig. 8) is implemented by adding the high-frequency bypass capacitor C_2 in parallel with the Type-IIa compensation network. Transfer function terms derived in reference 1 are reproduced in equations 21 through 24.

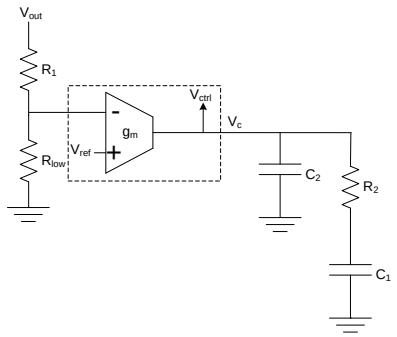

Fig. 8. Simplified Type-II OTA compensation.

$$G(f) = -G_0 \frac{1 - j\frac{\omega_z}{2\pi f}}{1 + j\frac{2\pi f}{\omega_p}} \qquad (21)$$

where,

$$\omega_z = \frac{1}{R_2 C_1} \tag{22}$$

$$\omega_p = \frac{1}{R_2\left(\frac{C_1 C_2}{C_1 + C_2}\right)} \tag{23}$$

$$G_0 = \frac{R_{low}}{R_{low} + R_1} g_m R_2 \frac{C_1}{C_1 + C_2} \tag{24}$$

By observation of the Type-II$_{esd}$ OTA compensation from Fig. 9, three independent storage capacitors are identified, resulting in a third-order polynomial transfer function in equation 25.

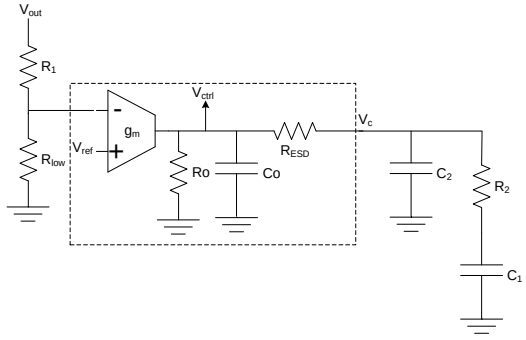

Fig. 9. Type-II$_{esd}$ OTA compensation.

$$G_{esd}(s) = -G_{0esd}\frac{1 + a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2 + b_3 s^3} \tag{25}$$

It may be shown that coefficients a_i and b_i are:

$$a_1 = R_{2eq} C_1 + R_{ESD} C_2 \tag{26}$$

$$a_2 = R_2 R_{ESD} C_1 C_2 \tag{27}$$

$$a_3 = 0 \tag{28}$$

$$b_1 = R_0 C_0 + \left(R_0 + R_{2eq}\right) C_1 + \left(R_0 + R_{ESD}\right) C_2 \tag{29}$$

$$b_2 = R_0 R_{2eq} C_0 C_1 + R_0 R_{ESD} C_0 C_2 + R_2 \left(R_0 + R_{ESD}\right) C_1 C_2 \tag{30}$$

$$b_3 = R_0 R_{ESD} R_2 C_0 C_1 C_2 . \tag{31}$$

As a design example, we select as component values R_1 = 66 kΩ, R_{low} = 10 kΩ, R_2 = 2.0 kΩ, C_1 = 33 nF, and C_2 = 470 pF. The contribution from coefficient b_3 in the frequency range of interest below ~1 MHz is negligible. Selecting b_3 = 0 reduces G(s) to a second-order expression as in equation 32. This expression may be further simplified by recognizing $R_{2eq}C_1 >> R_{ESD}C_2$, $(R_0 + R_{2eq})C_1 >> R_0C_0$, and $(R_0 + R_{2eq})C_1 >> (R_0 + R_{ESD})C_2$.

$$G_{esd}(s) = -G_{0esd} \frac{1 + a_1 s + a_2 s^2}{1 + b_1 s + b_2 s^2} \tag{32}$$

Poles, zeroes and a_i, b_i coefficients are found to be:

$$a_1 = R_{2eq} C_1 \tag{33}$$

$$a_2 = R_2 R_{ESD} C_1 C_2 \tag{34}$$

$$\omega_{z1esd} = \frac{1}{2}\left(\frac{R_{2eq}}{R_2 R_{ESD} C_2}\right)\left(1 - \sqrt{1 - \frac{4 R_2 R_{ESD} C_2}{R_{2eq}{}^2 C_1}}\right) \tag{35}$$

$$\omega_{z2esd} = \frac{1}{2}\left(\frac{R_{2eq}}{R_2 R_{ESD} C_2}\right)\left(1 + \sqrt{1 - \frac{4 R_2 R_{ESD} C_2}{R_{2eq}{}^2 C_1}}\right) \tag{36}$$

$$b_1 = \left(R_0 + R_{2eq}\right) C_1 \tag{37}$$

$$b_2 = R_0 R_{2eq} C_0 C_1 + R_0 R_{ESD} C_0 C_2 + R_2 \left(R_0 + R_{ESD}\right) C_1 C_2 \tag{38}$$

$$\omega_{p1esd} = \frac{1}{2} \frac{R_0 + R_{2eq}}{R_0 R_{2eq} C_0 + R_2 \left(R_0 + R_{ESD}\right) C_2} \left(1 - \sqrt{1 - \frac{4 R_0 R_{2eq} C_0 + R_2 \left(R_0 + R_{ESD}\right) C_2}{\left(R_0 + R_{2eq}\right)^2 C_1}}\right) \tag{39}$$

$$\omega_{p1esd} \approx \frac{1}{2}\frac{1}{R_2C_2}\left(1-\sqrt{1-\frac{R_2C_2}{R_0C_1}}\right) \tag{40}$$

$$\omega_{p2esd} = \frac{1}{2}\frac{R_0+R_{2eq}}{R_0R_{2eq}C_0+R_2\left(R_0+R_{ESD}\right)C_2}\left(1+\sqrt{1-\frac{4R_0R_{2eq}C_0+R_2\left(R_0+R_{ESD}\right)C_2}{\left(R_0+R_{2eq}\right)^2C_1}}\right) \tag{41}$$

$$\omega_{p2esd} \approx \omega_{p1esd} \approx \frac{1}{2}\frac{1}{R_2C_2}\left(1+\sqrt{1-\frac{R_2C_2}{R_0C_1}}\right). \tag{42}$$

The Type-II$_{esd}$ OTA transfer function may now be expressed as in equation 43.

$$G_{esd}(f) = -G_{0esd}\frac{\left(1+j\frac{2\pi f}{\omega_{z1esd}}\right)\left(1+j\frac{2\pi f}{\omega_{z2esd}}\right)}{\left(1+j\frac{2\pi f}{\omega_{p1esd}}\right)\left(1+j\frac{2\pi f}{\omega_{p2esd}}\right)} \tag{43}$$

where,

$$G_{0esd} = \frac{R_{low}}{R_{low}+R_1}g_mR_0 \tag{44}$$

Transfer functions *G(f)* and $G_{esd}(f)$ are plotted in Fig. 10. R_{ESD} introduces midband gain and phase errors that become pronounced above ~100 kHz.

For the Type-II OTA design example, f_{z1} = 2.41 kHz and f_{p1} = 172 kHz. For the Type-II$_{esd}$ OTA, f_{z1esd} = 1.90 kHz, f_{z2esd} = 792 kHz, f_{p1esd} = 1.61 Hz, and f_{p2esd} = 169 kHz.

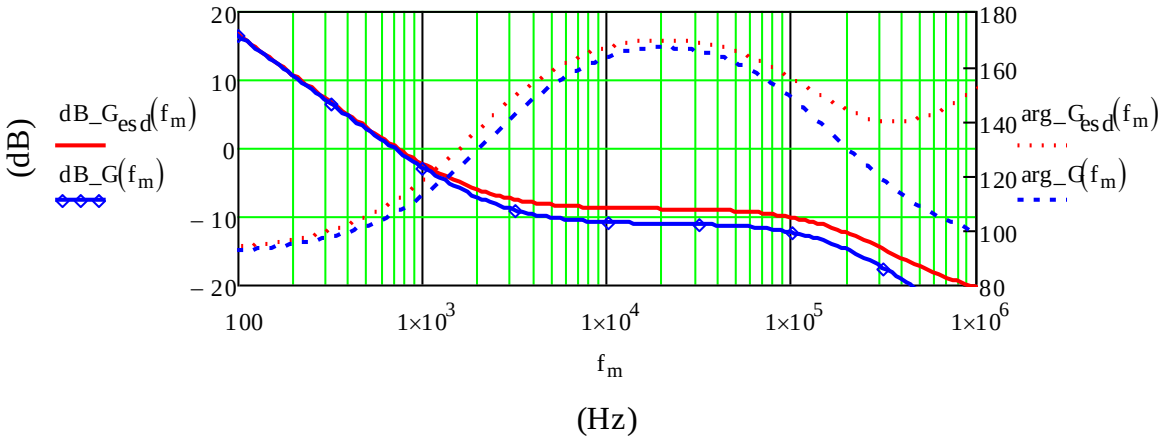

Fig. 10. Type-II and Type-II$_{esd}$ OTA response.

Type-III$_{esd}$ OTA

Type-III OTA compensation is implemented by placement of a series R_3-C_3 lead-network in parallel with input voltage divider resistor R_1 (Figs. 11 and 12). The pole and zero of the lead network are readily identifiable. The resulting zero/pole transfer function may then be multiplied by the previously derived Type-II and Type-II$_{esd}$ transfer functions.

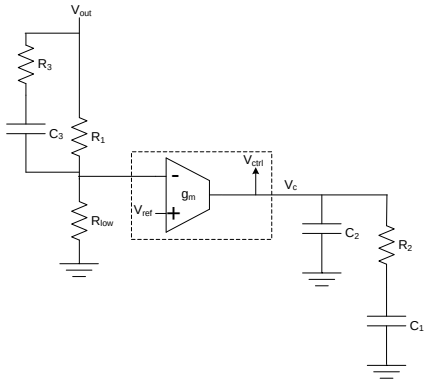

Fig. 11. Simplified Type-III OTA compensation.

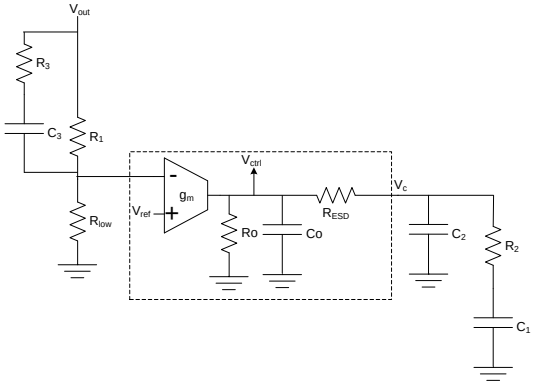

Fig. 12. Type-III$_{esd}$ OTA compensation.

It may be shown that the lead network zero and pole are defined by equations 45 and 46. The type-III transfer function is given by equation 47.

$$\omega_{z3} = \frac{1}{(R_1 + R_3)C_3} \tag{45}$$

$$\omega_{p3} = \frac{1}{\left(\frac{R_{low}R_1}{R_{low1} + R_1} + R_3\right)C_3} \tag{46}$$

$$G(f) = -G_0 \frac{\left(1 - j\frac{\omega_{z1}}{2\pi f}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1}}\right)} \frac{\left(1 + j\frac{2\pi f}{\omega_{z3}}\right)}{\left(1 + j\frac{2\cdot\pi f}{\omega_{p3}}\right)} \tag{47}$$

The type-III$_{esd}$ transfer function is similarly defined in equation 48.

$$G_{esd}(f) = -G_{0esd} \frac{\left(1 + j\frac{2\pi f}{\omega_{z1esd}}\right)\left(1 + j\frac{2\pi f}{\omega_{z2esd}}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1esd}}\right)\left(1 + j\frac{2\pi f}{\omega_{p2esd}}\right)} \frac{\left(1 + j\frac{2\pi f}{\omega_{z3}}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p3}}\right)} \tag{48}$$

For the Type-III design example, R_3 = 1 kΩ and C_3 = 47 nF are chosen for the lead network components. As a result, f_{z3} = 50.5 Hz and f_{p3} = 350 Hz are obtained.

The resulting transfer function for Type-III and Type-III$_{esd}$ OTAs are plotted in Fig. 13. The R_1, C_1, and C_2 compensation network were left unchanged to illustrate that the lead network has no influence on the error introduced by R_{ESD}. In a situation where both Type-II and Type-III compensation are under consideration, the midband gain from the Type-III compensation (Fig. 13) is ~15 dB greater than that from Type-II compensation (Fig. 10). If R_2 is further reduced to lower the Type-III midband gain, the R_{ESD}/R_2 ratio increases and the result will be an increase in divergence between the Type-IIIx and Type-IIIx$_{esd}$ transfer function gain and phase.

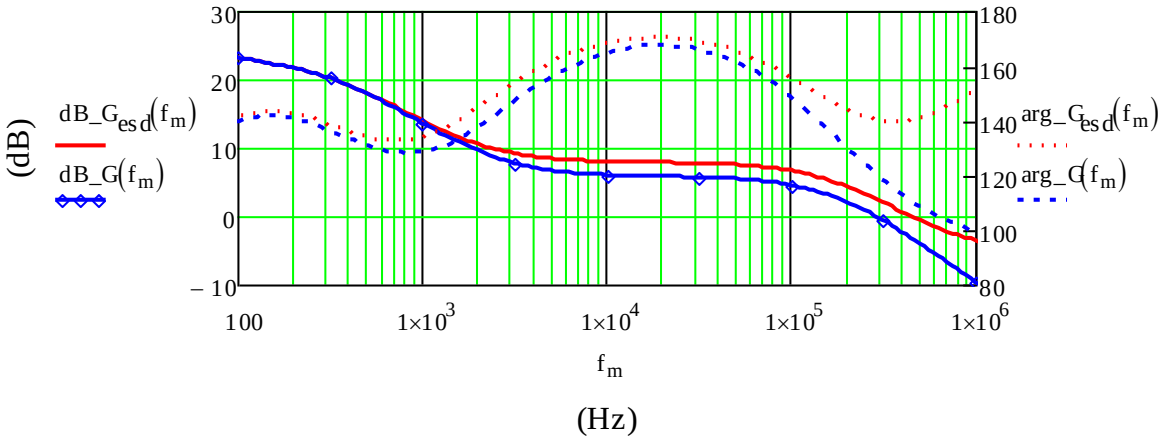

Fig. 13. Type-III and Type-III$_{esd}$ OTA response.

R_{ESD} Correction Factors

In a power supply design, feedback loop parameters are normally measured to verify gain and phase margins. When selecting the OTA pole and zero locations, the IC's internal control signal (V_{ctrl}) gain and phase behavior may be derived from empirical measurements of the response at pin V_c by multiplying the data by a frequency-dependent correction factor. The correction factor is determined by expressing the ratio of $G_{esd}(s)/G(s)$ as in equation 49 for Type-IIa and Type-IIIa compensation, or as in equation 50 for Type-II and Type-III compensation.

Correction factor curves $K_{IIa}(f)$ and $K_{II}(f)$ corresponding to the previously described Type-IIx$_{esd}$ examples are shown in Figs. 14 and 15.

$$K_{IIa}(f) = \frac{G_{oesd}}{G_o} \frac{\left(1 + j\frac{2\pi f}{\omega_{z1esd}}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1esd}}\right)\left(1 + j\frac{2\pi f}{\omega_{p2esd}}\right)} \frac{1}{\left(1 - j\frac{\omega_z}{2\pi f}\right)} \qquad (49)$$

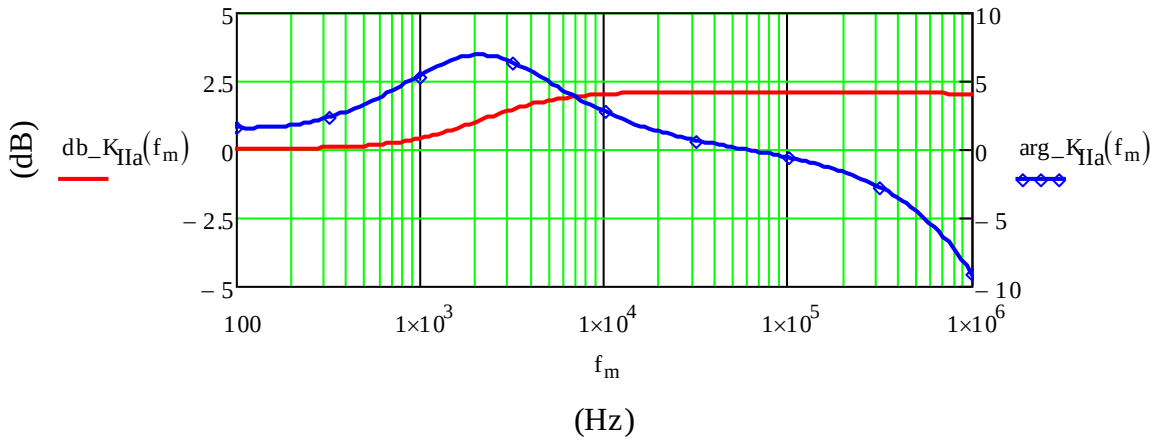

Fig. 14. Correction factor KIIa for Type-IIa (and Type-IIIa) compensation.

$$K_{II}(f) = \frac{G_{oesd}}{G_o} \frac{\left(1 + j\frac{2\pi f}{\omega_{z1esd}}\right)\left(1 + j\frac{2\pi f}{\omega_{z2esd}}\right)\left(1 + j\frac{2\pi f}{\omega_p}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1esd}}\right)\left(1 + j\frac{2\pi f}{\omega_{p2esd}}\right)\left(1 - j\frac{\omega_z}{2\pi f}\right)} \quad (50)$$

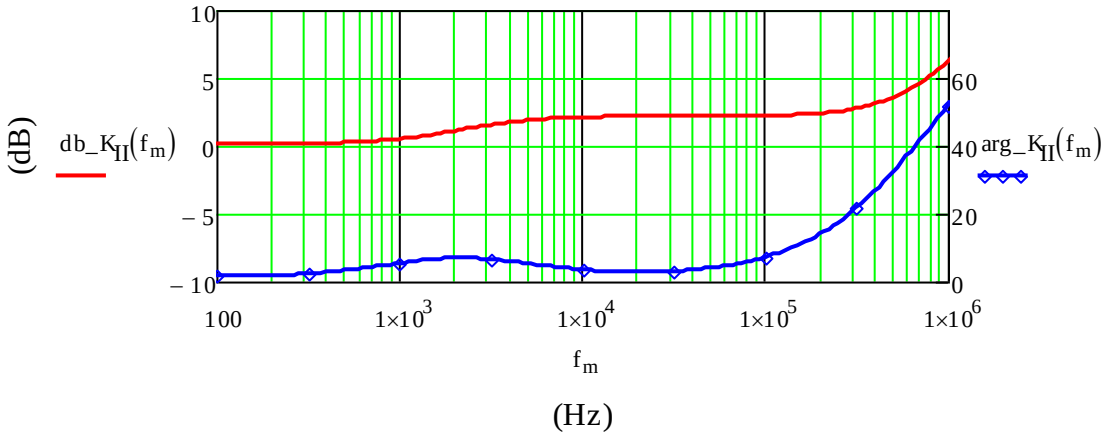

Fig. 15. Correction factor KII for Type-II (and Type-III) compensation.

Conclusion

An OTA model inclusive of an output series ESD protection resistance was described. Power supply Type-I compensation has been shown to be correctly modeled as Type-IIa compensation. Transfer functions for Type-II and Type-III compensation were also derived.

The mid-band and high-frequency gain and phase errors due to the absence of R_{ESD} in the ideal OTA model may become pronounced in low-input-voltage applications where the compensation gain does not benefit from a significant attenuation by the feedback input voltage divider. Correction factors were introduced to derive the representation of the feedback control transfer function from empirical measurements.

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About The Author

Alain Laprade received an MEng in electrical engineering from McGill University in Montréal in 1984. Since then he has worked in power supply development for commercial, telecommunication, automotive, and aerospace applications and as an applications engineer. In 2010, he relocated to Rhode Island to join ON Semiconductor's Analog Power Group New Product Development team.

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