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Current-Mode Control Stability Analysis For DC-DC Converters (Part 2)

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In this article, part 2 of 2, we discuss current-mode control loop compensation[1] for industrial and automotive applications. Starting from the small-signal model, simple expressions are derived that yield an intuitive procedure for designing the compensator for a current-mode-controlled buck converter. Even with an error amplifier of finite gain-bandwidth, the simplicity and convenience of this design procedure makes it viable for everyday use by the practicing power electronics engineer.

To bolster the theoretical analysis, an actual design example based on a commercially available PWM regulator is presented here with simulation used to verify the results obtained from the aforementioned design procedure. This discussion assumes some understanding of current-mode control and how it's modeled. For those who want to review current-mode operation and small-signal modeling, check out Part 1 again.[1]

Compensator Transfer Function

A type-II compensator using an error amplifier (EA) with transconductance, g_m, is shown in Fig. 1.

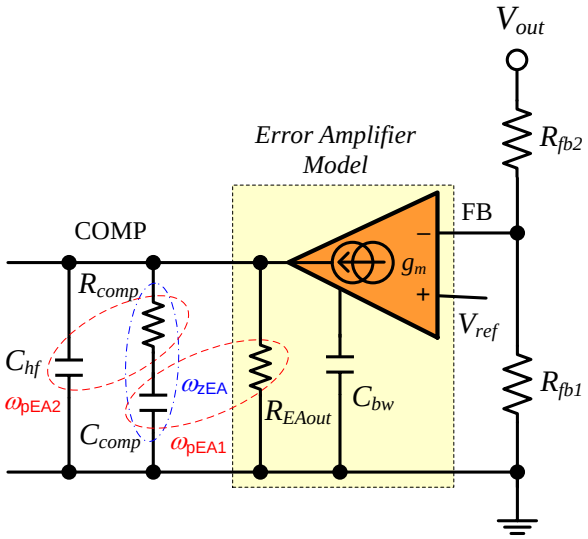

Fig. 1. Small-signal representation of an operational transconductance EA. The component combinations representing two poles and one zero are circled.

The dominant pole of the EA open-loop gain characteristic is set by the EA output resistance, R_{EAout}, and the effective bandwidth-limiting capacitance, C_{bw}, as in equation 1:

$$G_{EA(openloop)}(s) = -\frac{g_m R_{EAout}}{1 + sR_{EAout}C_{bw}} \quad . \qquad (1)$$

The influence of any EA high-frequency poles, whether parasitic or included by design, is neglected in the above expression. The compensator transfer function from output voltage to COMP, including the gain contribution from the feedback resistor divider network, is given by

$$G_c(s) = \frac{\tilde{v}_{comp}(s)}{\tilde{v}_{out}(s)} = -A_{fb} g_m Z_{EAout}(s) \qquad (2)$$

with

$$Z_{EAout}(\mathrm{s}) = g_m R_{EAout} \left\| \left(R_{comp} + \frac{1}{\mathrm{s}C_{comp}} \right) \right\| \frac{1}{\mathrm{s}C_{hf}} \left\| \frac{1}{\mathrm{s}C_{bw}} \right. \tag{3}$$

and the feedback attenuation factor is

$$A_{fb} = \frac{V_{ref}}{V_{out}} = \frac{R_{fb1}}{R_{fb1} + R_{fb2}}. \tag{4}$$

Evaluating equation 3 gives an expression of the form

$$Z_{EAout}(\mathrm{s}) = R_{EAout} \frac{1 + \mathrm{s}/\omega_{\mathrm{zEA}}}{1 + \left(\mathrm{s}/\omega_{p\mathrm{EA1}}\right) + \left(\mathrm{s}^2/\omega_{\mathrm{pEA1}}\omega_{\mathrm{pEA2}}\right)}. \tag{5}$$

As ω_{pEA1} and ω_{pEA2} are well separated in frequency, the low-Q approximation applies and equation 5 becomes

$$Z_{EAout}(\mathrm{s}) = R_{EAout} \frac{1 + \dfrac{\mathrm{s}}{\omega_{\mathrm{zEA}}}}{\left(1 + \dfrac{\mathrm{s}}{\omega_{\mathrm{pEA1}}}\right)\left(1 + \dfrac{\mathrm{s}}{\omega_{\mathrm{pEA2}}}\right)} \tag{6}$$

where

$$\omega_{\mathrm{zEA}} = \frac{1}{R_{comp}C_{comp}};$$

$$\omega_{\mathrm{pEA1}} \cong \frac{1}{R_{EAout}\left(C_{comp} + C_{hf} + C_{bw}\right)} \cong \frac{1}{R_{EAout}C_{comp}}; \text{ and} \tag{7}$$

$$\omega_{\mathrm{pEA2}} \cong \frac{1}{R_{comp}\left(C_{comp} \left\| \left(C_{hf} + C_{bw}\right)\right.\right)} \cong \frac{1}{R_{comp}C_{hf}}.$$

Typically, $R_{comp} << R_{EAout}$, $C_{comp} >> \left(C_{hf} + C_{bw}\right)$ and the approximations set forth in equation 7 are valid. Circled in Fig. 1 are the components to provide two compensator poles and one compensator zero. Fig. 2 gives an example of the typical frequency response of both the open-loop EA and the compensator.

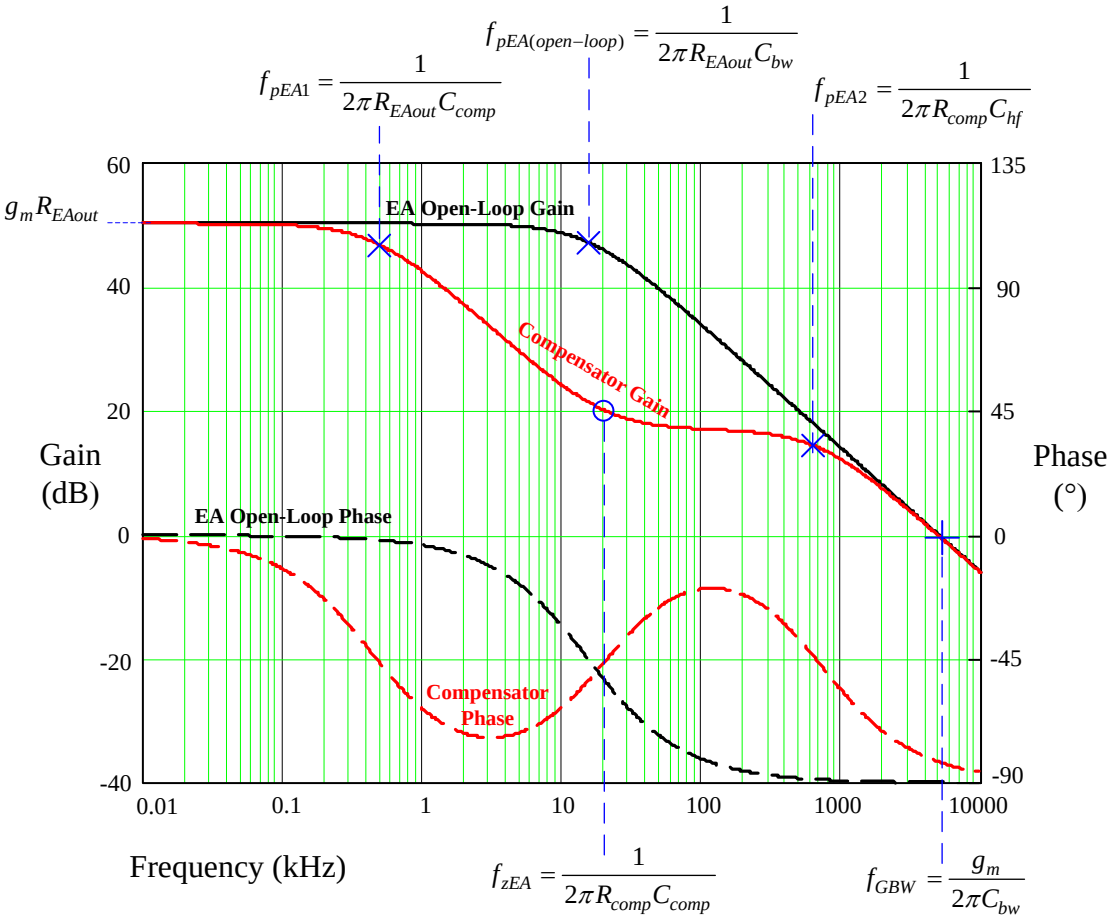

Fig. 2. Small-signal frequency responses of open-loop EA and compensator.

In this example, the feedback attenuation is unity, and the EA has 50 dB of open-loop dc gain and a 5-MHz bandwidth. Again, the poles and zeros are denoted with **x** and **o** symbols, respectively, and a **+** symbol indicates the EA bandwidth. Not included in the phase plots is the 180° phase lag contribution related to the EA in the inverting configuration.

Compensator pole ω_{pEA1} appears at very low frequency and is easily replaced by an integrator term. The compensator transfer function simplifies to

$$G_c(s) = -\frac{A_c}{s}\frac{1+\frac{s}{\omega_{zEA}}}{1+\frac{s}{\omega_{pEA}}} \qquad (8)$$

where the integrator gain term, A_c, is given by

$$A_c = \frac{g_m}{C_{comp}} A_{fb}\,. \qquad (9)$$

Note that both feedback resistors, R_{fb1} and R_{fb2}, factor into the control-loop gain when a transconductance-type EA is used. In contrast, if an operational amplifier-type EA is employed, the FB node is effectively at ac ground and the lower feedback resistance bears no influence on the loop dynamics.

Compensator Design

A frequently used compensation strategy that generally applies to peak, valley, and emulated current-mode circuits is to equate the control-to-output transfer function to the compensator transfer function term-by-term to attain a single-pole (–20 dB/decade) roll off of the loop response. To demonstrate, consider

- one compensator pole, ω_{pEA1}, positioned to provide high gain in the low-frequency range, minimizing output steady-state error for best load regulation;
- one compensator zero located to offset the dominant load pole, $\omega_{zEA} = \omega_{p,}$ which typically is the minimum load resistance (maximum load current) condition used; and
- one compensator pole positioned to cancel the output capacitor ESR zero, $\omega_{pEA2} = \omega_{esr}$.

The loop gain is expressed as the product of the control-to-output and compensator transfer functions. From equation 5 in part 1 and equation 8, the loop gain is

$$T(\mathrm{s}) = G_c(\mathrm{s})G_v(\mathrm{s}) = -\frac{A_c\left(1+\dfrac{\mathrm{s}}{\omega_{\mathrm{zEA}}}\right)}{\mathrm{s}\left(1+\dfrac{\mathrm{s}}{\omega_{\mathrm{pEA}}}\right)}\,\frac{A_{dc}\left(1+\dfrac{\mathrm{s}}{\omega_{esr}}\right)}{\left(1+\dfrac{\mathrm{s}}{\omega_p}\right)\left(1+\dfrac{\mathrm{s}}{Q\omega_{\mathrm{n}}}+\dfrac{\mathrm{s}^2}{\omega_n^2}\right)}. \quad (10)$$

Select the crossover frequency $\omega_c = 2\pi f_c$ (where the loop gain is 0 dB) between one-tenth and one-fifth of the switching frequency. If $\omega_{zEA} = \omega_p$ and $\omega_{pEA} = \omega_{esr}$, the loop gain reduces to

$$T(\mathrm{s}) \approx -\frac{A_c A_{dc}}{\mathrm{s}\left(1+\dfrac{\mathrm{s}}{Q\omega_{\mathrm{n}}}+\dfrac{\mathrm{s}^2}{\omega_n^2}\right)}. \quad (11)$$

Assuming a well-designed current loop ($0.5 \le Q \le 1$), the sampling gain contribution is insignificant at frequencies up to the crossover frequency. This assumption precludes the case where too much slope-compensating ramp is added. The magnitude of the loop gain at the dominant pole frequency is

$$\left|T\left(j\omega_p\right)\right| = \left|T\left(j\omega_{\mathrm{zEA}}\right)\right| \approx A_c A_{dc} R_{comp} C_{comp} = g_m A_{fb} A_{dc} R_{comp}. \quad (12)$$

Using basic Bode plot principles, it is apparent that

$$\left|T\left(j\omega_p\right)\right| \approx \frac{\omega_c}{\omega_p}. \quad (13)$$

Thus derived, a straight-forward solution for the crossover frequency is

$$f_c = f_p g_m A_{fb} A_{dc} R_{comp}. \quad (14)$$

Finally, compensator component values are calculated sequentially as

$$R_{comp} = \frac{1}{g_m A_{fb} A_{dc}} \frac{f_c}{f_p}$$

$$C_{comp} = \frac{5}{\omega_c R_{comp}}$$

$$C_{hf} = \frac{1}{\omega_{esr} R_{comp}} - C_{bw} \qquad (15)$$

$$R_{fb1} = R_{fb2}\left(\frac{V_{out}}{V_{ref}} - 1\right) \quad .$$

The compensator zero is positioned at one-fifth of the target crossover frequency. An initial value is selected for R_{fb2} based on a practical minimum current level flowing in the divider chain. Note that the compensation zero frequency represents the dominant time constant in a load-transient response. A large C_{comp} capacitor is thus antithetical to a fast transient response settling time. C_{comp} is adjusted mainly to tradeoff phase margin and settling time. A phase margin target of 50° to 60° is ideal. Furthermore, a smaller compensation capacitance is advantageous, if the transconductance EA has a low output-drive-current capability.

Compensator Design Example

The circuit operating conditions, key component values and control circuit parameters for the LM21305 peak-current-mode synchronous-buck PWM regulator[2] are specified in the Table. A switching frequency of 400 kHz provides a suitable tradeoff of efficiency versus size.[3]

Table. Buck converter parameters for a peak-current-mode synchronous-buck PWM regulator (LM21305).

V_{in}	8 V to 18 V	f_s	400 kHz	C_{bw}	38 pF
V_{out}	5 V	R_{dc}	36 mΩ	V_{slope}	0.462 V
I_{out}	5 A	R_{esr}	7 mΩ	S_e	0.185 V/μs
D	0.43	R_i	115 mΩ	S_n	0.245 V/μs
L_f	3.3 μH	R_{EAout}	430 kΩ	m_c	1.754
C_{out}	100 μF	g_M	2.4 mS	Q	0.641

With 12-V nominal input, the relevant gains and corner frequencies are calculated using expressions from part 1 as

$$K_{\mathrm{M}} = \frac{1}{(0.5-D)R_i\frac{T_s}{L_f}+\frac{V_{slope}}{V_{in}}} = \frac{1}{(0.5-0.43)(115\mathrm{m}\Omega)\frac{2.5\mu\mathrm{s}}{3.3\mu\mathrm{H}}+\frac{0.462\mathrm{V}}{12\mathrm{V}}} = 22.4$$

$$A_{dc} = \frac{K_{\mathrm{M}}R_{out}}{R_{out}+R_{dc}+R_s+K_{\mathrm{M}}R_i} = \frac{(22.4)(1\Omega)}{1\Omega+36\mathrm{m}\Omega+(22.4)(115\mathrm{m}\Omega)} = 6.19 \qquad (16)$$

$$f_p = \frac{1}{2\pi C_{out}\left(R_{out}\left\|K_{\mathrm{M}}R_i\right.\right)} = \frac{1}{2\pi(55\mu\mathrm{F})\left[1\Omega\left\|\left((22.4)(115\mathrm{m}\Omega)\right)\right.\right]} = 4.01\mathrm{kHz}$$

$$f_{esr} = \frac{1}{2\pi R_{esr}C_{out}} = \frac{1}{2\pi(7\mathrm{m}\Omega)(55\mu\mathrm{F})} = 413\mathrm{kHz}$$

.

If the output capacitor is ceramic, a capacitance derating for applied voltage is necessary. In these calculations, a derating of 45% is used. Given a target crossover frequency of 60 kHz, using the equations in 15, the compensation component values are found as

$$R_{comp} = \frac{1}{g_m A_{fb}A_{dc}}\frac{f_c}{f_p} = \frac{1}{2.4\mathrm{mS}\left(\frac{0.598\mathrm{V}}{5\mathrm{V}}\right)(6.19)}\frac{60\mathrm{kHz}}{4.01\mathrm{kHz}} = 8.4\mathrm{k}\Omega$$

$$C_{comp} = \frac{5}{\omega_c R_{comp}} = \frac{5}{2\pi(60\mathrm{kHz})(8.4\mathrm{k}\Omega)} = 1.6\mathrm{nF}$$

$$C_{hf} = \frac{1}{\omega_{esr}R_{comp}} - C_{bw} = \frac{1}{2\pi(413\mathrm{kHz})(8.4\mathrm{k}\Omega)} - 38\mathrm{pF} = 8\mathrm{pF} \qquad (17)$$

$$R_{fb1} = R_{fb2}\left(\frac{V_{out}}{V_{ref}}-1\right) = 10\mathrm{k}\Omega\left(\frac{5\mathrm{V}}{0.598\mathrm{V}}-1\right) = 73.6\mathrm{k}\Omega$$

.

Fig. 3 shows Mathcad-derived loop gain and phase plots for the example converter. The equivalent plots with an ideal EA are also shown with dashed lines. (The nonideal EA has a bandwidth-limiting capacitance, C_{bw}, which appears in parallel with C_{hf} as shown above in Fig. 1.) The phase margin (PM or ϕ_M) is the difference between the loop phase and −180° (EA inversion phase lag contribution not included). Note that if C_{hf} is not installed, the EA itself provides high-frequency attenuation by virtue of its finite gain-bandwidth.

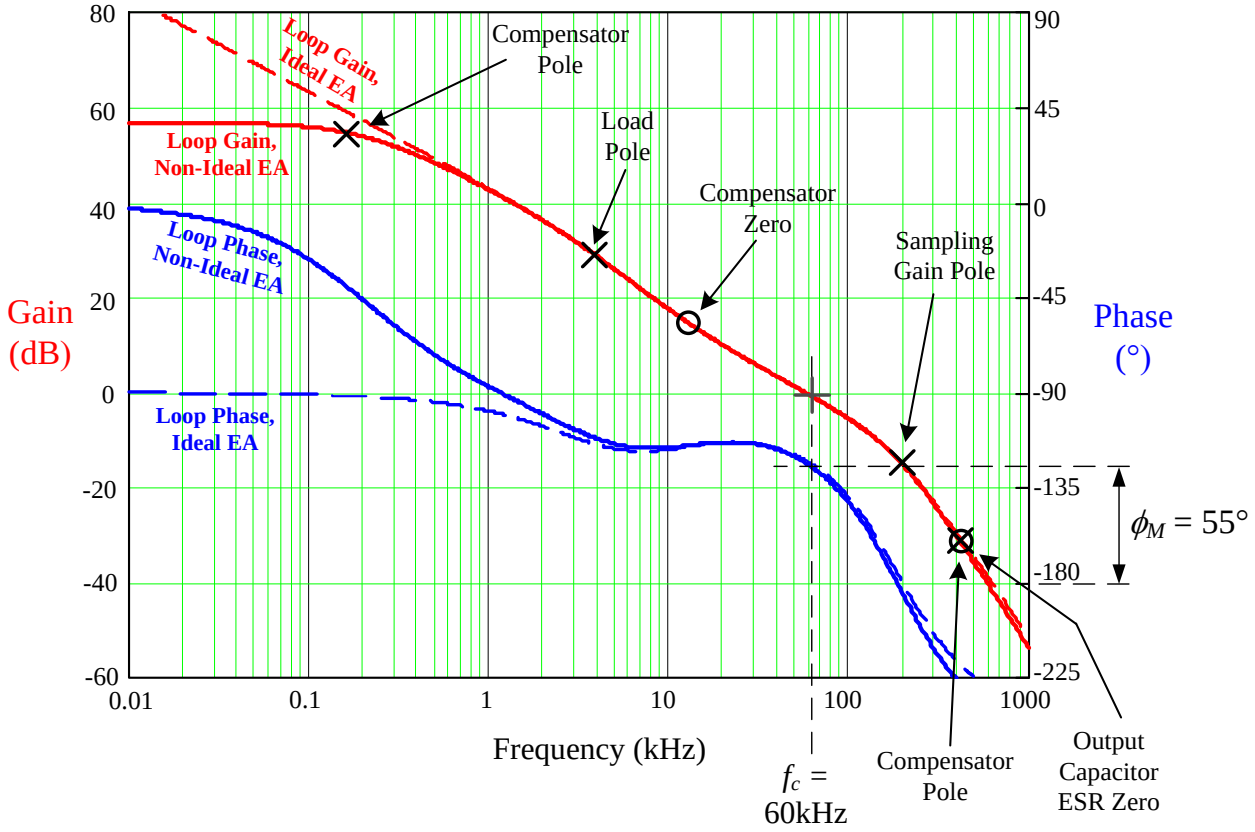

Fig. 3. Buck converter loop gain and phase plots based on the LM21305.

Control Loop Simulation

Using an LM21305 PWM regulator in a buck converter configuration per Table 1, a SIMetrix/SIMPLIS[4] switching model circuit simulation is run to substantiate the just-completed analysis. Fig. 4 presents the model schematic.

The loop gain $T_V(s)$ of the system is measured by breaking the loop at the upper feedback resistor, injecting a variable-frequency oscillator signal, and analyzing the frequency response. The element with reference designator X1 in Fig. 4 is the SIMPLIS clock edge trigger to find the circuit's periodic operating point (POP) before running the ac analysis.

POP analysis works on the full nonlinear switching time-domain model of the circuit and enables subsequent ac or transient analyses. The ac source with reference designator V_{inj} in Fig. 4 is the input stimulus for the ac sweep and its amplitude is automatically controlled to keep the ac response in the linearized small-signal region. Fig. 5 illustrates a Bode plot simulation result that aligns closely with the analytical result in Fig. 3.

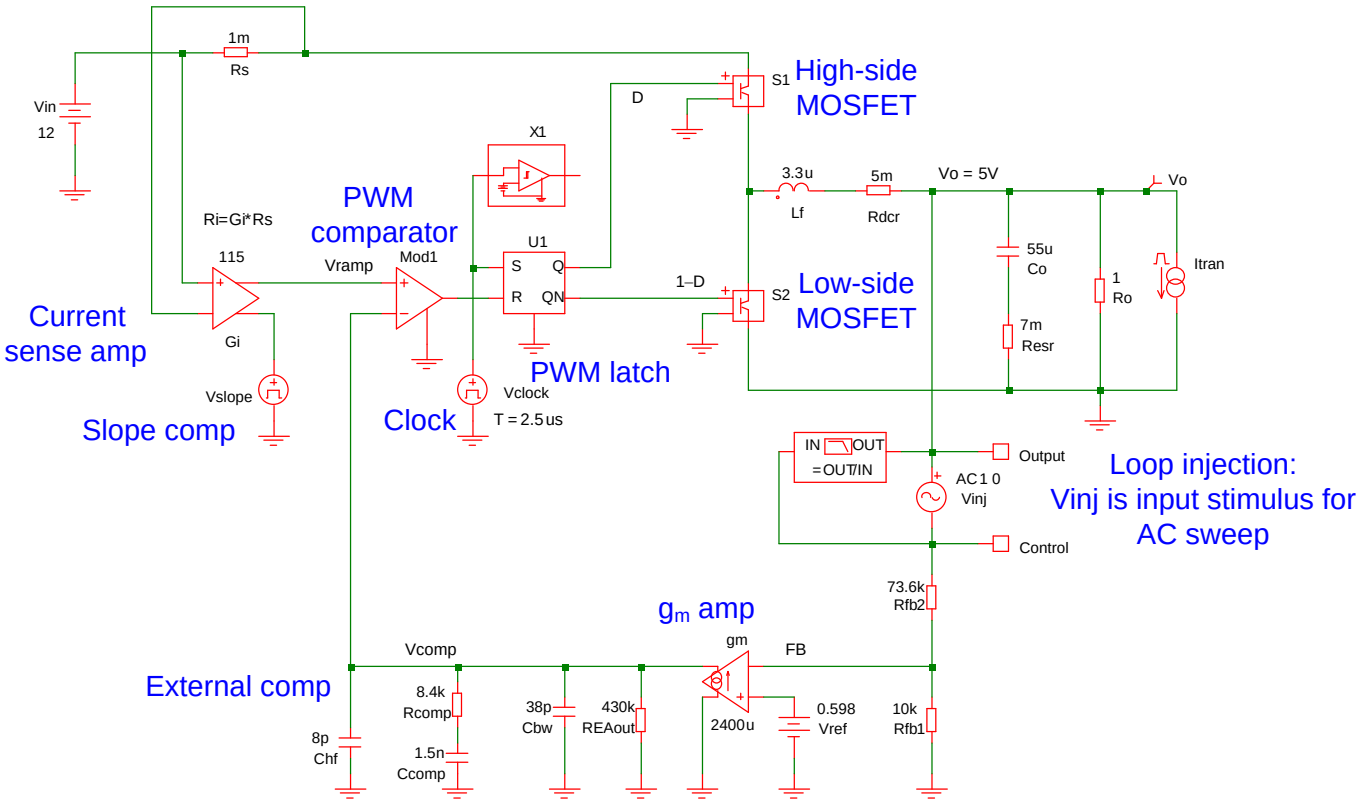

Fig. 4. SIMPLIS ac and transient analysis simulation schematic for the LM21305-based buck converter.

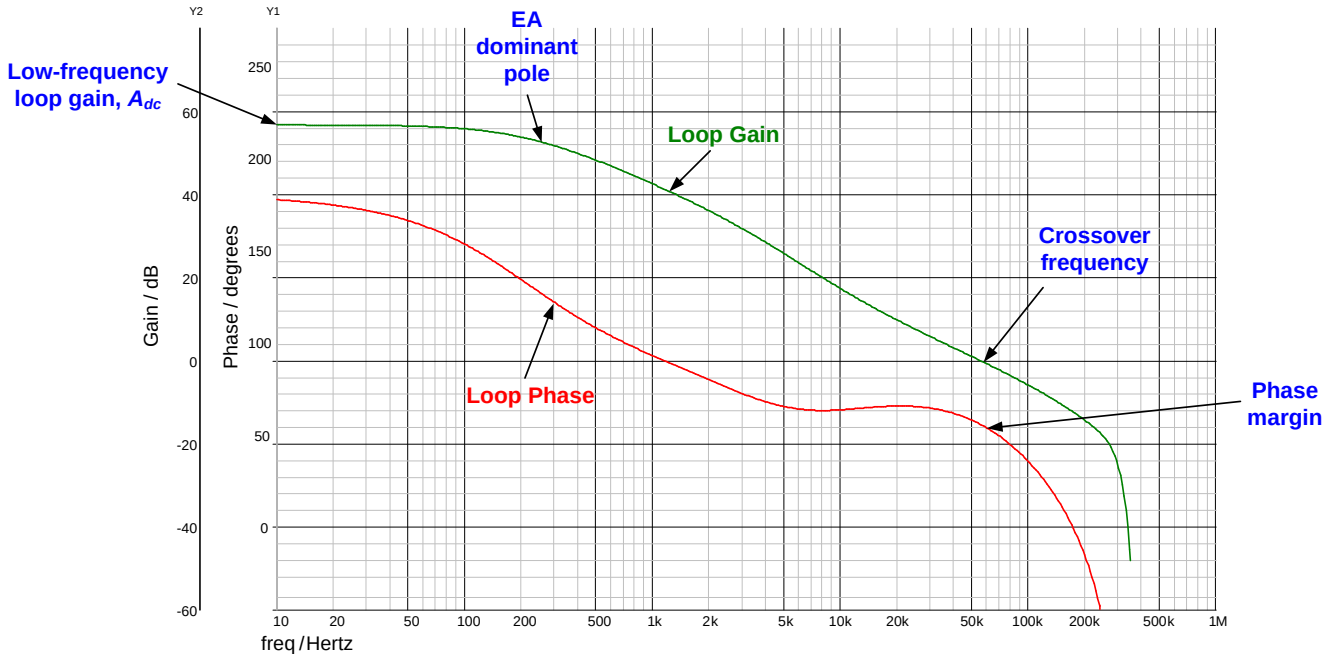

Fig. 5. Results of Bode plot simulation.

Using a SIMPLIS time-domain transient analysis, load-on and load-off transient responses are obtained (see Fig. 6) with high (3.9 nF) and low (1.5 nF) compensation-capacitor values chosen so that the compensator zero is

located directly at the load pole and the power stage resonant frequencies, respectively. The load step is from 50% to 100% full load at 1 A/μs. It is evident that the lower compensation capacitance results in a much more favorable settling time. Interestingly, this is achieved with very little relative change in the Bode plot—approximately 1-kHz decrease in crossover frequency and 4° less phase margin using the 1.5-nF capacitor.

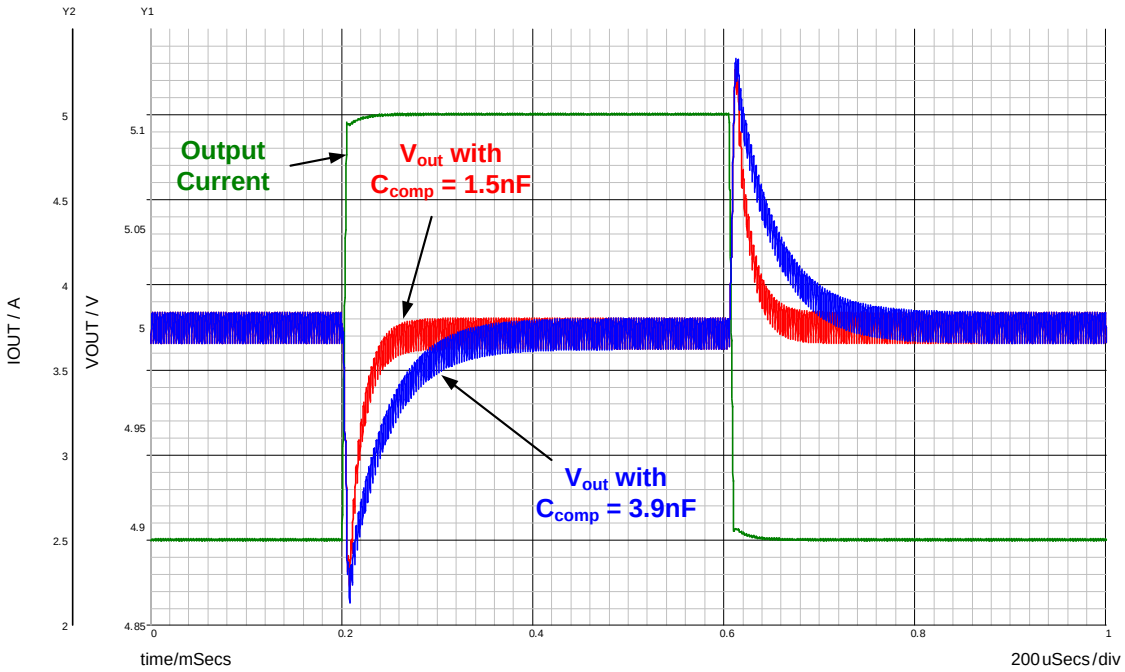

Fig. 6. Load-step transient response simulation with 1.5-nF and 3.9-nF compensation capacitance.

Conclusion

Simple expressions for current-mode control yield an easy and straightforward outline for compensating a buck converter. Understanding the frequency-domain Bode plot information helps to optimize the time-domain load transient response waveform. The reader is encouraged to consider the application to other peak-current-mode-controlled converter topologies like boost or flyback, and to consult works such as reference 5, which provide further background and analysis of current-mode control.

References

1. "Current-Mode Control Stability Analysis For DC-DC Converters (Part 1)," by Timothy Hegarty, How2Power Today, June 2014 issue.

2. LM21305 5-A Current-Mode Synchronous Buck Regulator EVM.

3. "The Buck Regulator Efficiency/Size Tradeoff Dilemma," Power House, Texas Instruments, December 2, 2013.

4. SIMetrix/SIMPLIS simulation software.

5. "Current-Loop Control In Switching Converters," by Dennis Feucht, How2Power Today, September 2011 through March 2012 issues. After reviewing the history of current-loop control theory (i.e. how to accurately model current-mode control), this article series attempts to clarify established concepts, identify problems with the existing theories or models of current-mode control, and offer what might be the first truly unified model of current control.

About The Author

Timothy Hegarty is a systems engineer with the Texas Instruments Silicon Valley Analog group. He received his bachelor's and master's degrees in electrical engineering from University College Cork, Ireland. His area of interest is integrated PWM switching regulators and controllers for wide input voltage range industrial and automotive applications. He is a member of the IEEE Power Electronics Society. You can reach Tim at ti_timhegarty@list.ti.com.

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