ISSUE: February 2015

Choose The Right Regulator For The Right Job (Part 1): Regulator Control Schemes

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It can be a daunting task for an engineer, who is responsible for all aspects of a complex board, to choose the optimum regulator for a particular point of load. Several suppliers offer very good solutions, but that does not assure you of obtaining the right regulator for a particular application.

For example, a power IC designed for an automotive application may not be a good choice for a consumer product. Portable power applications present a unique set of challenges as the processing power increases while the battery runtime decreases. Equipment with sensitive RF circuitry and low-noise analog front-ends (AFEs) provides an even greater challenge when using switching regulators. In ultrasound equipment where low-level reflected signals from the body are processed, a frequency sync input may be a hard and fast requirement to control the power-supply switching harmonics.

In higher-current applications efficiency is often the most important requirement. Ultimately, an engineer must decide what power features are critical to the application and then select a regulator designed for those requirements.

This article is part 1 of a three-part series on power regulators. Here we begin with a brief review of the importance of duty cycle and load usage. We then move to the main focus of the discussion, regulator control schemes, their types, critical parameters, and compensation schemes. We will finish with a short description of internal versus external FETs.

In the follow-up part 2 article, we will discuss other control methods besides voltage mode (VM) and current mode (CM) control. These include constant on-time, hysteretic, and pulse-frequency modulation (PFM) control schemes. We will also explain how to select these regulator types for an application. In our concluding part 3 article, we close with how to select and simulate the optimal regulator for an application.

The Devil Is In The Details

When choosing regulators for portable applications, the duty cycle and load usage are important details. Load usage refers to how the loads behave. Under normal operation, are the loads constant? Do they vary frequently between minimum and maximum full-scale currents? The duty-cycle operation of the application is the ratio of how long the equipment is active to the time that it spends in an idle or low-current state.

Why is all this important? Let's look at some details. Load usage is important as it helps determine the required quiescent current (I_Q). For example, does the regulator spend most of its time fully loaded? Then choosing a regulator with ultra-low I_Q may not be the most important specification, especially if the average load current is substantially higher than the regulator's rated I_Q. If this is the case and the operation duty cycle is low, and if the regulator's output is not a keep-alive voltage and can be shut down during idle and sleep modes, then choosing a regulator with low shutdown current may be more important.

If, on the other hand, the duty cycle is low and the regulator must be kept on, then selecting a regulator with low I_Q in a battery-operated product is important. Additionally, if the regulator during normal operation spends as much time servicing light loads as it does servicing full loads, then ultra-low operating current is very important for optimizing its efficiency and battery runtime.

Choosing The Control Scheme

Regulator control schemes play a very important role in your decision. To complicate matters, there are several types of regulator control schemes. Hysteretic or PFM schemes are typically used where efficiency needs to be optimized at light loads. On the other hand, pulse-width modulation (PWM) schemes are needed when lower output noise is required because these converters operate at fixed frequencies and are, therefore, easier to

filter. PWM contrasts with PFM in which the switching frequencies decrease when lightly loaded, while the switching frequency increases when load current increases.

Some regulators offer dual-mode operation, thus switching between PWM and skip operation modes. In skip mode overall power efficiency improves at light loads versus using PWM mode. Fig. 1 is a typical efficiency plot for a switching regulator, here the MAX15053, operating in skip mode. Note that the typical operating current is 1.53 mA. Therefore, if the application's operation duty cycle is low and the load currents are close to their maximum, this switching regulator is a good choice for a portable application.

There is a caveat—this is all accurate as long as the regulator can be placed in shutdown during idle states. However, whenever the operation duty cycle is low and the regulator is always on during idle and sleep states, then a stepdown regulator with lower operating current is more appropriate. Fig. 1 also shows that the operating current for the MAX1556 stepdown regulator in skip mode is typically 16 µA. A side-by-side efficiency comparison between these two parts reveals that the MAX1556 would be a better choice to extend battery runtime if the regulator must be active 100% of the time while the system is powered on.

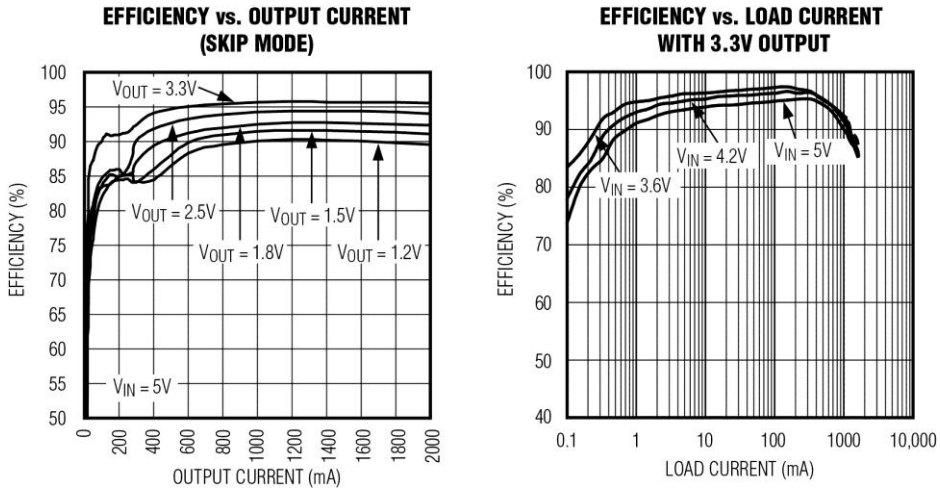

Fig. 1. Efficiency for the MAX15053 switching regulator (left) versus the MAX1556 stepdown regulator (right). Data shows that the MAX1556 would be a better choice for always-on power in standby mode.

Standby current is important for portable applications, and the regulator search can be simplified by using the suppliers' website parametric search tool (Fig. 2.) By selecting a few key parameters, such as internal switch, minimum voltage input, maximum voltage input, and I_{CC}, it is relatively easy to sort through many part options and quickly select the right regulator for the application.

In the example below, the minimum and maximum input voltage were set and the internal switch box checked. The design engineer can set the I_{CC} slider to the lowest setting offered. Now the designer sees the two best matches among all the parts.

Fig. 2. Parametric search tool used to narrow the down the choices.

Current-Mode Versus Voltage-Mode Control

Let's now spend some time examining the two control methods available for PWM switching regulators: voltage mode (VM)[2,4] and current mode (CM).[1,2,3]

The CM regulator uses the inductor current as part of the feedback loop in addition to the voltage feedback loop. The inductor current and the output-voltage-error signal are input signals to the PWM modulator. Fig. 3 shows a simplified schematic of peak CM control, where the peak inductor current is controlled along with the output voltage. The inductor current is sensed by some means and compared to a control voltage, V_C, which is derived from the output voltage error. Slope compensation is needed for CM control to prevent subharmonic oscillations for duty cycles greater than 50%.

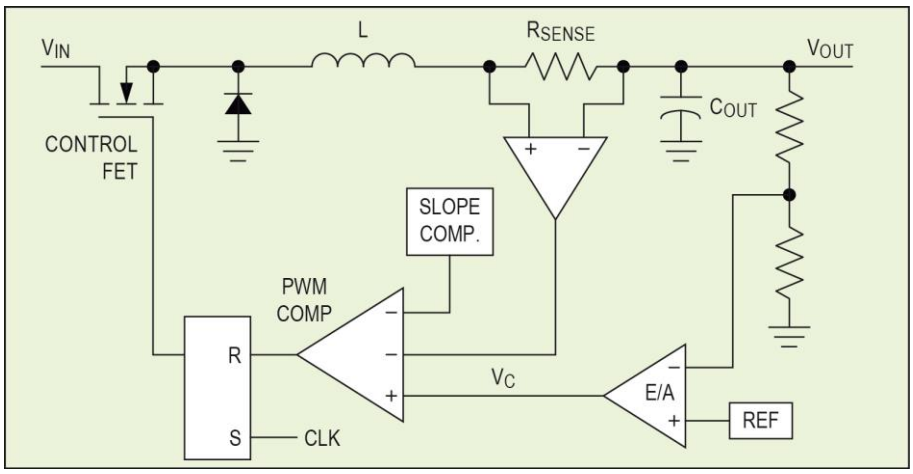

Fig. 3. Current mode (CM) control.

Voltage-mode control has been used for a long time since the first switching regulator designs became available. Voltage mode has a single voltage feedback path; PWM is performed by comparing the voltage error signal with a constant ramp waveform. Fig. 4 shows this basic configuration.

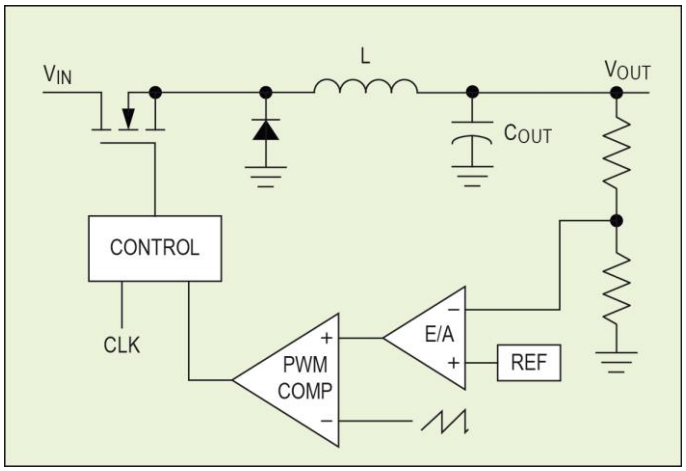

Fig. 4. Voltage-mode (VM) control.

Advantages of CM Control

So let's briefly dig into the advantages and disadvantages of both methods, starting with the CM topology.

Why current mode? In taking a closer look at the current control-loop response we find that when the control FET is on, the current through R_{SENSE} provides a voltage ramp from the output of the current-sense amp. The voltage ramp is proportional to the ramp current in the inductor. This slope-compensated voltage ramp is then compared to the output of the error amp.

The control FET will be on until the voltage sensed from the inductor current equals the control voltage, V_C. When these two voltages are equal, the control FET is turned off. The next switching cycle is started by setting the RS flip-flop from a fixed-frequency clock signal shown in Fig. 3. So, basically the voltage control loop determines the level at which the current loop regulates the peak current through the control FET switch and inductor.

Without drilling down into the math, CM control eliminates the inductor pole and second-order characteristic found in VM control because the inner-current control loop includes the output filter inductor. The outer voltage control loop, therefore, only has the single pole of the output filter and load resistance. You can think of a CM converter as a current source, supplying and regulating current to a single pole formed by the output capacitor in parallel with the load impedance at frequencies below the current-loop bandwidth. What does all this mean? Basically, it means that compensating a CM controller for stability is a lot easier than doing it with a VM controller.

Now let's talk about compensation schemes. Fig. 5 illustrates the difference between the two typical compensation networks used in these two control schemes. Voltage-mode compensation[4] (Type III) on the left requires a more complex compensation network than the current-mode compensation (Type II)[5] on the right where C2 may not even be needed.

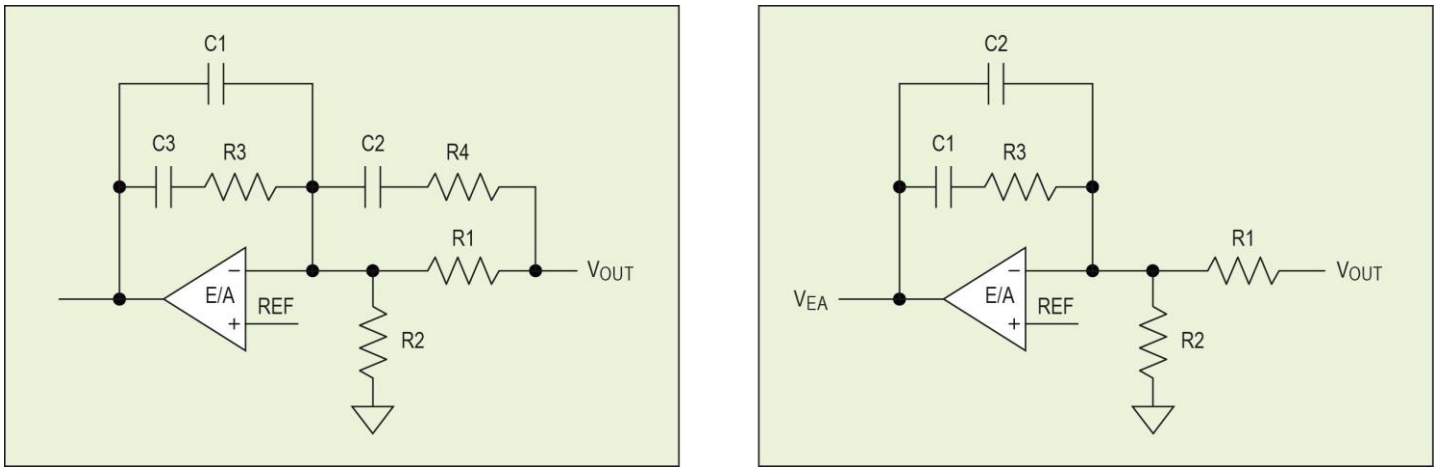

Fig. 5. Schematics showing VM compensation (left) versus CM compensation (right). With CM compensation, C2 may not be needed.

One of the disadvantages early on of the CM control scheme was that it required accurate current sensing[2] which, in turn, caused a slight power loss in the sensing element. Today's integrated power solutions eliminate the need for external current-sense resistors; the current sensing is performed internally by using the R_{DSON} of the high-side FET. In addition to a simple compensation[2] network, the CM converter offers superb line regulation, very good transient response to large load changes, and cycle-by-cycle current limiting because the current is sensed each switching cycle.

Line regulation is defined as the amount that the output voltage changes with a change in input voltage. It is related to the gain of the control-to-output transfer function. Since the gain of the control-to-output transfer function for the CM topology is independent of the input voltage, the line regulation is very good. Also for this topology a single pole operates with less phase/time lag, so a converter with peak CM control will have better transient response than a converter with VM PWM control.

When examining the control-to-output transfer function of the VM technique, the input voltage has a direct impact on the gain and the line regulation will be degraded. Today's VM converters overcome this by employing voltage feed-forward techniques that change the slope of the PWM ramp based on the input voltage. The table below outlines the advantages/disadvantages[2] of both approaches.

So why choose VM versus CM? Since the CM design requires two control loops and greater circuit complexity versus that of VM, it may be more cost effective to choose a regulator with VM control. Historically, with a wide input-voltage operating range especially under low-line/light-load conditions, the current ramp slope may be too shallow for stable CM PWM operation. This limitation has been greatly improved by new devices like the MAX17500 – MAX17504 family of high-voltage CM converters.

Table. Summary of VM control versus CM control.

	Current Mode	Voltage Mode
Compensation	Simple compensation network	Complex compensation network
DCM and CCM operation	Transitions from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) are not a problem.	Harder to design a compensator that provides good performance in both conduction modes.
Line rejection	Very good line regulation	Needs voltage feed forward
Current sensing	Needed	Not needed
Subharmonic oscillations	Current-mode control can be unstable when the converter's duty cycle approaches 50%. Modern converters employ internal slope compensation that eliminates both these effects and the need for power-supply design expertise to account for these effects.	Not applicable
Transient response	Since CM control senses a change in load cycle; the error amplifier does not need to react quickly so the loop can make a correction.	In VM control a load current change must change the output voltage before the error amplifier can react and make a correction. VM control is slower to respond to very high-speed load transients than is CM control.

What Is Slope Compensation?

Although most modern integrated converters include built-in slope compensation, it is important to understand why slope compensation is needed.

Assume that a stepdown converter is operating in continuous conduction mode (CCM). This means that the current in the inductor never falls to zero, and the duty cycle of the converter is about 75% at heavy load with only the output current as the ramp signal to the comparator (i.e., no slope compensation). A load transient to light load will then cause the current control loop to turn off the control FET switch early.

Since the duty cycle is at 75%, there is little time for the inductor current to decay and the flux in the inductor core to reset itself. Meanwhile, the load voltage determines the inductor's falling slope. As long as the load is not shorted, the current in the output inductor will take time to ramp down to the lower threshold value at the PWM comparator.

When the clock initiates the next cycle, the switch never turns on because the current is still too high. (Alternatively, it turns on very briefly at the minimum duty cycle of the controller.) If the current is really high, the next cycle may see the same conditions and remain effectively off.

These conditions will make the converter oscillate at some subharmonic of the PWM switching frequency. Slope compensation provides a means to bring the ramp down to zero during the short dead time. The ramp of the internal clock signal is summed with the sensed current waveform. There will still be very short pulses for overcurrent conditions, but by summing the clock signal with the current signal, this subharmonic oscillation has been resolved.

Synchronous Versus Asynchronous Rectification

Taking a closer look at the power stage of a typical dc-dc converter, we see that there are two types of output stages (Fig. 6.) A converter that employs a diode in the output stage is said to be using asynchronous (or nonsynchronous) rectification. Meanwhile, a converter with both high-side and low-side FETs is commonly referred to as having synchronous rectification; the control block of the dc-dc converter will synchronize the turn on/off times of both FETs. This action optimizes and prevents overlapping of these FETs so that both FETs are not conducting at the same time.

The high-side FET conducts at $V_{OUT}/V_{IN} \times 1/f_{sw}$; the low-side FET conducts at $1 - V_{OUT}/V_{IN} \times 1/f_{sw}$, where f_{sw} is the switching frequency of the converter. In general, for low-duty-cycle applications, asynchronous converters may not meet board power-efficiency goals, as the conduction power loss can be dominated by the $I \times V_{DIODE}$ power loss versus the low-side $R_{DS(ON)} \times I$ power loss of a synchronous converter.

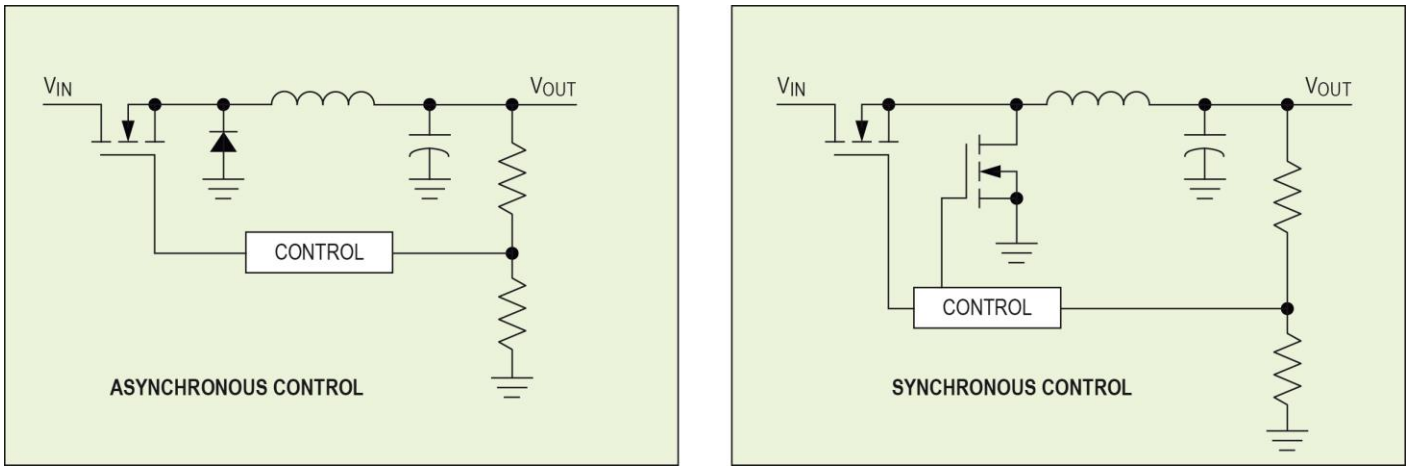

Fig. 6. Asynchronous versus synchronous control of the output rectifier.

When choosing a part with synchronous rectification, look closely at the application. For example, if the application is to convert 5 V to 2.5 V, then a regulator with a rating of 14 V may not be optimal as it could be designed for a distributed 12-V power bus commonly found in telecom and server applications. As such, the internal high-side FET may have a higher R_{DSON}, optimized for typical duty cycles that are less than 10% for 1-V and lower core voltages.

For this example, the 12-V regulator's FETs can be optimized for a much lower duty cycle in which the R_{DSON} is optimized for the low-side FET where conduction power losses dominate; the high-side FET has higher R_{DSON} but much lower gate charge where the switching power losses tend to dominate. Thus, to convert 5 V to 2.5 V the duty cycle is 50%. Choosing a part with a maximum rating of 6 V may be the better choice.

Typically, the majority of stepdown converters designed for 5-V and 12-V systems will employ a synchronous-rectifier output stage. Asynchronous rectification stages that use Schottky diodes in place of the low-side FET seem to be more common in industrial applications when voltage levels are at least 24 V and higher.

Newer parts like the MAX17501 – MAX17504 mentioned above integrate both high-side and low-side FETs. They have a maximum input voltage rating of 60 V that allows for increased efficiency in industrial applications where the dc voltage bus is 24 V or higher.

Internal Versus External FETs

There is no one-size-fits-all regulator optimized for all possible power rails. Consequently, sometimes a designer who wishes to optimize efficiency for a given application will choose a dc-dc controller that requires external FETs. At higher power levels when creating sub-1V power rails from a 12-V rail, FET selection is critical. Thus, choosing a high-side FET with higher R_{DSON} and low gate charge can optimize overall efficiency when duty cycles are low. Further, it may be necessary to use two or more FETs in parallel to decrease the conduction loses, while keeping the switching losses at a minimum for the low-side FET. The references at the end of this article provide a good starting point for the selection criteria of external FETs for dc-dc controllers.

Conclusion

This part 1 article provides the reader with a better understanding of the design tradeoffs in selecting a switching regulator. Understanding the application is critical for choosing the optimal regulation solution! Once these criteria are understood, decisions can be made on the control mode.

By explaining the differences between voltage mode (VM) and current mode (CM) control we help the reader choose the best control method for the application. A brief description of the tradeoffs between synchronous versus asynchronous rectification will also help the reader determine the performance-versus-cost tradeoffs—asynchronous parts tend to be lower cost.

Finally, I have outlined why it may be advantageous to use choose a controller that uses external FETs. No attempt has been made to include countless power-supply equations, as this article targets the board designer who may not have the luxury of utilizing in-house power supply engineers.

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About The Author

Don Corey joined Maxim Integrated in 2006 and is a principal member of technical staff, field applications. He has over 30 years of analog electronic design experience. He got his BSEE from Central New England College.

For further reading on power supply control schemes, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Control Methods" in the Design Area category.