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Choose The Right Regulator For The Job (Part 2): Primary And Secondary Control Schemes

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This article is part 2 of a three-part series on power regulators. In <u>part 1</u>, we discussed two regulator control schemes, current mode (CM) and voltage mode (VM), for pulse-width modulated (PWM) converters. We also examined the critical differences between those control modes. In that article I explained how the product application is very important for selecting the right regulator. One size does not fit all! Quite the opposite. Semiconductor companies target segment markets and tailor regulator parameters to the end-product requirements. Clearly, understanding the application will help in selecting the right regulator.

We begin our part 2 article with an examination of other commonly used regulator control methods and describe the application benefits for each. Besides the VM and CM PWM control discussed earlier, modern regulators incorporate other primary control schemes: pulse-frequency modulation (PFM), hysteretic, and constant on-time (COT). After we look at each, we add a short discussion about secondary control methods, such as skip mode.

This discussion will continue in <u>part 3</u> with the basic equations to help a designer choose the best regulator for an application and optimize the surrounding components.

A PFM Converter Provides Better Overall Efficiency

A PFM converter^[1] is an alternative dc-dc architecture. This control scheme varies the converter switching frequency in direct relationship to the converter load. Consequently, the architecture is referred to as PFM. Many portable applications will use PFM mode to maximize battery life, because a PFM converter is much more efficient at light loads than a PWM-based converter.

Electromagnetic interference (EMI) is an important consideration when choosing between a PWM or PFM converter. In PWM mode the switching frequency is fixed so EMI from converter switching is predictable and constant, and in many cases can be filtered. Many PWM converters also offer external, frequency synchronization input to help mitigate conflict with other important signal frequencies often present on the application board. If an application requires more than one voltage, all the switching converters can be clocked at the same frequency. This approach eliminates the inherent beat frequencies when multiple converters are not switching at the same frequency and not perfectly phase aligned.

In contrast to PWM-based converters, the switching frequency is variable for PFM, and it is much harder to control EMI. As such, PFM mode may not be the best choice for powering sensitive, low-noise audio or RF circuits. PFM would, however, be an excellent choice when efficiency must be optimized over a wide range of output loads.

It should be noted, finally, that many converters have provisions to run in either PFM or PWM mode. A logic-controlled mode pin or internal circuitry automatically switches between these two modes based on load current.

Operation Of A PFM Controller

In stepup PFM control^[1] two one-shot circuits operate based on the load current from the dc-dc converter's output. The PFM is based on two switching times (the maximum on-time and the minimum off-time) and two control loops (a voltage-regulation loop and a maximum peak-current, off-time loop). The PFM is also characterized by control pulses of variable frequency. The two one-shot circuits in the controller define the T_{ON} (maximum on-time) and the T_{OFF} (minimum off-time).

The T_{ON} one-shot circuit activates the second one-shot, T_{OFF} . Whenever the comparator of the voltage loop detects that V_{OUT} is out of regulation, the T_{ON} one-shot circuit is activated. The time of the pulse is fixed up to a



maximum value. This pulse time can be reduced if the maximum peak-current loop detects that the current limit is surpassed, as shown in Fig. 1. The quiescent current (I_Q) consumption of a PFM controller is limited only to the current needed to bias its reference and error comparator (tens of microamps.) In striking contrast, the internal oscillator of a PWM controller must be turned on continuously, leading to a current consumption of several milliamps.

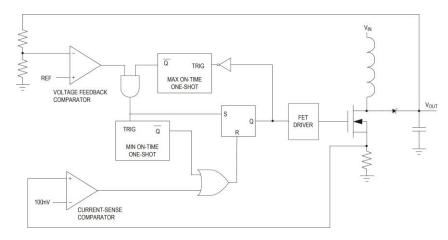


Fig. 1. Pulse-frequency modulation (PFM) control circuit. With this control technique the pulse time can be reduced if the maximum peak-current loop detects that the current limit is surpassed.

Synchronous stepdown converters often have dual-mode operation so the designer can select between PWM and PFM modes and optimize efficiency over a wide range of load currents. Two example converters, the MAX17503 and MAX17504, use an alternate PFM control scheme but are also good examples for efficiency improvement at lighter loads.

For example, Fig. 2 shows efficiency curves for PFM and PWM modes. With load currents below 100 mA in PFM mode we see a dramatic efficiency improvement versus PWM mode for the same load current. Note that for a voltage input of 12 V and voltage output of +5 V, the efficiency is close to 92% in PFM mode versus 81% in PWM mode!

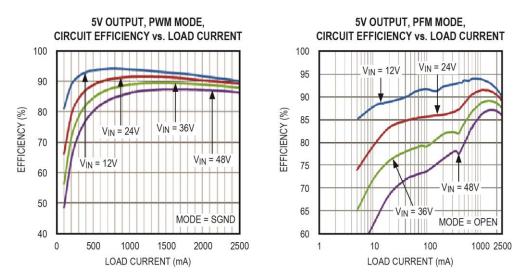


Fig. 2. PWM and PFM efficiency curves for the MAX17503 stepdown converter. Note that with load currents below 100 mA in PFM mode (right) we see a dramatic efficiency improvement vs. PWM mode for the same load current.



Let's summarize the advantages of PFM:

- Very good low-power conversion efficiency,
- Does not require a loop-compensation network and
- Lower solution cost.

And the PFM disadvantages:

- Variable frequency can be harder to filter for emissions. This mode may not be suitable in the presence
 of low-noise, sensitive analog circuitry.
- Output ripple can be higher than PWM mode.

A Hysteretic Converter Offers Predictable Operation

As in most comparator-based circuits, hysteresis is used to maintain predictable operation and avoid switch chatter. The hysteretic converter^[2] in Fig. 3 turns the power FET on or off based on the output-voltage changes sensed by the converter. Sometimes called a "ripple regulator" or "bang-bang controller," this architecture continuously shuttles the output voltage back and forth to just above or below the ideal set point. Because the hysteretic architecture varies, the drive signal to the power FET is based on the operating conditions of the circuit. The switching frequency is not constant. The hysteretic approach is, therefore, one type of PFM architecture.

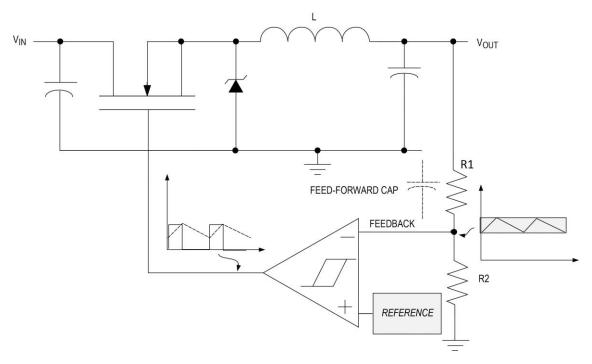


Fig. 3. A converter employing hysteretic control turns the power FET on or off based on the output-voltage changes sensed by the converter.



Now look at the advantages of hysteretic control:

- No loop compensation required (the same for a PFM topology). The loop bandwidth is close to the switching frequency itself.
- No clock or error amplifier is needed, so operating current is very low. This type of regulator is suitable for battery-powered applications.
- · Hysteretic converters are low cost.

And the hysteretic control disadvantages:

- With no fixed clock, it is difficult to predict switching frequency compared to PWM control. This type of regulator is not suitable for applications with sensitive analog circuitry.
- May require a feed-forward capacitor across R1 in Fig. 3 to increase voltage ripple on the feedback pin when using lower-ESR output capacitors.

Hysteretic Constant On-Time (COT) Control Keeps Frequencies Constant

Recall that the main disadvantage of the hysteretic converter is the variable frequency. Because it uses a comparator with hysteresis, there must be sufficient voltage ripple at the feedback node to ensure stable switching. Basically, the ripple voltage at the comparator's feedback node must be greater than the comparator's hysteresis band. Moreover, a higher ESR capacitor may be needed to increase output ripple voltage or a feed-forward capacitor like the one in Fig. 3 must be added.

However, there is another option. To keep the frequency as constant as possible, a constant on-time (COT) generator may be been added. In this COT control mode, the T_{ON} time will be inversely proportional to the input voltage, as shown in Fig. 4.

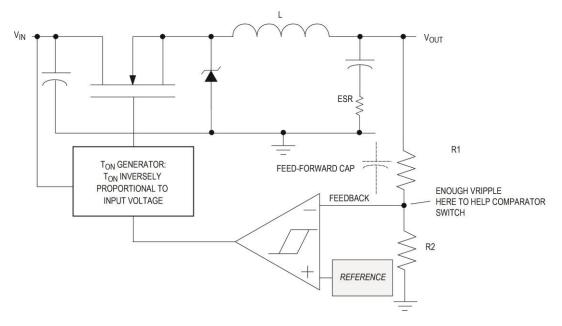


Fig. 4. Constant on-time (COT) hysteretic converter keeps the frequency as constant as possible.

The COT generator greatly enhances this type of converter, allowing it to maintain a constant frequency over a wider range of input voltages. The generator, however, does not solve the need to add ripple at the feedback node to help the comparator switch. The addition of COT to hysteretic control lets the design engineer better



predict the switching frequency. COT control also lets you better optimize filtering for EMI and offers the advantage of low cost and good transient response.

Modern converters with COT control also create a ripple voltage by sensing the current in the low-side MOSFET. The COT control then adds this voltage to the internal feedback voltage or to the internal voltage reference. The resulting benefits from the COT control technology are important: no more requirement for a ripple voltage, and low-ESR ceramic capacitors can now be used.

There are modern synchronous stepdown converters that employ a minimum on-time control in a hysteretic PWM control scheme. As in Fig. 3, the hysteretic comparator is still used. Operation of this control scheme is quite simple. When the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This switch remains on until the minimum on-time expires and either the output voltage is above the regulation threshold or the inductor current is above the current-limit threshold.

Once off, the high-side switch remains off until the minimum off-time expires and the output voltage again falls below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on again or the inductor current approaches zero. To help improve efficiency, an internal synchronous rectifier eliminates the need for an external Schottky diode, as shown in Fig. 5.

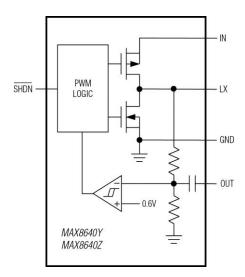


Fig. 5. Hysteretic PWM control in the MAX8640Y/Z stepdown converter.

Skip/Power-Save Mode Optimizes Efficiency At Lighter Loads

Pulse-skipping mode, also called power-save mode, is a secondary control mode used with some PWM converter architectures; it is especially useful to optimize efficiency at lighter loads for portable or low-power applications.

When a PWM converter operates at moderate to high load currents, it runs in continuous-conduction mode, meaning that the inductor current will not reach down to zero. As the load current decreases, the converter may switch to discontinuous-conduction mode, where the current in the inductor does decrease to zero, depending on the value of the inductor. Then at very light loads, the converter goes into skip or power-save mode. Now it intermittently turns off the internal oscillator and reenables it only as needed to maintain the output regulation. Hence, the "skipping" and power savings. Because this action further modulates the switching frequency, skip or power-save mode is sometimes referred to as a form of PFM mode.

There are modern dc-dc converters that allow the user to select between PWM or skip mode to reduce current consumption and achieve a higher efficiency at light output loads. In skip mode, the high-side and low-side MOSFETs are turned off when the inductor current falls below the skip-mode current threshold. Thus, the



inductor current is never allowed to go negative. If the inductor current falls below this threshold during the off time of the clock cycle, the low-side MOSFET turns off. At the next clock cycle, if the output voltage is above the set point, the PWM logic keeps both high-side and low-side MOSFETs off. If the output voltage is below the set point, the PWM logic turns the high-side MOSFET on for a minimum fixed on-time. This is how cycles are skipped and the switches are controlled to service the loads as needed.

The efficiency curves in Fig. 6 show the skip-mode efficiency improvement below 200 mA compared to the PWM mode of operation under the same conditions.

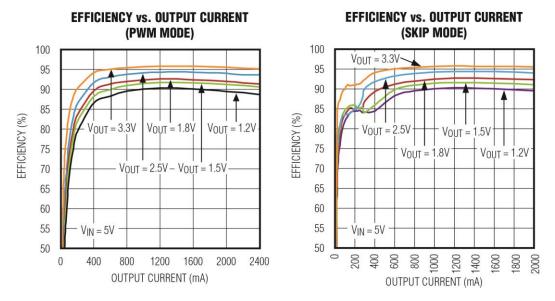


Fig. 6. PWM versus skip-mode efficiency curves for the MAX15053 stepdown switching regulator.

Note the improved efficiency of skip mode below 200 mA vs. PWM mode.

Conclusion

In this second article in the series on choosing the right regulator, we discussed and contrasted several control methods: PFM, hysteretic, COT, and skip mode. Despite their various differences, advantages, and disadvantages, we see that these techniques provide a distinct advantage in portable devices where battery runtime and low power must be optimized.

In the earlier <u>part 1 article</u>, we explained fixed-frequency voltage mode (VM) and current mode (CM) control schemes. We assessed their tradeoffs and the impact of each on the application.

In the next and final <u>part 3</u>, we will provide the basic equations to help a designer choose the best regulator and optimize the surrounding components for the total regulator solution. We will also provide a part selection and simulation example that illustrates the topics discussed in both prior articles.

Finally, there have been countless power-supply articles and textbooks that examine the topic in great detail. There are also many other control topologies that have been developed, which are beyond the scope of this article series. But hopefully, the part 1 and part 2 articles have provided a good starting point for engineers wishing to design point-of-load power management.

References

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About The Author



Don Corey joined Maxim Integrated in 2006 and is a principal member of technical staff, field applications. He has over 30 years of analog electronic design experience. He got his BSEE from Central New England College.

For further reading on buck converter design, see the How2Power Design Guide, select the <u>Advanced Search</u> option, go to Search by Design Guide Category and select "Control Methods" in the Design Area category.