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Take The Edge Off High dV/dt Supplies

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High dV/dt rise times on the power supply can cause problems with downstream components. This is especially true in 24-V powered industrial and automotive systems with high-current output drivers. This design idea describes how to control the rise time while limiting the power loss through the control FET.

Limiting The Rise Time

For many systems a simple pFET circuit with associated components is enough to limit the supply's risetime. However, when currents reach 8 A and beyond, the R_{DSON} of the pFET can cause heat to rise in the system. An nFET with lower R_{DSON} is a nice alternative.

The MAX16127 is a 3-mm x 3-mm nFET controller designed for overvoltage protection. It can also be used to control the ramp of a supply voltage. The power-good/FLAG output on this protection circuit gives it the unique ability to enable downstream devices when the controlled voltage is at 90% of the input voltage, regardless of the input voltage. This feature is a nice improvement over setting a fixed turn-on voltage or delay time, especially in industrial and automotive systems where input voltages can vary over a wide range.

The circuit in Fig. 1 shows the basic configuration used to ramp V_{IN}. The GATE pin of the MAX16127 is a current-output circuit coming from an internal charge pump. It drives the gate of an nFET transistor to about 10 V above the source of the nFET.

An additional capacitor on the GATE pin can be used to control the rise time of the nFET gate voltage, and the value of the capacitor can be adjusted for the desired slew rate. In this case C1, a 220-nF capacitor is used, as shown in Fig. 1. Resistor R2 (1 kΩ) is in series with C1. R2 isolates C1, so that when the MAX16127 turns off during an overvoltage or fault condition, there is a quick turn-off time.

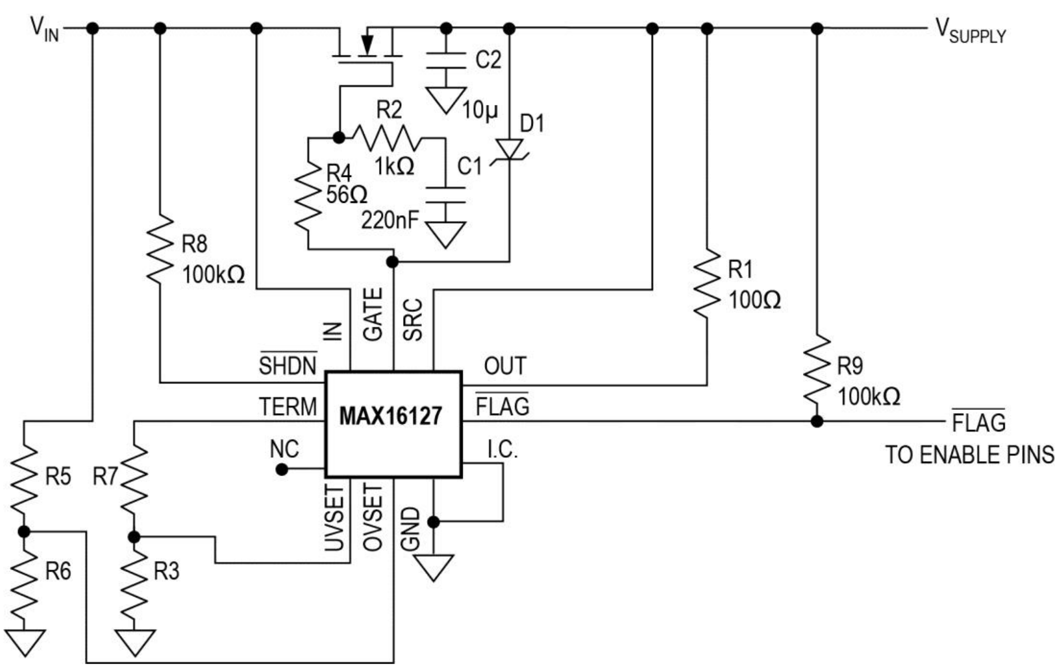


Fig. 1. Schematic for rise-time control circuit.

The nFET will be in its linear region while the gate ramps. Consequently, large amounts of power dissipation can be seen if all of the downstream circuits start working while it is ramping. The /FLAG pin of the MAX16127 is, in this case, used as an enable pin for downstream drivers and power supplies. Figs. 2 and 3 show how the /FLAG-enable signal moves out in time as V_{IN} changes, always enabling when V_{SUPPLY} is at 90% of V_{IN}. When using /FLAG as an enable, you only have to worry about sizing the nFET for that last 10% when everything is on.

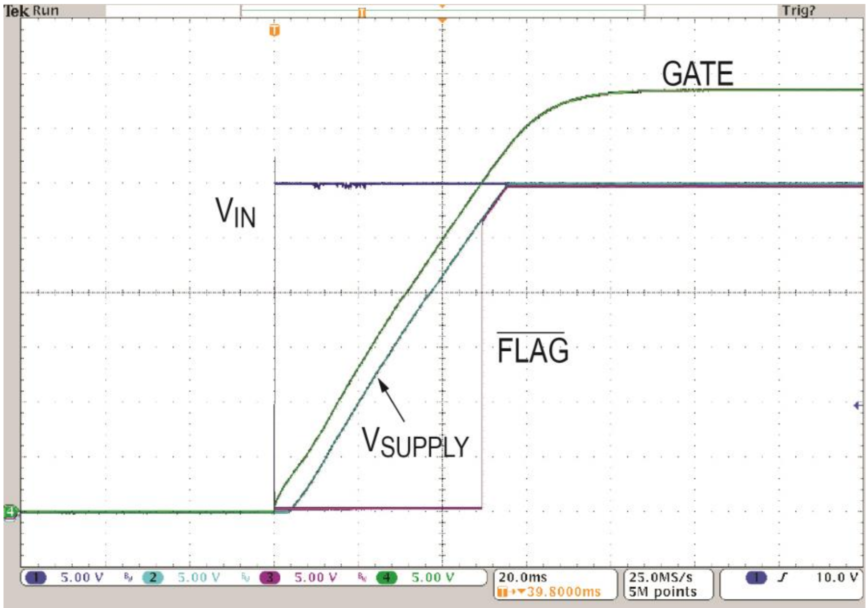


Fig. 2. Waveforms and /FLAG behavior for a 30-V V_{IN}.

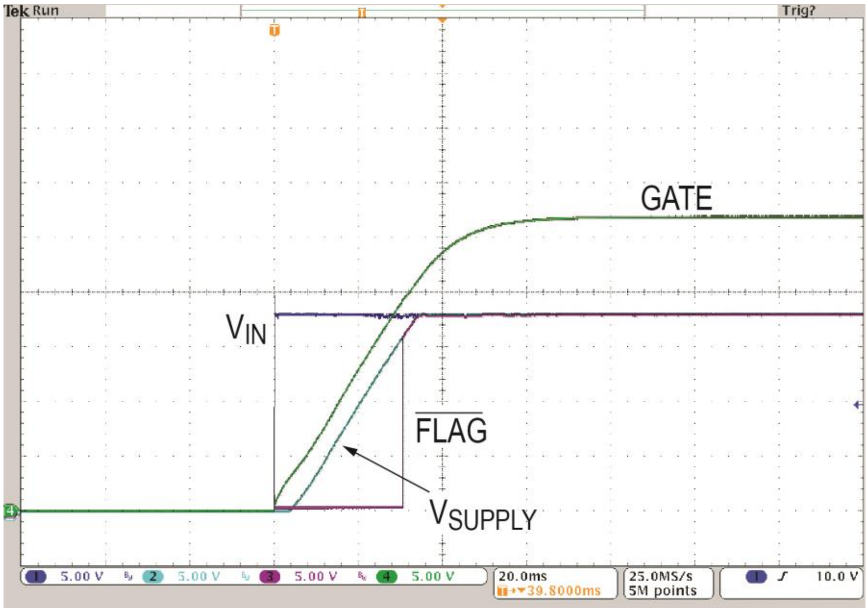


Fig. 3. Waveforms and /FLAG behavior for a V_{IN} of 18 V.

The GATE pin of the MAX16127 has a nominal current of 180 µA, and you calculate your gate-drive rise time using the formula: I = C*dV/dT. Using the 220-nF capacitor shown gives us a dV/dT of approximately 0.82 V/ms. Fig. 2 shows V_{SUPPLY} ramping to 30 V in approximately 40 ms, which is close to what we would expect, as the gate drive ramps linearly.

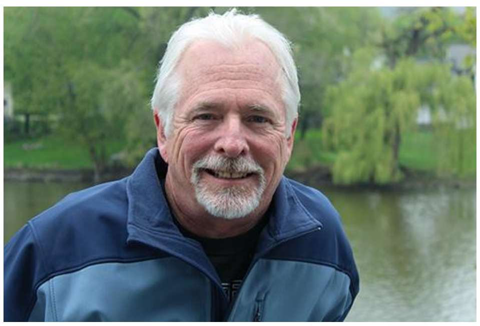
This circuit also provides the standard overvoltage protection using resistors R5 and R6, and undervoltage lockout using resistors R3 and R7.

Sizing The FET

In this example we use the 90% /FLAG to enable a downstream load of 10 A. Assuming a maximum of 30 V on V_{IN}, we need to size the FET so that it can handle the average power as V_{SUPPLY} ramps from 27 V to 30 V in about 4 ms. The average power will be ½(V_{IN} - V_{OUT}) × I or 1.5 V × 10 A = 15 W, but for a short duration.

Most power FET data sheets will have a safe-operating-area (SOA) graph that shows V_{DS} versus current with an overlay of time. Check the SOA to size your FET.

About The Author



Rob McCarthy has been with Maxim since 2011 as a field application engineer in the Chicago area. He has 30 years of design and application experience including stints at Snap-on Tools, Harris Corporation and TI. In his free time he enjoys bicycling and fishing the rivers of Illinois.