Optimizing The Efficiency Of The Four-Switch Buck-Boost Converter

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With higher ambient operating temperatures now quite prevalent in many automotive and industrial applications, efficient and reliable dc-dc power solutions are a necessity, spurring designers to look more closely at power losses. A converter with excessive component temperature rise can mandate a circuit redesign or a board layout revision,[1] disrupting the cadence of product development and possibly compromising committed schedule dates.

With that in mind, easy-to-use converter design tools[2] have gained favor as a quick way to choose components, review Bode plots and compensation, examine efficiency curves, and estimate power losses within the converter. That said, a keen understanding of a converter's operating modes and power losses is both essential and invaluable.

A primary objective of this article is to look closely at the four-switch buck-boost converter's efficiency. The real purpose here is a practical one—the performance of the power stage is crucial as it can make or break an actual design. The four-switch buck-boost converter is actually a convenient platform to study dc-dc converter efficiency as the analysis is primarily based on buck and boost switching modes. By deriving the relevant duty cycle in each mode, we can calculate efficiency and power losses over input voltage and output current ranges.

Converter Structure

Let's review the structure of the four-switch (non-inverting) synchronous buck-boost power stage as shown in Fig. 1. The main attraction of this "contemporary" buck-boost power stage is that simple buck or boost operating modes are harnessed to achieve high conversion efficiency across wide and overlapping ranges of input and output voltage. It produces a positive output voltage—in contrast to the "classic" single-switch (inverting) buck-boost—and, by virtue of its simple magnetic component, lower power loss and higher power density relative to SEPIC, flyback, or cascaded boost-buck topologies.[3]

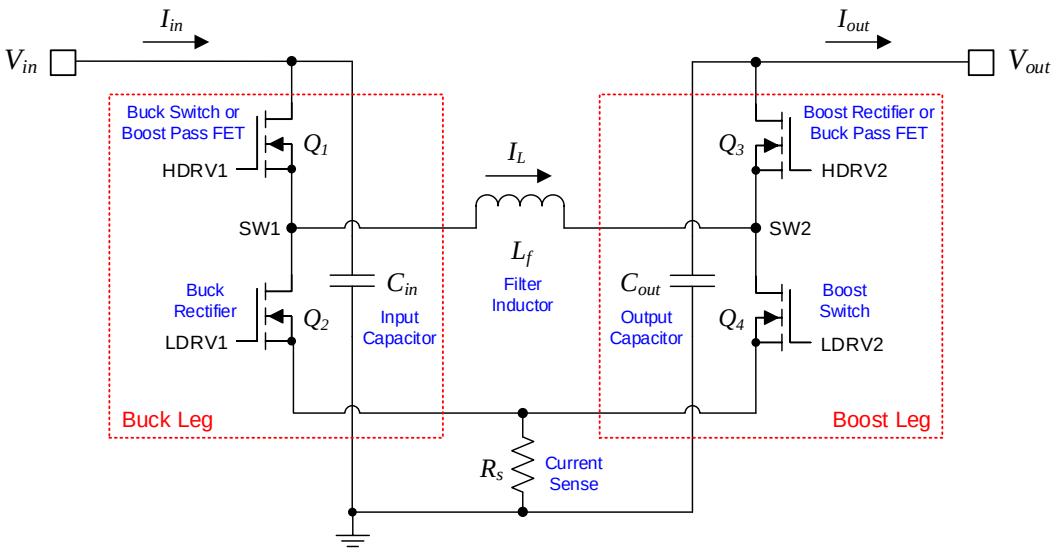

Fig. 1. Four-switch synchronous buck-boost converter power stage. Three operating modes are possible depending on the input voltage relative to the output voltage: buck ($V_{IN} > V_{OUT}$), boost ($V_{IN} < V_{OUT}$) and buck-boost transition ($V_{IN} \cong V_{OUT}$) mode.

In its favor, the four-switch buck-boost converter has an intuitive topology approach as it combines two easily understood topologies—the buck and boost. It also offers compact solution size, controlled startup and short circuit protection in boost mode, output disconnect in shutdown, simple control and compensation, and fixed-switching frequency. As such, it fits a cross section of applications including battery charging, solid-state lighting, industrial computing, RF power amplification, and automotive.

Operating Modes

Arranged in Fig. 1 are four power MOSFETs in an H-bridge configuration, with switch nodes SW1 and SW2 connected by inductor L_f. Synchronous buck or boost operation occurs when the input voltage is a sufficient margin above or below the output voltage, respectively, and the high-side MOSFET of the opposite, non-switching leg conducts as a pass device. Furthermore, as the input voltage approaches the output voltage, the switching buck or boost leg conduction time reaches a prescribed timer threshold, setting a latch that initiates operation in buck-boost transition mode.

A buck-boost controller, for example the LM5175,[4] uses a scheme in the buck-boost (B-B) region where both buck and boost legs each switch at half switching frequency in a phase-shifted, interleaved manner for lower switching losses. The switch-node voltage waveforms corresponding to input voltage variation are shown in Fig. 2.

Given the lack of conventional buck-boost switching where diagonal MOSFET pairs conduct, the term "buck-boost mode" [5] here is somewhat of a misnomer and can be easily misinterpreted. In the context of the four-switch buck-boost topology, it is only meant to designate operation when the input voltage is close to the output voltage setpoint and both legs are switching.

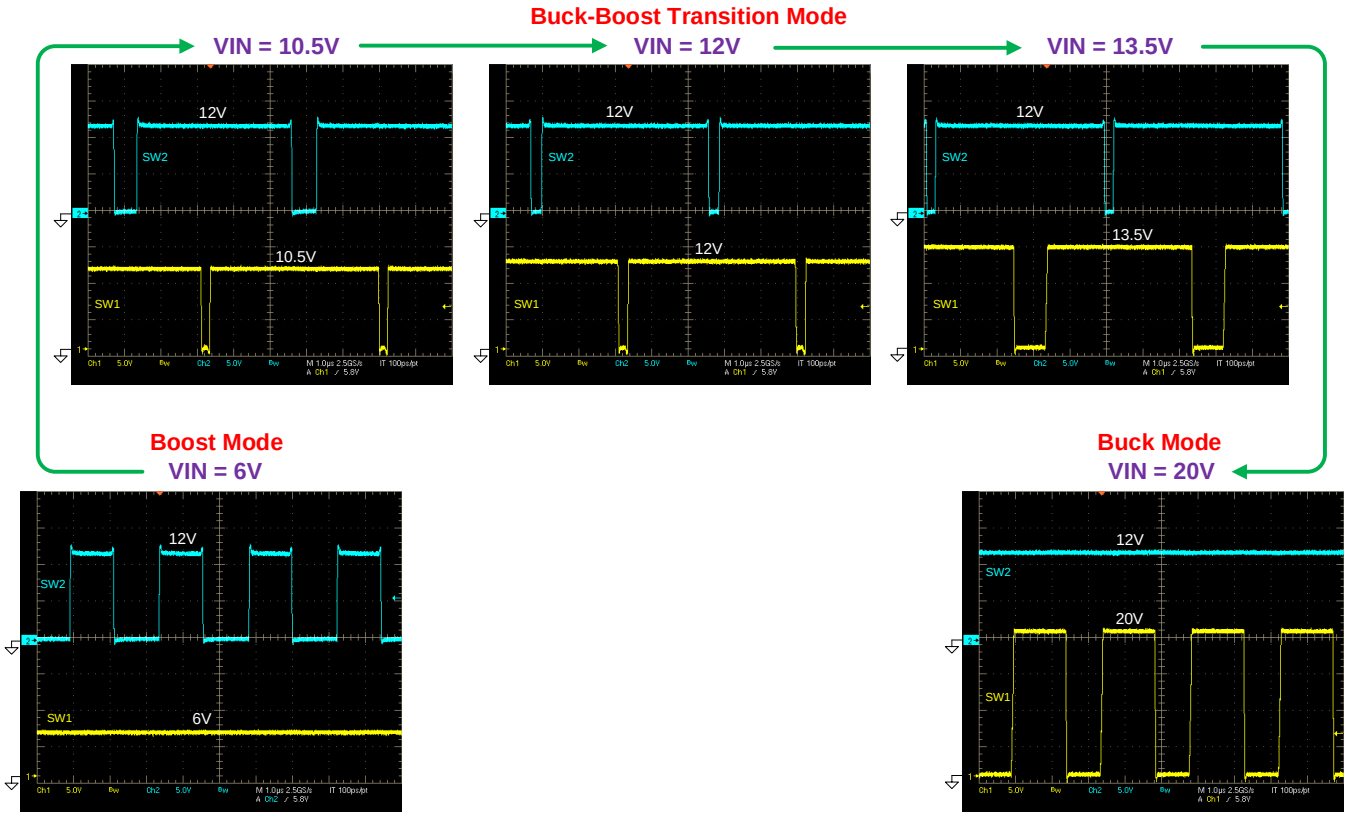

Fig. 2. SW-node voltages for buck (SW1) and boost (SW2) legs during buck, boost, and buck-boost operating regions. V_{out} = 12 V.

Of course, the four-switch buck-boost converter's mode of operation must change smoothly and autonomously without a need to alter the control configuration. How this is realized, and what the codependent relationship between power stage and control scheme may be, is quite important. Peak current-mode control in boost and valley current-mode in buck enable smooth mode transitions, and only one low-side configured shunt resistor is required for current sensing.

Duty Cycle In Buck Or Boost Mode

Using the inductor volt-second balance technique and assuming continuous conduction mode (CCM), the respective duty cycles in buck and boost modes are calculated for a given current as follows:

$$D_{buck} = \frac{V_{out} + \left(R_{DS(on)Q2} + R_s + R_{dcr}\right) I_L}{V_{in} + \left(R_{DS(on)Q2} - R_{DS(on)Q1} + R_s\right) I_L} \approx \frac{V_{out}}{V_{in}} \quad (1)$$

$$D_{boost} = \frac{V_{out} + \left(R_{DS(on)Q3} + R_{dcr}\right) I_L - V_{in}}{V_{out} + \left(R_{DS(on)Q3} - R_{DS(on)Q4} - R_s\right) I_L} \approx 1 - \frac{V_{in}}{V_{out}} \quad (2)$$

where $R_{DS(on)}$, R_s and R_{dcr} are the applicable MOSFET on-state resistance, shunt resistance, and inductor dc resistance (DCR) consistent with the schematic of Fig. 1. The dc level of inductor current relates to the output current by

$$I_L = \begin{cases} I_{out}, & \text{buck mode} \\ \dfrac{I_{out}}{1 - D_{boost}}, & \text{boost mode} \end{cases} . \quad (3)$$

Duty Cycles In The Buck-Boost Region

Fig. 3 delineates the idea of an equivalent mid-rail voltage, V_{mid}, from which the duty cycle of each leg during the buck-boost region is derived. The converter is modeled as a cascaded connection of equivalent buck and boost stages with filter inductor split by capacitor C_{mid}. Taking 11-V input to 12-V output conversion as an example, the (passive) buck leg operating at 95% max duty cycle steps down to 10.4 V, thus providing adequate headroom for the (active) boost leg to regulate the output to 12 V.

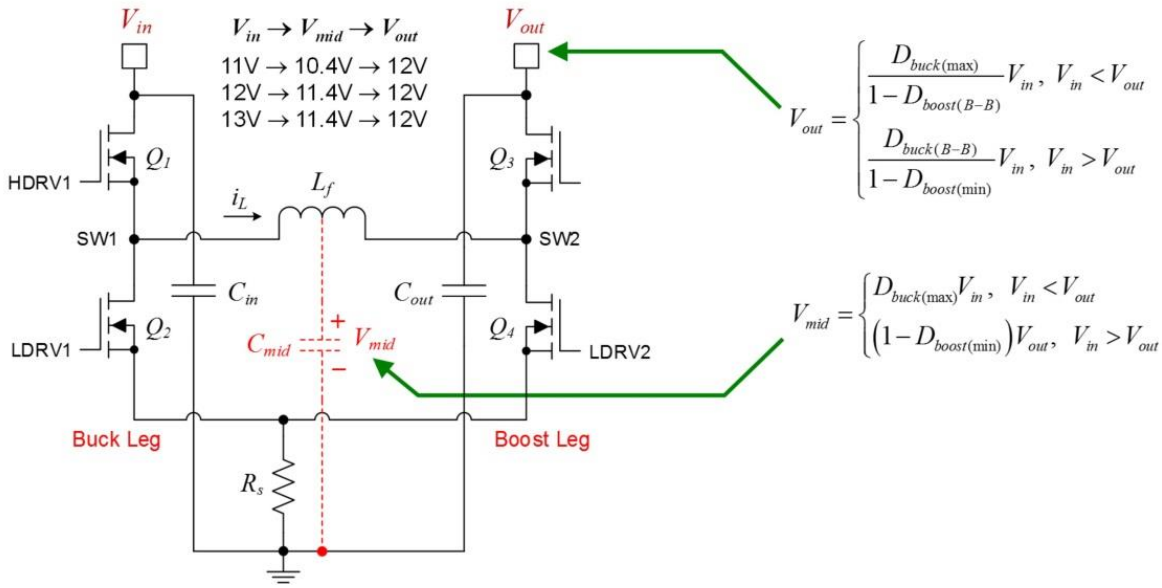

Fig. 3. This equivalent circuit model for power stage operation in the buck-boost region is used to derive duty cycle equations.

Depending on the operating point within the buck-boost window, the duty cycle of the passive, non-modulated leg is held at $D_{buck(max)}$ or $D_{boost(min)}$. By inspection, the equivalent mid-rail voltage is:

$$V_{mid} = \begin{cases} D_{buck(\max)} V_{in}, & V_{in} < V_{out} \\ \left(1-D_{boost(\min)}\right) V_{out}, & V_{in} > V_{out} \end{cases} . \quad (4)$$

Then, the buck or boost duty cycle corresponding to the active, modulated leg in the buck-boost region becomes:

$$D_{boost(B-B)} = 1 - \frac{V_{mid}}{V_{out}} = 1 - \frac{V_{in}}{V_{out}} D_{buck(\max)}, \quad V_{in} < V_{out}$$
$$D_{buck(B-B)} = \frac{V_{mid}}{V_{in}} = \frac{V_{out}}{V_{in}} \left(1 - D_{boost(\min)}\right), \quad V_{in} > V_{out} . \quad (5)$$

Rearranging equation 5 to obtain the output voltage as a function of duty cycle and input voltage within the buck-boost region gives:

$$V_{out} = \begin{cases} \frac{D_{buck(\max)}}{1-D_{boost(B-B)}} V_{in}, & V_{in} < V_{out} \\ \frac{D_{buck(B-B)}}{1-D_{boost(\min)}} V_{in}, & V_{in} > V_{out} \end{cases} . \quad (6)$$

Plotting Duty Cycle As A Function Of Input Voltage

Applying the duty cycle relationships from equations 1, 2, and 5 to a 12-V output converter design,[6] the variation of buck and boost leg duty cycles with increasing input voltage is given by Fig. 4.

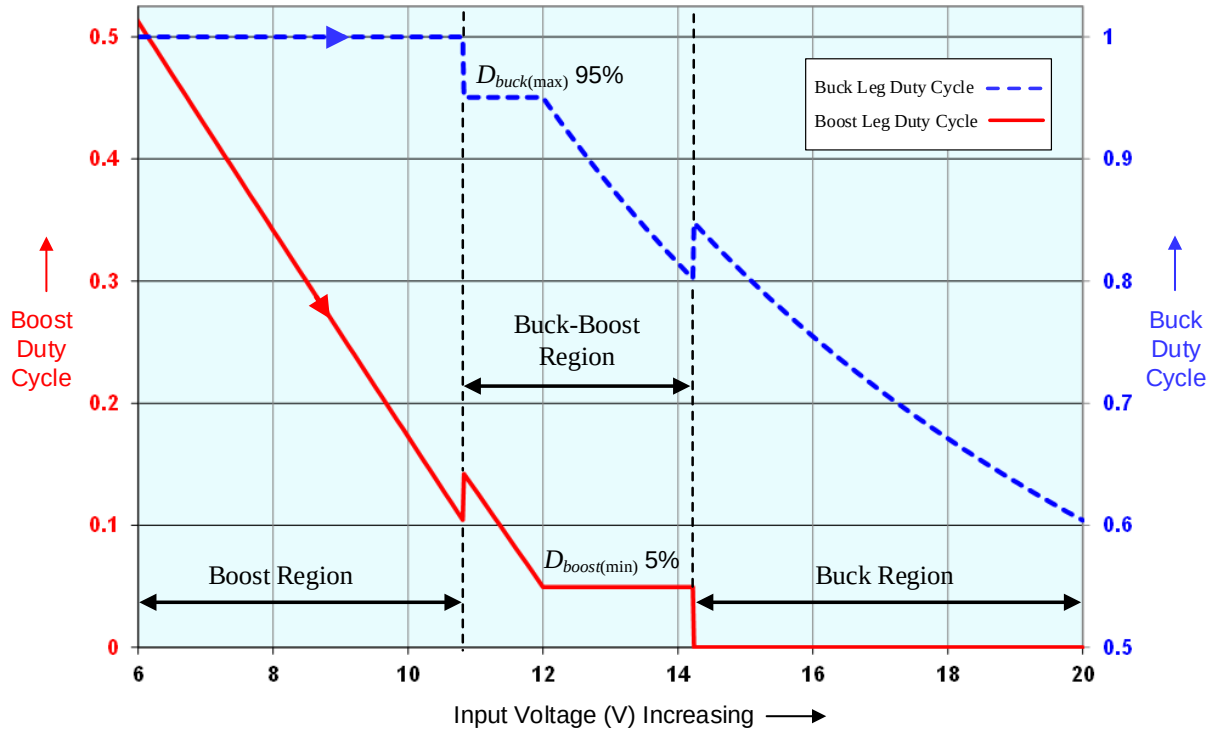

Fig. 4. Buck and boost leg duty cycle variations over the input voltage range. Output voltage is 12 V.

Modeling Converter Efficiency Performance

Characterization of all four power MOSFETs requires data for on-state resistance, gate charge, gate resistance, forward transconductance, gate-source threshold voltage, body diode forward drop and reverse-recovery charge, and thermal resistance. This information is mined from MOSFET datasheets and from analysis of the switching waveforms.[7–9]

Buck And Boost Region Power Dissipation

Table 1 presents expressions in buck and boost modes for MOSFET conduction, switching, gate-drive, deadtime, and shunt-resistor power dissipation. The switching transition times of the control MOSFETs, Q_1 and Q_4, are dictated by the respective gate driver's source and sink current capability,[8] MOSFET effective gate capacitance, and parasitic inductances.[9]

Deadtime is also a function of the gate-driver circuit (based on its fixed or adaptive timing) as well as circuit operating conditions, and should be experimentally verified at the required load current and operating temperature conditions. The deadtime-conduction voltage drop, V_d, is reduced by anti-parallel connection of Schottky diodes across the synchronous FETs.

Table 1. Component power loss expressions when operating in buck and boost modes.

Mode	Buck	Boost
MOSFET conduction loss	$P_{cond(buck)} = I_{out}^2 \left[R_{DS(on)Q3} + D_{buck} R_{DS(on)Q1} + D_{buck}{}' R_{DS(on)Q2} \right]$	$P_{cond(boost)} = I_{in}^2 \left[R_{DS(on)Q1} + D_{boost} R_{DS(on)Q4} + D_{boost}{}' R_{DS(on)Q3} \right]$
Shunt loss	$P_{shunt(buck)} = D_{buck}{}' R_s I_{out}^2$	$P_{shunt(boost)} = D_{boost} R_s I_{in}^2$
MOSFET switching loss	$P_{sw(buck)} = V_{in} f_{sw} \left[I_{out} \left(\frac{t_{on\,Q1} + t_{off\,Q1}}{2} \right) + Q_{rrQ2} \right]$	$P_{sw(boost)} = V_{out} f_{sw} \left[I_{in} \left(\frac{t_{on\,Q4} + t_{off\,Q4}}{2} \right) + Q_{rrQ3} \right]$
MOSFET gate-driver loss	$P_{gate(buck)} = V_{cc} I_{gate(buck)} = V_{cc} f_{sw} \left(Q_{gQ1} + Q_{gQ2} \right)$	$P_{gate(boost)} = V_{cc} I_{gate(boost)} = V_{cc} f_{sw} \left(Q_{gQ3} + Q_{gQ4} \right)$
Deadtime conduction loss	$P_{deadtime(buck)} = V_d I_{out} f_{sw} \left(t_{dead_1} + t_{dead_2} \right)$	$P_{deadtime(boost)} = V_d I_{in} f_{sw} \left(t_{dead_3} + t_{dead_4} \right)$

Buck-Boost Region Power Dissipation

The corresponding expressions for power dissipation in buck-boost mode are given in Table 2. These are weighted combinations of the expressions in Table 1 consistent with the operating point within the buck-boost window and the switching frequency divided by two.

Table 2. Component power loss expressions when operating in the buck-boost region.

Mode	Buck-Boost	
	$V_{in} < V_{out}$	$V_{in} > V_{out}$
MOSFET conduction loss	$P_{cond(B-B)} = I_L{}^2 \times \left[D_{buck(\max)} R_{DS(on)Q1} + D_{buck(\max)}{}' R_{DS(on)Q2} + D_{boost(B-B)} R_{DS(on)Q4} + D_{boost(B-B)}{}' R_{DS(on)Q3} \right]$	$P_{cond(B-B)} = I_L{}^2 \times \left[D_{buck(B-B)} R_{DS(on)Q1} + D_{buck(B-B)}{}' R_{DS(on)Q2} + D_{boost(\min)} R_{DS(on)Q4} + D_{boost(\min)}{}' R_{DS(on)Q3} \right]$
Shunt loss	$P_{shunt(B-B)} = \left(D_{buck(\max)}{}' + D_{boost(B-B)} \right) R_s I_L^2$	$P_{shunt(B-B)} = \left(D_{buck(B-B)}{}' + D_{boost(\min)} \right) R_s I_L^2$
MOSFET switching loss	$P_{sw(B-B)} = V_{in} \frac{f_{sw}}{2} \left[I_L \left(\frac{t_{on\,Q1} + t_{off\,Q1}}{2} \right) + Q_{rrQ2} \right] + V_{out} \frac{f_{sw}}{2} \left[I_L \left(\frac{t_{on\,Q4} + t_{off\,Q4}}{2} \right) + Q_{rrQ3} \right]$	
MOSFET gate driver loss	$P_{gate(B-B)} = V_{cc} I_{gate(B-B)} = V_{cc} \frac{f_{sw}}{2} \left(\sum_{n=1}^{4} Q_{g_n} \right)$	
Deadtime conduction loss	$P_{deadtime(B-B)} = V_d I_L \frac{f_{sw}}{2} \sum_{n=1}^{4} t_{dead_n}$	

From equation 3, inductor current, I_L, is derived from the output current and the boost duty cycle. $D' = 1 - D$ is the duty cycle complement. Note that both tables show the classic idealized expressions for MOSFET switching loss.

Inductor And Bias Losses

As expected, inductor copper and core losses and bias regulator loss contributions also factor into efficiency calculations:

$$P_{L(copper)} = I_{L(rms)}^2 R_{dcr}$$
$$P_{L(core)} = K_m \, f_{sw}^{\alpha} \, \Delta I_L^{\beta} \qquad (7)$$
$$P_{LDO(bias)} = \left(V_{supply} - V_{cc}\right)\left(I_Q + I_{gate}\right) \quad .$$

The inductor's DCR is readily available from the inductor datasheet. For cores losses, the ac flux density is proportional to inductor peak-to-peak ripple current. Core loss expressions using the Steinmetz[9] parameters in equation 7 are typically obtained from the inductor vendor for the required switching frequency.

Meanwhile, controller quiescent current and total MOSFET gate-drive current are ultimately derived from input, output, or auxiliary system supply rails. Bias regulator power dissipation tracks the difference of supply rail and V_{CC} voltages.

Charting Efficiency And Losses

Using the converter implementation[6] shown in Fig. 5, plots of the four-switch buck-boost converter's efficiency and component power dissipation versus line and load were obtained as shown in Fig. 6. Considering losses in totality, the converter with 12-V regulated output quite readily achieves efficiencies in excess of 95% across wide ranges of output current and input voltage.

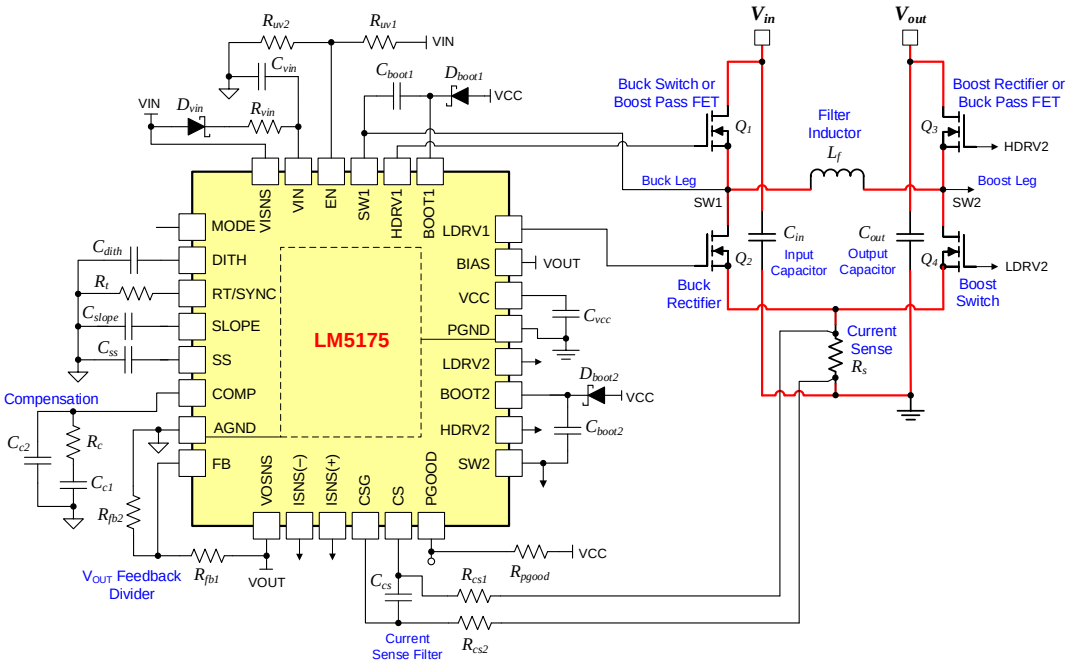

Fig. 5. Practical four-switch buck-boost converter schematic with peak/valley current-mode controller.

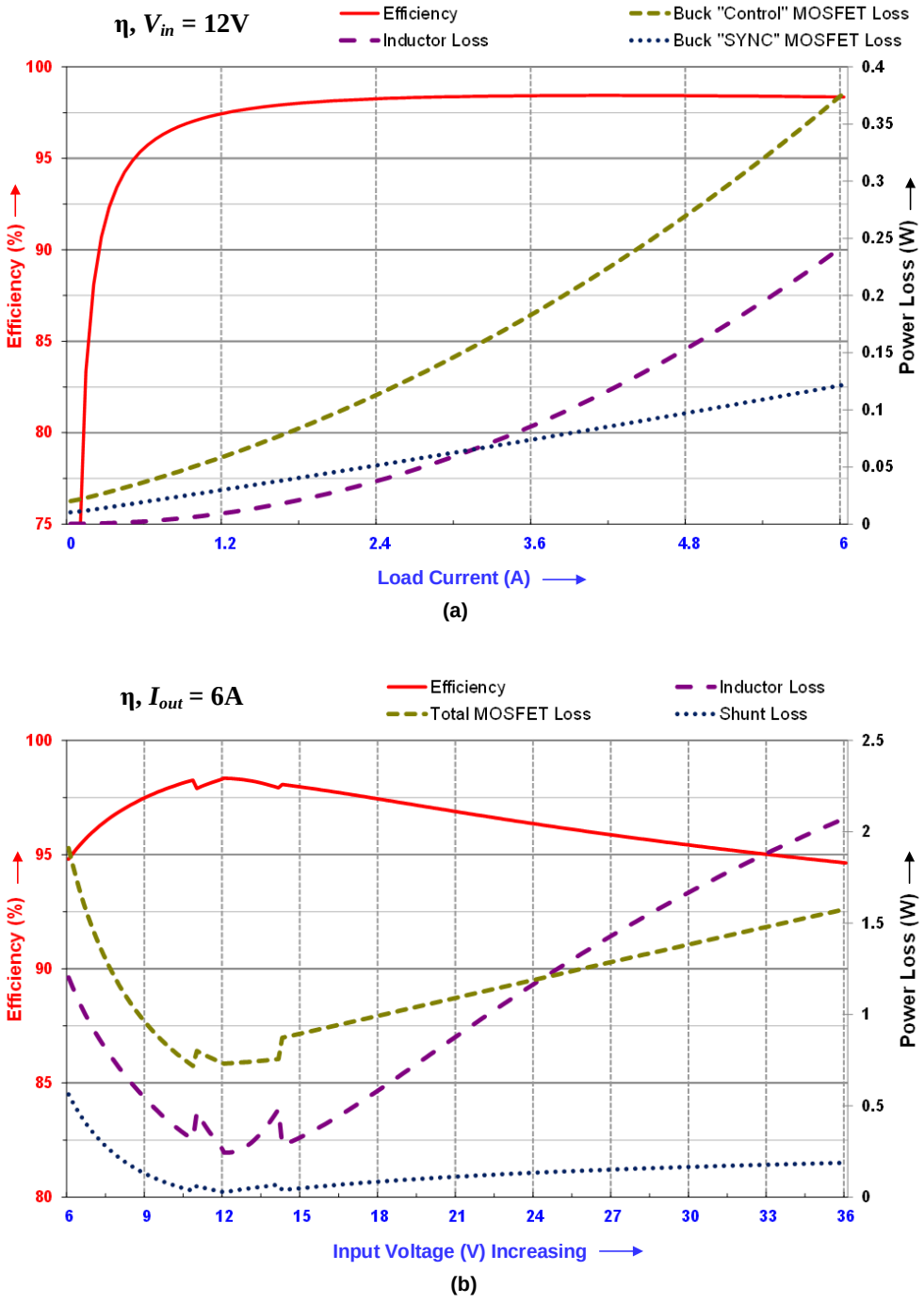

Fig. 6. Efficiency plots and component power loss breakdown versus load current (a) and input voltage (b). The buck-boost window is evident in the efficiency vs. line plot.

Summary

Fundamental to any dc-dc power converter design is the optimization of the power stage, both electrically and thermally. Not only can this amount to better performance and lower cost, it can also yield better reliability as a result of lower component temperatures as well as smaller solution size—both volume and footprint.

A converter with excessive component temperatures quite often forces a circuit design iteration that impacts project schedule, not to mention the undue expenditure of financial and managerial resources. Identifying the converter's switching modes and dissecting the expressions required to predict efficiency and power losses helps the designer to achieve a greater understanding of the converter's operation and—most of all—the nuances of its electrical and thermal behavior.

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