Understanding Op Amp Dynamic Response In A Type-2 Compensator (Part 2): The Two Poles

by Christophe Basso, ON Semiconductor, Toulouse, France

In part 1 of this article, we have shown the impact of the operational amplifier open-loop gain A_{OL} on the response of a type-2 compensator. Pushing the analysis further, a closer look at the magnitude and phase response of an operational amplifier reveals the presence of two poles—one low frequency and one high frequency. While the presence of these poles can be neglected in low-bandwidth compensator designs, you must account for the distortion they produce when you need gain and phase boost in high-bandwidth systems.

In this second part, we will see how to determine the transfer function of the type-2 compensator accounting for these poles and how they distort the response of the filter. As we will see, the op amp's poles and finite gain produce distortions in the gain and especially the phase characteristics of the compensator. Fortunately, these distortions can be minimized by appropriate selection of the op amp and we'll present a method for doing so. Finally, we'll apply our more-complete transfer function for the type-2 compensator in a design example consisting of a high-frequency, current-mode-controlled buck converter.

Two Poles In The Op Amp

For stability reasons, op amp designers implement what is called dominant-pole compensation. It consists of placing a pole at low frequency so that gain roll-off to 1 (0 dB) occurs at frequency f_c before a second high-frequency pole is placed, usually at $2f_c$.

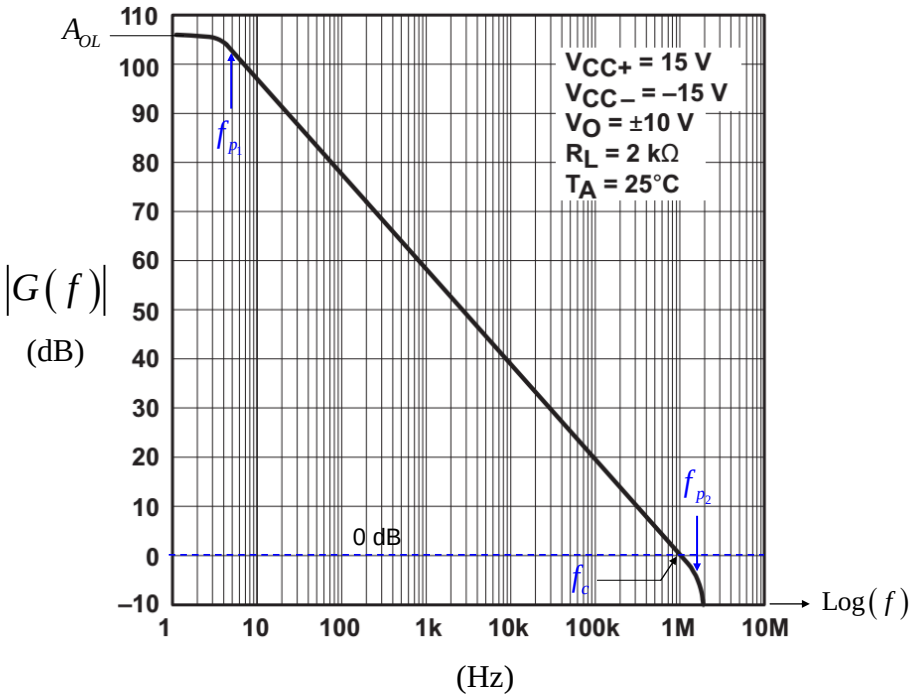


Fig. 1. The open-loop dynamic response of an op amp reveals the presence of two poles (f_{p1} and f_{p2}.)

This is what Fig. 1 illustrates for a classical µA741 in which you can observe a crossover frequency at 1 MHz. In this case, a low-frequency pole exists around 5 Hz while a second pole manifests itself at approximately 2 MHz.

Please note that this is a typical response with an open-loop gain A_{OL} of 106 dB. The open-loop gain is not a precisely-controlled parameter and it can vary quite significantly. The datasheet stipulates a gain moving from 15,000 (83.5 dB) to 200,000 (106 dB) across the whole temperature range (-55 to 125 °C). So expect this curve to shift as dispersions occur.

A simple Laplace expression can depict this two-pole open-loop response shown in Fig. 1:

$$G_{OL}(s) = \frac{A_{OL}}{\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)} \quad (1)$$

It is confirmed by the Mathcad plot appearing in Fig. 2.

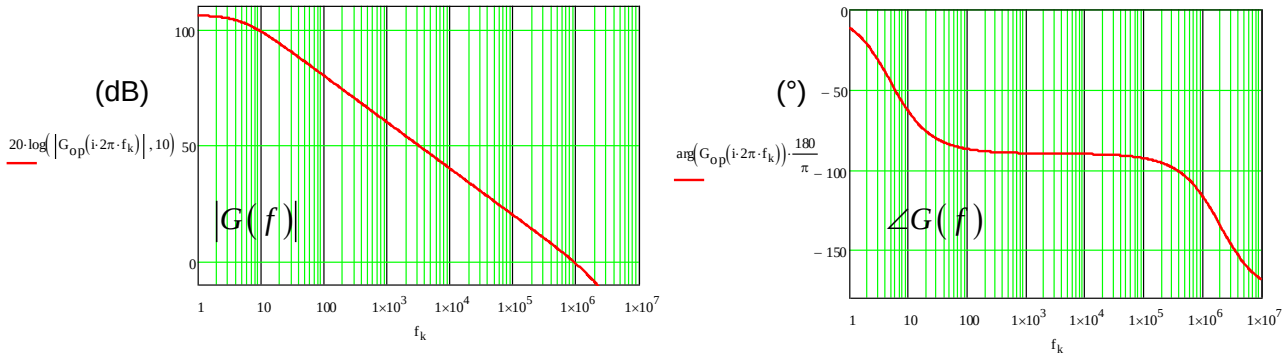


Fig. 2. The op amp features a low-frequency pole and a second pole placed beyond the 0-dB crossover frequency.

A Simple SPICE Model For The Op Amp

A SPICE model mimicking the frequency response of Fig. 2 can be built quite easily. As drawn in Fig. 3, it uses a voltage-controlled current source G_1 featuring a transconductance g_m followed by a resistor R_{OL} to ground in parallel with capacitor C_1. Across R_{OL}, the transfer function to the inverting pin V_{inv} is simply:

$$\frac{V_{R_{OL}}(s)}{V_{inv}(s)} = -\frac{g_m R_{OL}}{1+sR_{OL}C_1} \quad (2)$$

If we now buffer the voltage and place a second pole with resistor R_2 and capacitor C_2, we obtain the complete transfer function we want:

$$\frac{V_{out}(s)}{V_{inv}(s)} = -\frac{g_m R_{OL}}{(1+sR_{OL}C_1)(1+sR_2C_2)} \quad (3)$$

Component values have been automated on the left-side of Fig. 3 and once the simulation is run, the right-side displays the obtained magnitude/phase diagram. This is a simplified op amp model but it can be used for a first-order analysis. Later, it can be upgraded to model more specific characteristics such as voltage clamps or a slew-rate circuit as described in reference [1].

Please note the presence of *LoL* and *CoL* in the schematic. They are there to fix the op amp output voltage at 2.5 V as the part runs open loop. Here, because there are no supply rails, we could run a simple ac analysis without caring about the dc bias point.

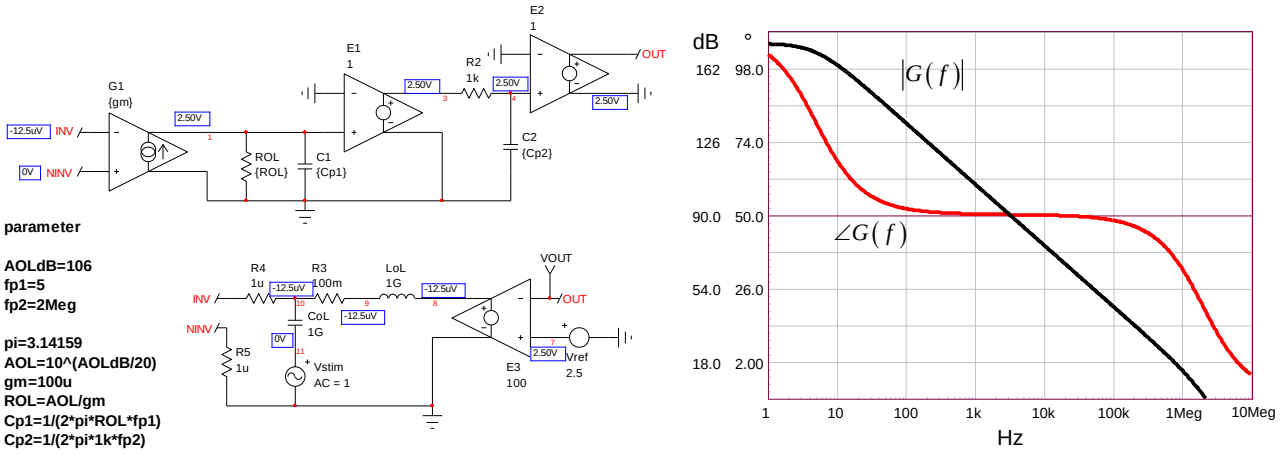


Fig. 3. A simple SPICE circuit lets you build an op amp featuring an open-loop gain and two poles.

However, if you plan to look at the response of a more comprehensive model including supply rails, then this simple circuit will prevent the integrated circuit from railing up or down as you attempt to manually fix its dc operating point. *LoL* is a short circuit at the beginning of the simulation and helps fixing the operating point with E_3 and source V_{ref}.

Once an ac sweep starts through *CoL*, *LoL* blocks the modulation from E_3 and the circuit fixing the operating point becomes silent. This is a classical trick used with average models to run an open-loop gain analysis while making sure the closed-loop bias point is established to the desired output value. This simple SPICE model will help to test the mathematical expression obtained through our analysis.

The Type-2 Compensator Featuring The Two-Pole Configuration

Now that we know our op amp features two extra poles, we can update the sketch we originally used in part 1 of this article. Fig. 4 shows the newly-formed type-2 compensator now including the op amp internal characteristics.

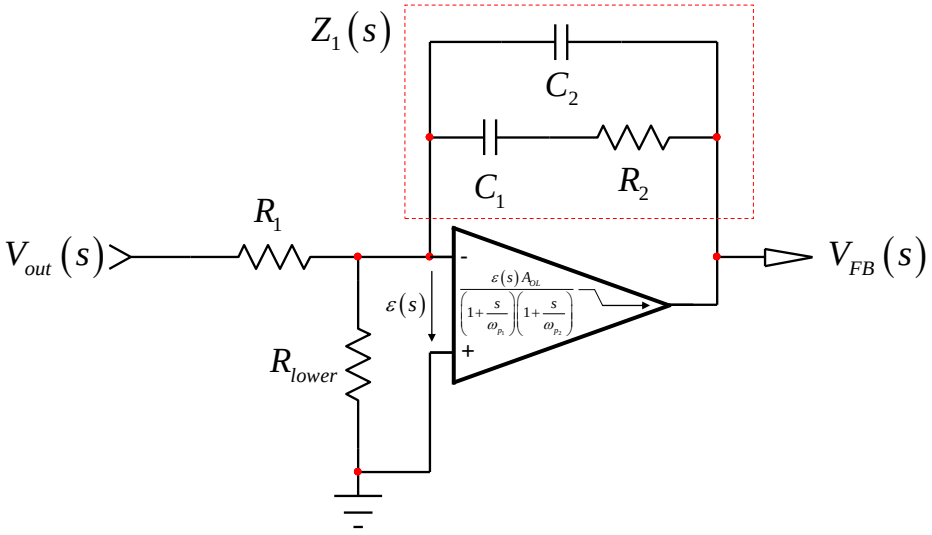


Fig. 4. The updated circuit accounts for the two poles present in the operational amplifier.

The output voltage V_{FB} is the error voltage ε multiplied by the op amp open-loop transfer function:

$$V_{FB}(s)=\varepsilon(s)\frac{A_{OL}}{\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)} \tag{4}$$

The error voltage can be found using the superposition theorem alternatively setting V_{out} and V_{FB} to 0 V:

$$\varepsilon(s)=-\left(V_{FB}(s)\frac{R_1 \parallel R_{lower}}{R_1 \parallel R_{lower}+Z_1(s)}+V_{out}(s)\frac{Z_1(s) \parallel R_{lower}}{Z_1(s) \parallel R_{lower}+R_1}\right) \tag{5}$$

If we now substitute (5) into (4) and rearrange the expression, we find:

$$G(s)=-\frac{A_{OL}\left[Z_1(s) \parallel R_{lower}\right]}{\left[R_1+Z_1(s) \parallel R_{lower}\right]\left[\frac{A_{OL}\left(R_1 \parallel R_{lower}\right)}{\left(Z_1(s)+R_1 \parallel R_{lower}\right)\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)}+1\right]}\frac{1}{\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)} \tag{6}$$

With $Z_1(s)$ equal to:

$$Z_1(s)=\frac{R_2C_1}{C_1+C_2}\frac{1+\frac{1}{sR_2C_1}}{1+sR_2\frac{C_1C_2}{C_1+C_2}} \tag{7}$$

Please read the appendix at the end of this paper to learn how I derived this expression in simple steps using fast analytical techniques.

This equation is awfully intractable (i.e. offering no analytical insight into circuit behavior by itself.) But fortunately, it is not a problem for Mathcad. We can verify if it is correct by comparing its dynamic response with that of the SPICE model. We assumed the following component values:

$R_1 = 3.8\ \text{k}\Omega$
$R_{lower} = 1\ \text{k}\Omega$
$C_1 = 1.8\ \text{nF}$
$C_2 = 93\ \text{pF}$
$A_{OL} = 106\ \text{dB}$
$\omega_{p_1} = 5\ \text{Hz}$
$\omega_{p_2} = 2\ \text{MHz}$

The SPICE circuit featuring the type-2 configuration is shown in Fig. 5.

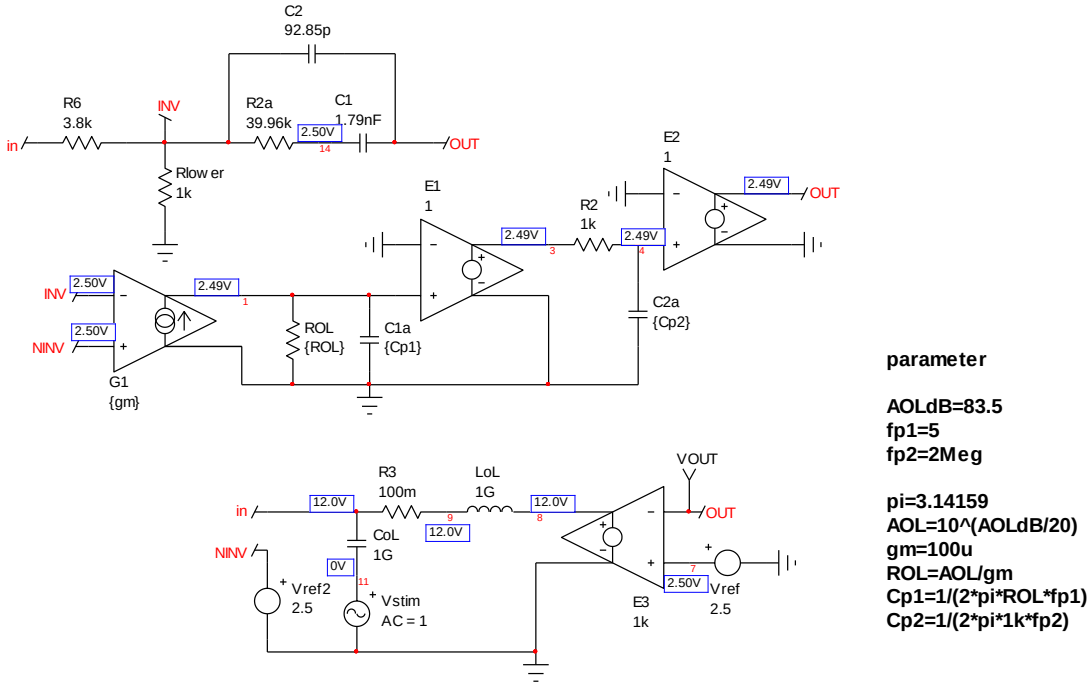


Fig. 5. The complete type-2 SPICE model now accounting for the op amp's dynamic response. Please note the dc bias point set to 12 V given the 2.5-V reference voltage Vref2 now biasing the NINV pin.

As confirmed by Fig. 6, responses between Mathcad and SPICE are identical confirming the validity of the equation.

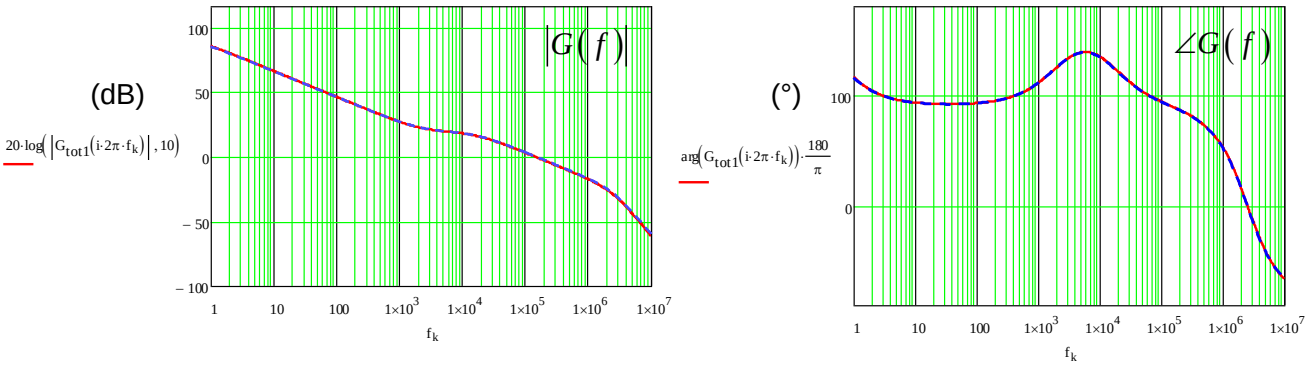


Fig. 6. The plots delivered by Mathcad perfectly superimpose on those produced by SPICE.

Distortion Of Characteristics

The component values adopted in the Fig. 5 simulation come from a type-2 compensator intended to build a 65° phase boost with a 20-dB gain at a 10-kHz crossover frequency. If we now compare the ideal type-2 response given by equation 36 in the first part of this article with the response of the type-2 circuit using a µA741 (106 dB A_{OL} with two poles, 5 Hz and 2 MHz), you will notice some discrepancies as indicated by Fig. 7.

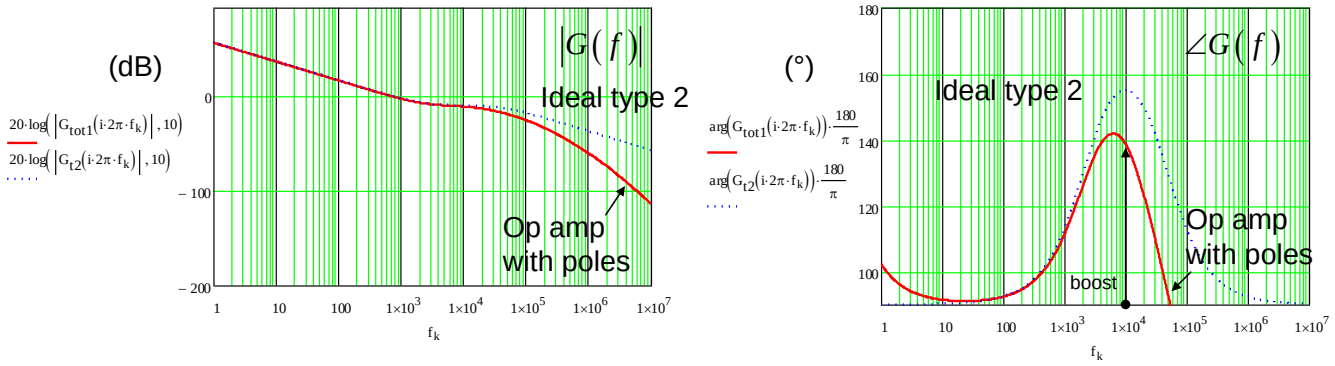


Fig. 7. Building the type 2 with a µA741 exhibiting its highest open-loop gain already induces phase boost distortion.

In this picture, we can observe a slight gain deviation at 10 kHz and the 20-dB target is missed by ≈2.2 dB. Not a big deal actually. But what is more important is the 65° phase boost you were expecting with the formula for the ideal op amp. At 10 kHz, the phase boost provided by the circuit featuring the real op amp is only 44.6° or a difference of 20.4°. This is going to reduce the final phase margin by that amount.

But the worst is yet to come. If you consider the open-loop gain variation as indicated by the datasheet, what if A_{OL} drops to 83.5 dB, the specified minimum for open-loop gain? Fig. 8 speaks for itself: the 20-dB gain at 10 kHz is missed by 17 dB while the phase boost collapses to 6.7°. No need to explain why the system's stability is at stake with this last value. The SPICE simulation from Fig. 9 confirms this data with the three different plots gathered in the same graph. You can see the deleterious impact of the open-loop gain variations.

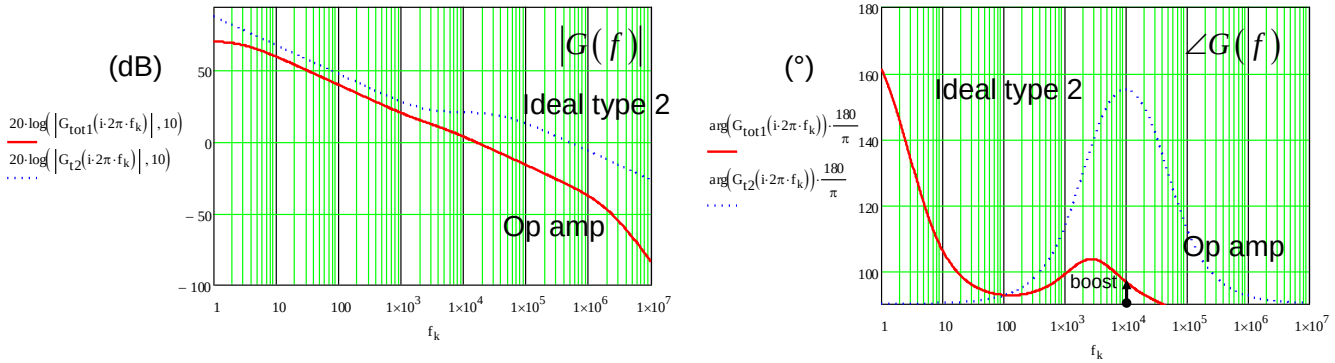


Fig. 8. If the open-loop gain now collapses to 83.5 dB as detailed in the op amp datasheet, the phase boost of the compensator almost disappears.

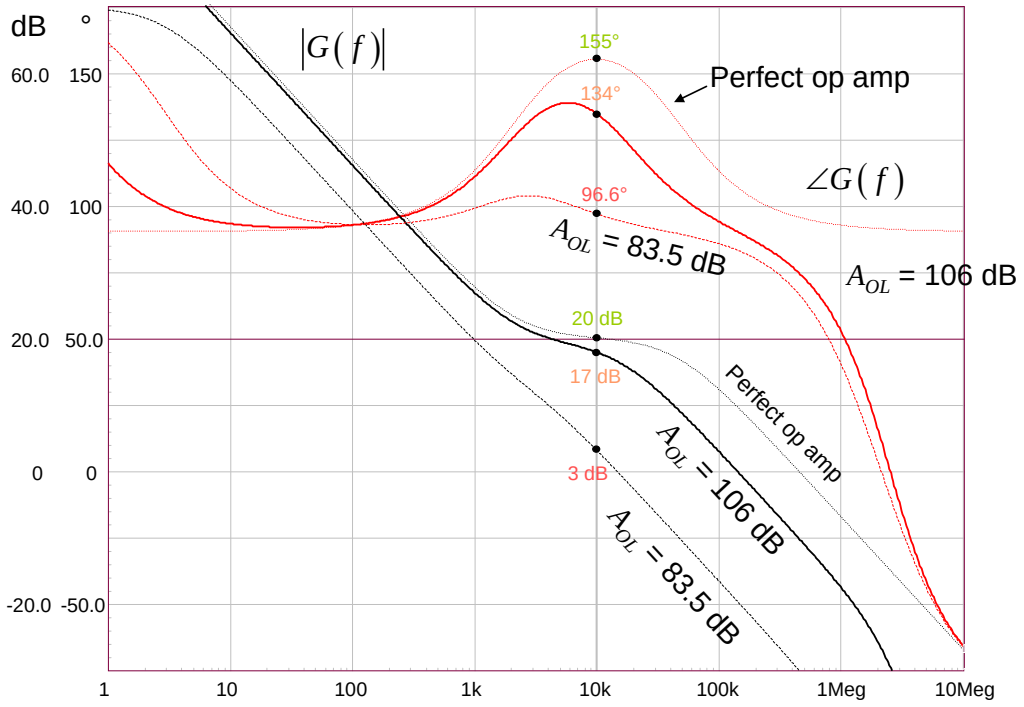


Fig. 9. Variations in the op amp open-loop gain induce severe gain and phase distortions.

If we now change the type-2 specifications, meaning we no longer need a gain at 10 kHz but a 10-dB attenuation at f_c with the same 65° phase boost, the phase boost distortion is less pronounced with the low open-loop gain (see Fig. 10.)

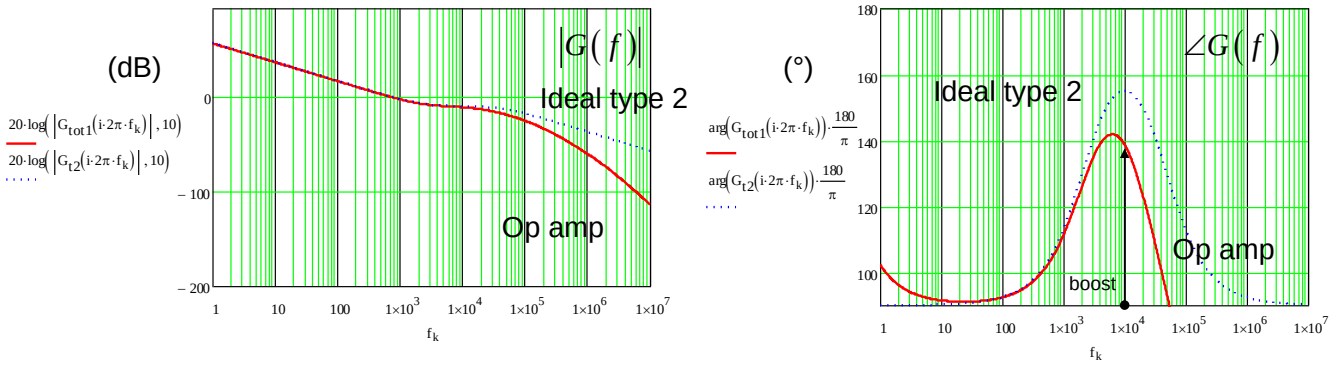


Fig. 10. If the type-2 circuit is modified to attenuate by 10 dB rather than amplifying at the same 10-kHz crossover frequency, the target for phase boost is still not attained but we're closer to the desired result.

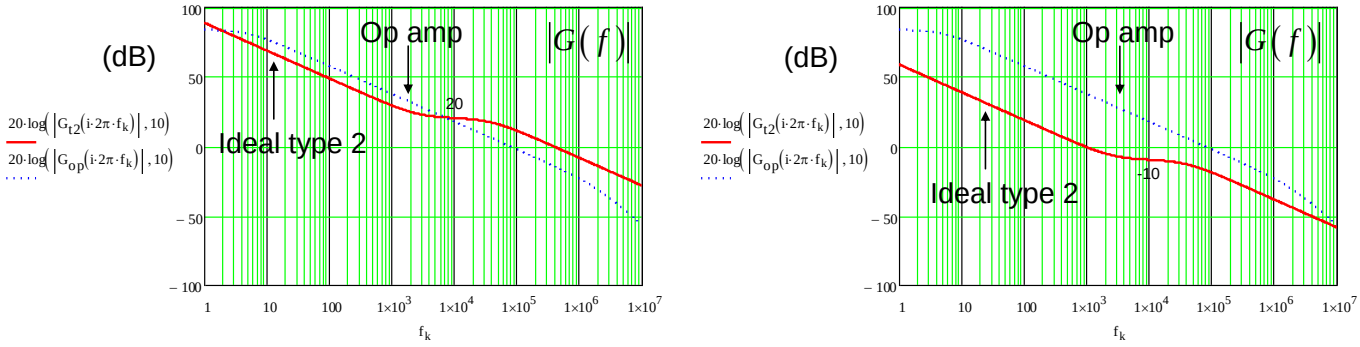
The mid-band gain obtained in this configuration is -11 dB (versus the -10-dB target) while the phase boost just hits 49° (versus the original 65° target.)

Type-2 Response And Open-Loop Gain Plots

The classical recommendation for making sure the op amp internals do not alter the compensator response is to superimpose on the same plot the theoretical type-2 magnitude and the op amp open-loop response.[2] In Fig. 11, the left-side plots correspond to our first attempt to build a type 2 compensator featuring a 65° phase boost and a 20-dB gain at 10 kHz. In this graph, the op amp magnitude intersects with that of the type 2

compensator and the conflict ends up destroying the characteristics we wanted (producing almost 60° phase error in the end.) At first sight, it is clear that this intersection shows that either the selected op amp is not adequate or the goals we set with the type-2 compensator were too ambitious.

The right-side of Fig. 11 seems to indicate that we should be good to go when designing that type-2 circuit which no-longer features gain but attenuation at the 10-kHz crossover. Our calculations unfortunately indicate otherwise as confirmed by the final 17° phase error.



A_{OL} = 83.5 dB and a need for a 20-dB gain at 10 kHz

A_{OL} = 83.5 dB and a need for a 10-dB attenuation at 10 kHz

Fig. 11. In the plots on the left, you clearly see that both responses intersect and degradation occurs. In those on the right, there is no intersection in the magnitude plots but the final result is also distorted.

One approach suggested in reference [2] recommends that we select an op amp featuring a gain-bandwidth product (GBW) greater than the 0-dB crossover frequency of the adopted type 3 compensator. You can see that, unfortunately, it does not apply to Fig. 11: On the left side, the 0-dB crossover for the type 2 is around 400 kHz while on the right side, we want an attenuation and not a gain.

Therefore, I propose a slightly different rule-of-thumb in which the op amp open-loop response must "fly" by 20 dB above the type-2 compensation at $20f_c$. This is what Fig. 12 illustrates. This graphical approach is a first step in determining what GBW product your op amp must exhibit to keep the wanted phase boost and gain targets within acceptable limits.

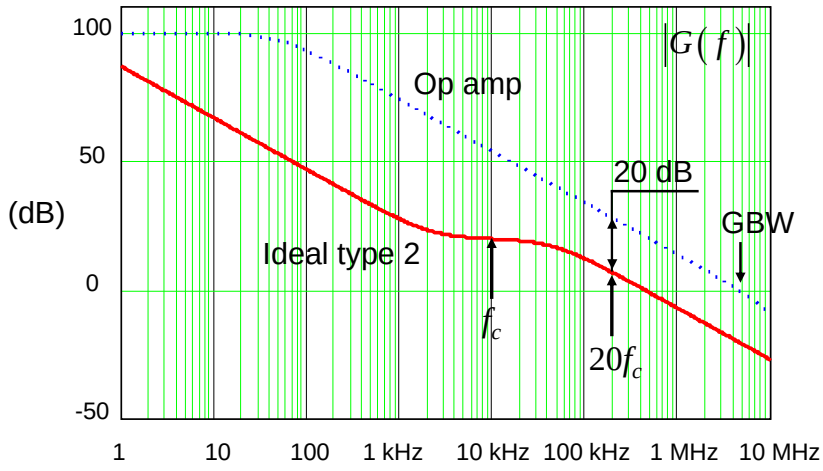


Fig. 12. As a first step in selecting the op amp, we recommend setting the open-loop response at least 20 dB above the second -1-slope of the type-2 compensator.

You first calculate the type 2 magnitude in dB at $20f_c$ to which you add 20 dB. Then you calculate the corresponding op amp open-loop gain crossover frequency or GBW product:

$$\mathrm{GBW} = 20 \cdot f_c \cdot 10^{\frac{\left[20\log_{10}\left|G(20 f_c)\right|\right]+20}{20}} \qquad (8)$$

In Fig. 11 left side, (8) gives a GBW product of 4.4 MHz while it suggests a GBW product of 150 kHz for the second case. Applying this strategy to the first example leads to the selection of an op amp having an open-loop gain of 90 dB with a low-frequency pole located at 150 Hz or an 80-dB open-loop gain with a 450-Hz low-frequency pole. Do not reduce the open-loop gain below 70 dB[2] to keep the steady-state error within acceptable limits. When this strategy is applied, the mid-band gain is 19.5 dB while the phase boost is ≈60°.

In the second example, (8) recommends a GBW of 140 kHz obtained with an 80-dB open-loop gain and a 15-Hz low-frequency pole. The mid-band gain dispersion is 0.4 dB and the phase boost is 56° or a 9° deviation. Pushing the low-frequency pole to 30 Hz reduces the gain dispersion to 0.2 dB and the phase boost error to 4.4°.

The formula in (8) is given to get you started in the selection of the GBW product of a suitable op amp. It is based on observations and iterations done to find suitable GBW products in several cases. I could have tried to extract a possible GBW product from (6)—for instance by ignoring the high-frequency pole contribution—to meet specific deviations from response of the original perfect type-2 compensator but I am not sure a meaningful expression could have been identified.

Once you have the suggested GBW in hand, look up the datasheets of operational amplifiers and identify a suitable component. Then, plug A_{OL} and the low-frequency pole into the Mathcad sheet [3] and check for the incurred target deviations. Be sure to explore minimum values so that deviations remain acceptable in the worst case.

Compensation Example: A High-Frequency Current-Mode Buck Converter

Assume that we have designed a 5-A buck regulator converting a 3.7-V battery down to 1.5 V and switching at a 1-MHz frequency. The output capacitor is 180 µF and features an equivalent series resistance (ESR) r_C of 3 mΩ. Assume we want a 50-mV drop on the output when the load changes from 1.5 A to 5 A. The power supply output impedance must thus be equal to:

$$Z_{out} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{50m}{5-1.5} = 14.3\,\text{m}\Omega \tag{9}$$

It is possible to show that the small-signal closed-loop output impedance at the crossover frequency f_c is dominated by the capacitor impedance providing that its ESR is small enough:

$$\text{If } r_C << Z_{C_{out}} @ f_c \rightarrow \Delta V_{out} \approx \Delta I_{out} \frac{1}{2\pi f_c C_{out}} \tag{10}$$

From the required drop, we can estimate what crossover frequency is needed considering the 180-µF capacitor and the desired 14.3-mΩ output impedance:

$$f_c \approx \frac{1}{2\pi Z_{out} C_{out}} = \frac{1}{2\times 3.14159\times 14.3m\times 180u} = 62\,\text{kHz} \tag{11}$$

Some will object that this is an approximation for a small-signal analysis and large-signal response will be different. This is true but experience shows that final results are not that far from what is calculated. Of course, when ESR and ESL (parasitic inductance) enter the picture, the result drastically differs but this first-order approach is an interesting starting point. Furthermore, this method analytically suggests a crossover frequency compared to the classical recommendations of $F_{sw}/5$ or $F_{sw}/10$ which are often pulled out of thin air.

We have selected a crossover frequency f_c of 62 kHz. To compensate such a converter, we first need the power stage dynamic response, it is the starting point of the analysis. There are several ways to get it: a) use the control-to-output transfer function $H(s)$ and get a Bode plot from it b) build a simulation setup using an average model c) build a prototype in the laboratory and extract the response with a network analyzer or d) build a switching model and extract the ac response with Simplis or PSIM. We have adopted strategy b) as shown in Fig. 13.

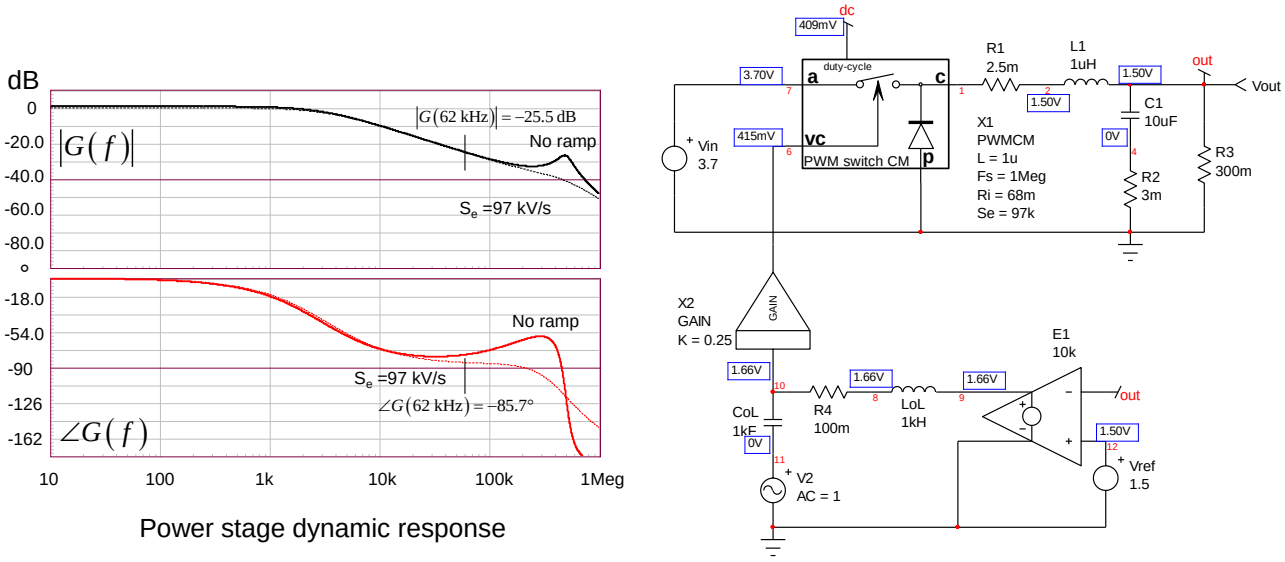


Fig. 13. An average model helps us build a current-mode converter quite quickly.

From the magnitude plot, we see that the mid-band gain must be 25.5 dB if we want to crossover at 62 kHz. The ≈86° phase lag read at crossover (pfc) requires a phase boost of the following value if we target a 70° phase margin (pm):

$$\text{Boost} = \text{pm} - \text{pfc} - 90 = 70 - (-86) - 90 = 66° \quad (12)$$

Calculations from the Mathcad sheet suggest a pole placed at 291 kHz with a zero located at 13.2 kHz. According to (8), a 50-MHz GBW amplifier must be selected. Looking up the various op amp datasheets, we found the LT1208. This device features a typical open-loop gain of 7000 (≈77 dB), which can drop to 2000 (66 dB) at its minimum value. Its typical gain-bandwidth product is 45 MHz and drops to 34 MHz at a ±5 V supply. The low-frequency pole is therefore placed at 34 MHz/7k ≈ 4.8 kHz.

Fig. 14 displays the type-2 Bode plots obtained with two different open-loop gains. The 77-dB gain gives a 45-MHz GBW and the deviation in gain (as indicated by ΔG) is small. When A_{OL} drops to 66 dB (the minimum specification), the gain deviation remains acceptable but the phase boost diverges from the target by 10.7°.

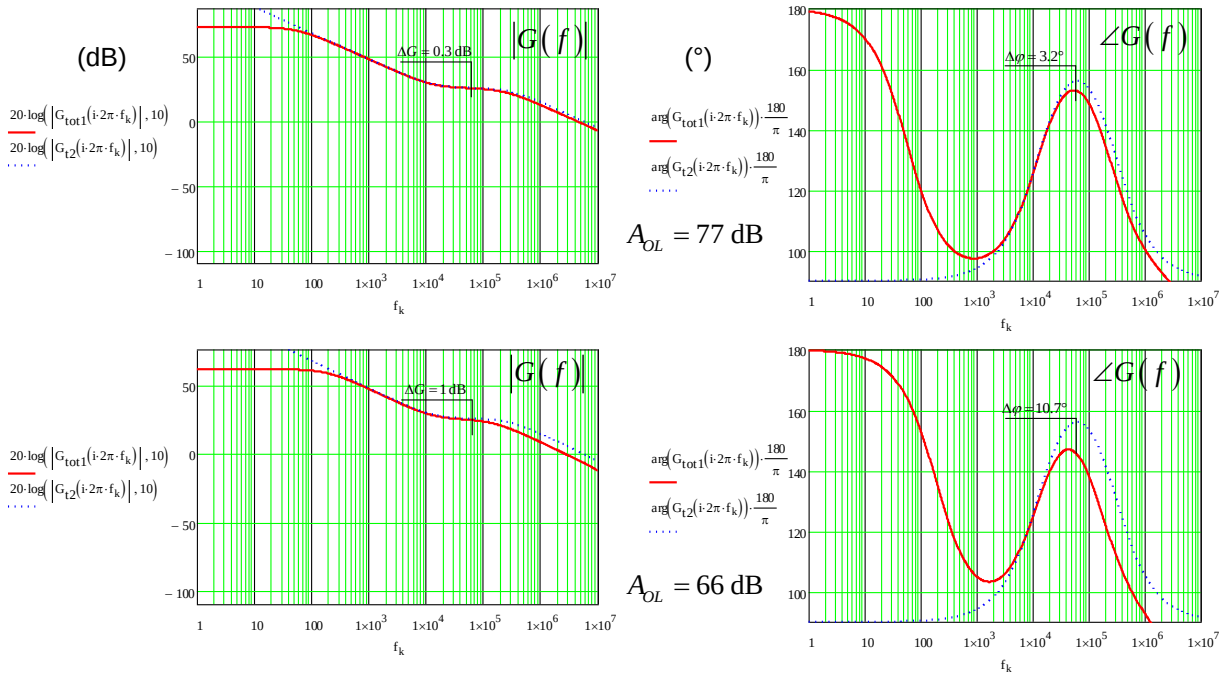


Fig. 14. The open-loop gain deviation affects the effective phase boost you will have at the end.

The Op Amp In the Buck Converter

We can now close the loop and capture the selected op amp characteristics in our simulation schematic, which is updated with the real model (at least with its A_{OL} and the two poles).

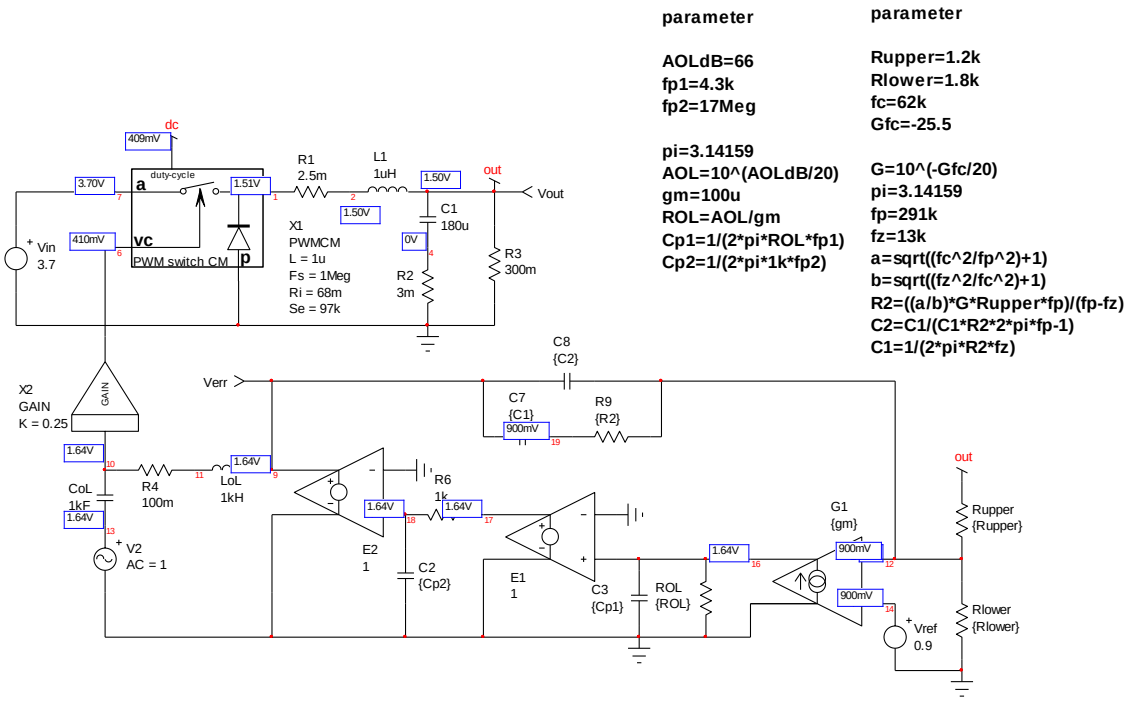


Fig. 15. The operational amplifier now features the two low- and high-frequency poles.

From this schematic, we can plot the open-loop gain $T(f)$ and see how the changes in the open-loop affect the dynamic response. The results appear in Fig. 16. As expected, some variation occurs in the crossover frequency and the phase margin.

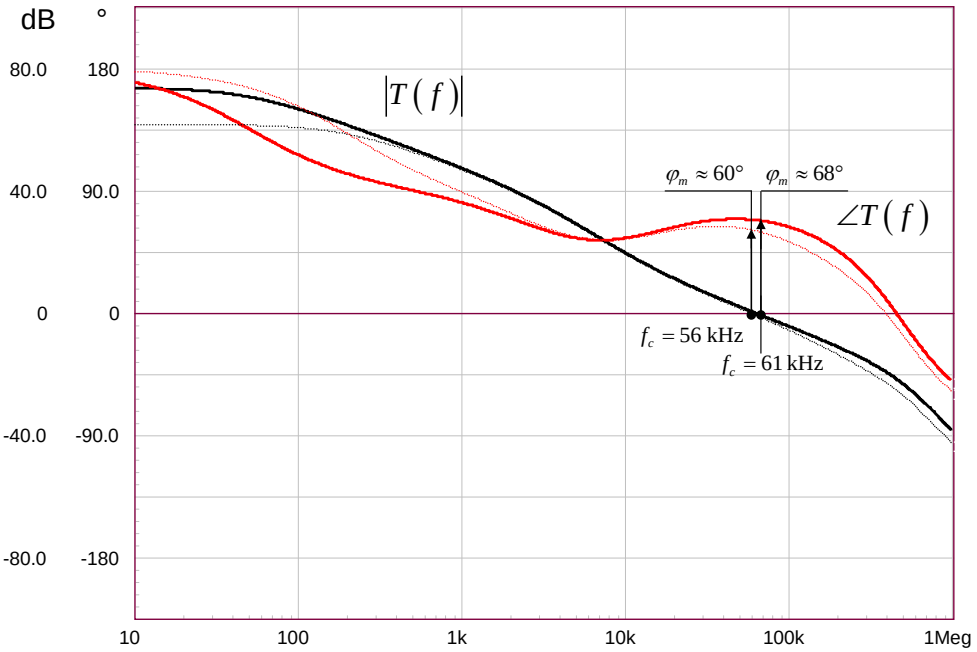


Fig. 16. The dynamic response is affected by the open-loop gain variations. In the worst case (66-dB A_{OL}), the phase margin drops to around 60° which is acceptable (dotted lines).

From the Fig. 15 simulation circuit, we can run a transient load step and check the response for the two different open-loop gains. The results are given in Fig. 17.

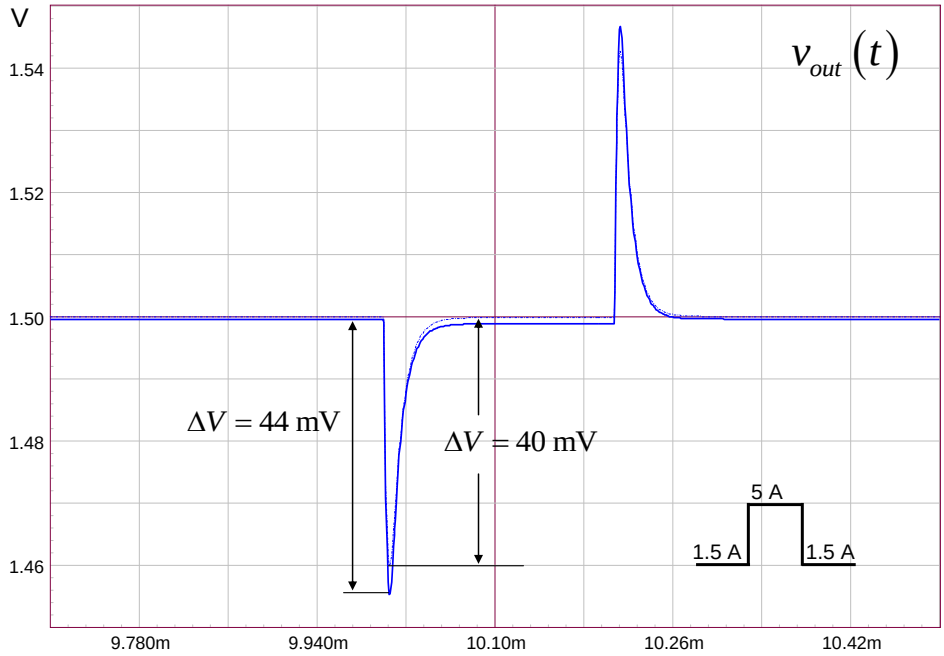


Fig. 17. The lowest open-loop gain gives a 44-mV deviation while the typical value induces a 40-mV drop (dotted lines correspond to the 66-dB A_{OL})

The drop is within the specifications for both open-loop gain values. Of course, this is a simplified approach and given the error voltage deviation on the op amp (1.6 V), the slew-rate must be part of the whole analysis and its impact assessed on the transient response.

Conclusion

This second part has shown some of the effects brought by the op amp dynamic response on the compensator performance. When a large bandwidth is expected, you can no longer neglect these contributions to the compensator dynamic response. Superimposing the ideal type-2 response you want with that of the selected op amp open-loop magnitude plot and checking for overlap is one way to go. However, we have seen a case where the absence of overlap leads to a significant phase boost distortion in the end.

By ensuring a significant distance between the op amp open-loop response and that of the perfect type 2, you can pick a gain-bandwidth product and check how it impacts the desired response with the given formula. A comprehensive stability analysis must consider the whole loop gain by affecting tolerances of all components, including the op amp internals. With the complete type-2 transfer function from (6), you are all set to push the analysis one step further.

References

1. "Practical Implementation of Loop Control in Power Converters" by Christophe Basso, APEC 2015 Professional Seminar, Charlotte, NC.
2. "Error Amplifier Limitations in High-Performance Regulator Applications" by Timothy Hegarty, AN-1997, Texas-Instruments, May 2013.
3. http://cbasso.pagesperso-orange.fr/Spice.htm

4. "Linear Circuit Transfer Functions – An Introduction to Fast Analytical Techniques" by Christophe Basso, Wiley 2016, ISBN 978-1-119-23637-5.

Appendix: Impedance Calculation

To determine the impedance given by (7), we can apply the Fast Analytical Techniques thoroughly described in reference [4]. The schematic appears in Fig. 18. To obtain the impedance, we use a current source I_T injecting current into the network. I_T is the *stimulus* while V_T is the *response*. The transfer function we want is the relationship linking the response to the stimulus. To ease the analysis, we have installed a dummy resistance R_{inf} across the measurement terminals. We will see in a moment the reason of it.

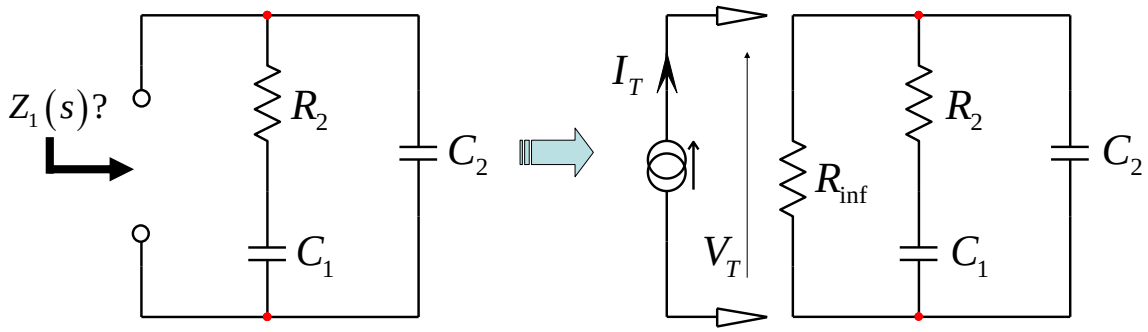


Fig. 18. There are two capacitors, this is a second-order circuit.

The transfer function of such a network can be put in the following form:

$$Z(s) = R_0 \frac{N(s)}{D(s)} \tag{13}$$

For a second-order system, we can show that the denominator obeys the following formula:

$$D(s) = 1 + b_1 s + b_2 s^2 = 1 + s(\tau_1 + \tau_2) + s^2(\tau_1 \tau_2^1) \tag{14}$$

τ_1 and τ_2 are the time constants obtained when all energy-storage elements—the capacitors and inductors—remain in their dc state (capacitors are open-circuited while inductors are shorted). The notation τ_2^1 means that the element in time constant 1 (the superscripted number) is put in its high-frequency state (capacitors are short-circuited while inductors are open-circuited) while you determine the resistance seen from time constant 2 element's terminals.

Conversely, τ_1^2 means that the element in time constant 2 (the superscripted number) is put in its high-frequency state (capacitors are short-circuited while inductors are open-circuited) while you determine the resistance seen from time constant 1 element's terminals. Then you assemble these time constants to form $D(s)$ as in (14).

First we look at the resistance offered from the energy-storage element's terminals for $s = 0$. In dc, we open all capacitors and short inductors (if any). SPICE does the same when determining a bias point prior to starting any type of analysis, .TRAN or .AC. In our head, we see that if we remove the capacitors, the resistance offered by the input terminals is fixed by R_{inf}, hence its presence to avoid an infinite term:

$$R_0 = R_{inf} \tag{15}$$

Then, we determine the resistance *R* offered by each capacitor's terminals while its counterpart is left in a dc state (open or removed from the circuit). We obtain the small drawings of Fig. 19. The time constant is defined by $\tau = RC$.

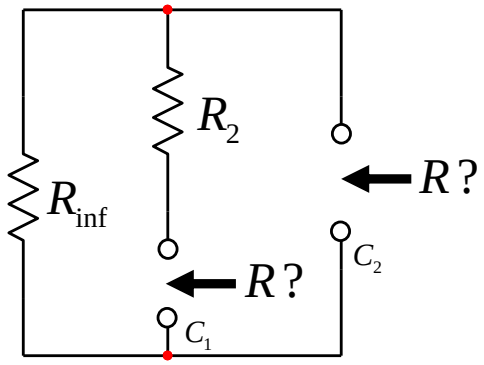


Fig. 19. You now evaluate the resistance offered by each capacitor's terminals while they are in their dc state (removed from the circuit).

Without writing a single line of algebra, we can inspect the figure and "see" the resistance observed from the capacitor's terminals. We have:

$$\tau_1 = C_1\left(R_2 + R_{inf}\right) \tag{16}$$

and

$$\tau_2 = C_2 R_{inf} \tag{17}$$

Now that have the dc time constants, let's determine the higher frequency one as shown in Fig. 20. For τ_2^1, capacitor C_1 is replaced by a short circuit and you look at the resistance offered by capacitor C_2's terminals.

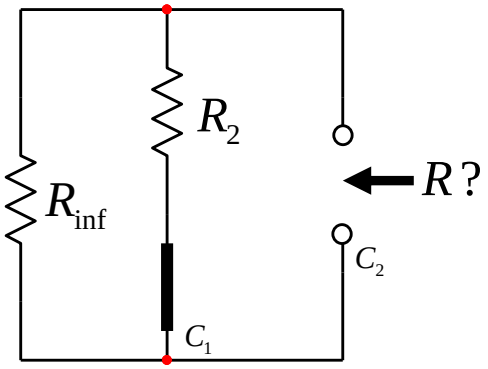


Fig. 20. Capacitor C_1 is replaced by a short circuit: what is the resistance "seen" from C_2's terminals?

The time constant is immediate and equal to:

$$\tau_2^1 = C_2\left(R_{inf} \parallel R_2\right) \tag{18}$$

Should we evaluate τ_1^2 instead, we would find

$$\tau_1^2 = C_1 R_2 \tag{19}$$

We have all the terms to form $D(s)$:

$$D(s) = 1 + s(\tau_1 + \tau_2) + s^2(\tau_1 \tau_2^1) = 1 + s\left[C_1(R_2 + R_{\text{inf}}) + C_2 R_{\text{inf}}\right] + s^2 C_1(R_2 + R_{\text{inf}}) C_2(R_{\text{inf}} \parallel R_2) \tag{20}$$

The numerator can be found by inspection. If you remember what I said in part 1, zeros are found when a specific value of *s* makes the response disappear in a transformed network (where is *C* is replaced 1/*sC*) despite the presence of a stimulus. In Fig. 18, the response is V_T measured across the current source. For V_T to become 0 V, there must be a transformed short circuit appearing in the circuit. This is the case if:

$$R_2 + \frac{1}{s_z C_1} = \frac{s_z R_2 C_1 + 1}{s_z C_1} = 0 \tag{21}$$

This is true if:

$$s_z = -\frac{1}{R_2 C_1} \tag{22}$$

We are all set, the complete transfer function is shown below:

$$Z_1(s) = R_{\text{inf}} \frac{1 + sR_2C_1}{1 + s\left[C_1(R_2 + R_{\text{inf}}) + C_2 R_{\text{inf}}\right] + s^2 C_1(R_2 + R_{\text{inf}}) C_2(R_{\text{inf}} \parallel R_2)} \tag{23}$$

In the denominator, factor R_{inf} and obtain:

$$Z_1(s) = R_{\text{inf}} \frac{1 + sR_2C_1}{R_{\text{inf}}\left\{\frac{1}{R_{\text{inf}}} + s\left[C_1\left(\frac{R_2}{R_{\text{inf}}} + 1\right) + C_2\right] + s^2 C_1\left(\frac{R_2}{R_{\text{inf}}} + 1\right) C_2 \frac{R_2}{1 + \frac{R_2}{R_{\text{inf}}}}\right\}} \tag{24}$$

Simplify and have R_{inf} approach infinity. The final expression is therefore:

$$Z_1(s) = \frac{1 + sR_2C_1}{s\left[C_1 + C_2\right] + s^2 C_1 C_2 R_2} \tag{25}$$

If you now factor R_2C_1 in the numerator, you have a so-called *low-entropy* expression featuring an inverted zero in the numerator:

$$Z_1(s) = \frac{R_2C_1}{C_1 + C_2} \frac{1 + \frac{1}{sR_2C_1}}{1 + sR_2 \frac{C_1C_2}{C_1 + C_2}} \tag{26}$$

It can be further rearranged in the following form:

$$Z_1(s) = Z_{mb}\frac{1+\frac{\omega_z}{s}}{1+\frac{s}{\omega_p}} \tag{27}$$

$$Z_{mb} = \frac{R_2C_1}{C_1+C_2} \tag{28}$$

$$\omega_z = \frac{1}{R_2C_1} \tag{29}$$

$$\omega_p = \frac{1}{R_2\frac{C_1C_2}{C_1+C_2}} \tag{30}$$

The leading term (28) still has the dimension of a resistance but is no longer the value for $s = 0$. It is the plateau region or mid-band resistance you see in Fig. 21 in which we gathered all expressions to test their individual responses. They are all identical.

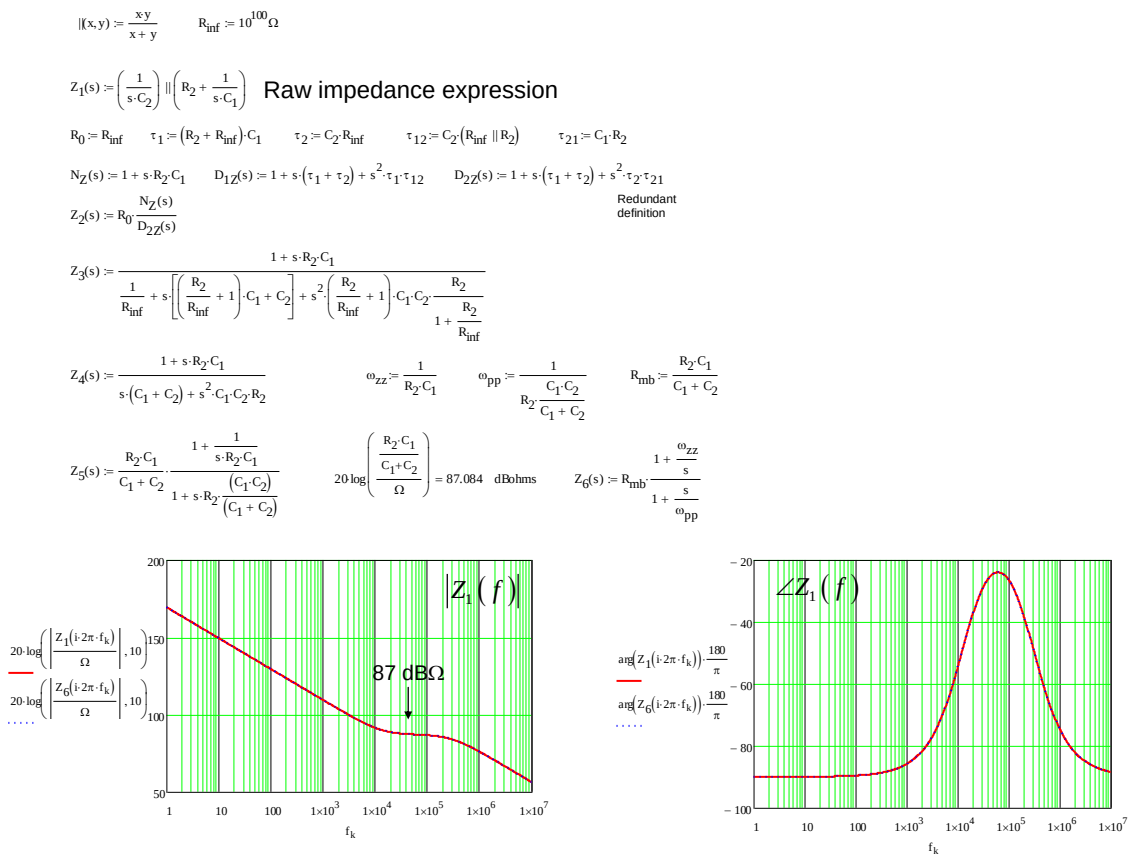


Fig. 21. Mathcad confirms that raw and final expressions are identical.

The Fast Analytical Circuits Techniques show how you can break a circuit into small individual sketches and solve each sketch independently. When inspection is possible, the result is obtained quite quickly and leads to a well-ordered form. This is the power of the approach and I encourage you to acquire the skill as you will save valuable time when determining a complicated transfer function.

To whet your appetite, look at Fig. 22. You will recognize a type-3 compensator. Without writing a single line of algebra, I can tell you that the response V_{FB} disappears when Z_1 and Z_2 respectively become a transformed short and a transformed open. Z_1 has already been evaluated in (26) and contributes a zero equal to:

$$\omega_{z_1} = \frac{1}{R_2 C_1} \tag{31}$$

To prevent the stimulus V_{out} from forming the response V_{FB}, the second option is that Z_2 becomes an open-circuit. In other words, for $s = s_{z2}$, the denominator of its impedance expression cancels.

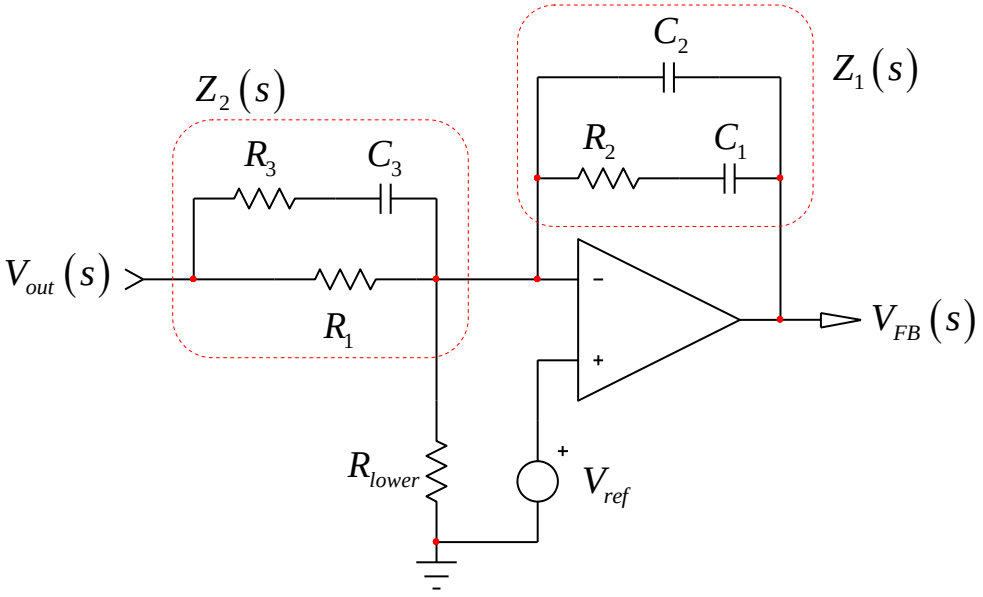


Fig. 22. A type-3 circuit is a third-order active filter.

To determine Z_2's impedance (isolate it from the whole circuit), we can imagine in our head a current source I_T connected across R_1 as shown on the right side of Fig. 18. For $s = 0$, the resistance you would "see" across the current source terminals is R_1 (C_3 is open-circuited in dc). The time constant when the excitation (the current source) is reduced to 0 A (a 0-A current source simply disappears from the circuit) is the resistance R seen from C_3's terminals times C_3. It is simply $\tau_3 = (R_1 + R_3)C_3$.

We do not need the numerator as we are only interested in the denominator's root. However, should you want the numerator also, it is the same structure as when we analyzed Z_1. The response V_T across the current source disappears if R_3 and C_3 become a transformed short. Once you have assembled this data, you have:

$$Z_2(s) = R_1 \frac{1 + sR_3C_3}{1 + s(R_1 + R_3)C_3} \tag{32}$$

To cancel the denominator and have this impedance magnitude approach infinity, you must solve:

$$1+s_{z_2}\left(R_1+R_3\right)C_3=0 \tag{33}$$

leading to

$$s_{z_2}=-\frac{1}{C_3\left(R_1+R_3\right)} \tag{34}$$

The intermediate type 3 transfer function is thus:

$$G(s)=G_0\frac{\left(1+\frac{s}{\omega_{z_1}}\right)\left(1+\frac{s}{\omega_{z_2}}\right)}{D(s)} \tag{35}$$

in which

$$\omega_{z_1}=\frac{1}{R_2C_1} \tag{36}$$

$$\omega_{z_2}=\frac{1}{\left(R_1+R_3\right)C_3} \tag{37}$$

and

$$G_0=-A_{OL}\frac{R_{lower}}{R_{lower}+R_1} \tag{38}$$

To determine *D*(*s*), you will have to bone up on [4].☺

About The Author

Christophe Basso is a technical fellow at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "Linear Circuit Transfer Functions: An Introduction to Fast Analytical Techniques."

Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 18 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on power supply compensation, see the How2Power Design Guide, and do a keyword search on "compensation."