ISSUE: January 2018

Online Simulation Validates Output Error Budget Analysis For Buck Converter

by Brooks Leman, Mark Fortunato and Nazzareno (Reno) Rossetti, Maxim Integrated, San Jose, Calif.

A buck converter design for a particular Maxim customer specified a tight output voltage tolerance across all operating conditions. To ensure the ensuing design met this goal, it was necessary to perform an output voltage error budget analysis. In general, the biggest contributor to the error is the output droop consequent to the load step. However, using different methods to estimate the droop led to different results. How do we make sense of it?

In this article, we perform a buck converter output error budget analysis. In estimating the droop amplitude, we compare a simulated result with two different back-of-the-envelope estimates and reconcile the different approaches.

The Error Budget

For this calculation, the buck converter parameters of interest are:

- V_{IN} = 5 V
- V_{OUT} = 3.3 V
- V_{OUT} dc accuracy ±2% = ±66 mV
- Output voltage droop error budget: V_{ERROR} = 240 mV.

The other defining elements of the buck converter are:

- Clock frequency = 695 kHz
- L = 2.7 µH
- C = 2 x 22 µF.

The design for this buck converter is created with the online EE-Sim DC-DC Converter Design Tool. Simulation results provided by this tool indicate the following:

V_{OUT} ripple = 2.6 mVpp or ≈ ±1.3 mV (Fig. 1)

V_{OUT} transient droop from 1 A to 2 A = 157 mV (Fig. 2)

Accordingly, the estimated worse-case error budget (negative deviation of the output voltage) is:

V_{ERROR} = 66 + 157 + 1.3 = 224.3 mV

The given target error budget is 240 mV against an estimated error of 224.3 mV. All is well, but as we will see, the result is not in line with our back-of-the-envelope calculations. Why?

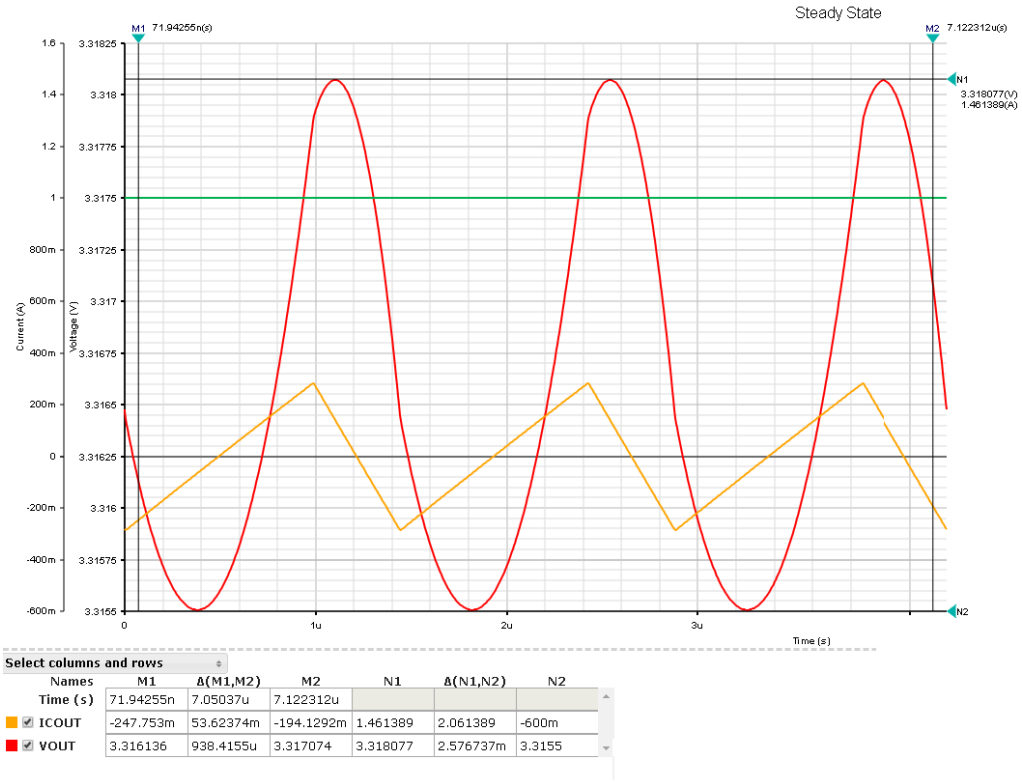

Fig. 1. Buck converter output voltage ripple (red) and capacitor current (yellow).

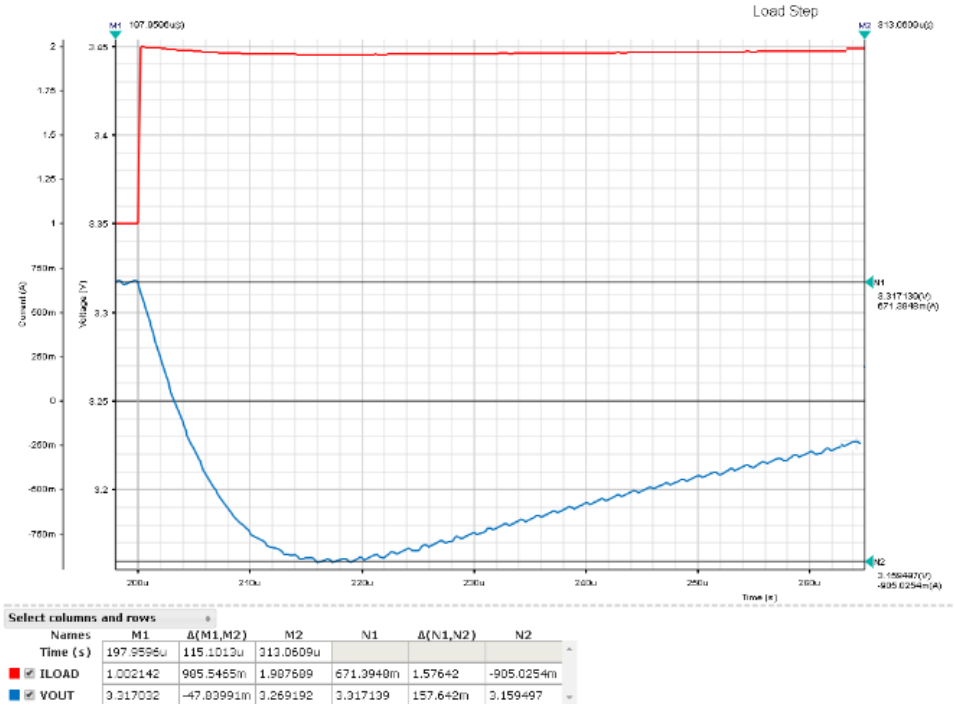

Fig. 2. Buck converter load step (red) and response (blue).

CdV/dt Back-Of-The-Envelope Estimate

A formula often used for this calculation is:

$$V_{droop} = \frac{I}{2\pi\, x f_{BW}\, x\, C} \qquad (1)$$

where I is the load step (1 A), C is the output capacitor (2 x 22 µF) and f_{BW} is the regulator closed-loop bandwidth. For the closed-loop bandwidth, f_{BW}, one can take a fraction of the clock frequency as a set value. In Fig. 3, we have the luxury of an online simulation, which determines the bandwidth more exactly as the point where the control loop gain curve crosses 0 dB. In this case, the bandwidth is 18.8 kHz.

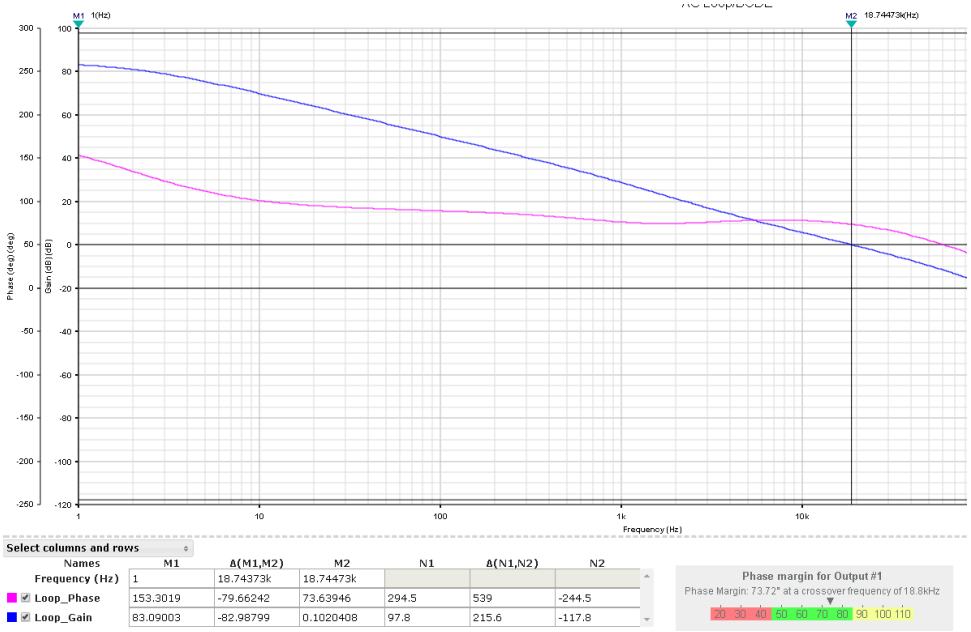

Fig. 3. Buck converter closed-loop bandwidth (blue) and phase margin (purple).

The rationale for this formula (equation 1) is that if the load step is steep the capacitors take all the hit, linearly discharging according to the law:

$$\frac{V_{droop}}{\tau} = \frac{I}{C} \qquad (2)$$

where τ is the discharge time. The capacitor's discharge lasts until the loop responds after a delay proportional to the inverse of the closed-loop bandwidth, f_{BW}:

$$\tau = \frac{1}{2\pi f_{BW}} \qquad (3)$$

By substitution of equation (3) into equation (2), we get equation (1). With this formula, the estimated droop for our buck converter example is:

$$V_{droop} = \frac{1}{2\pi\, x 18.8k\, x\, 44.6\mu} = 190\ mV$$

Note that an unusual capacitance value, 44.6 µF, is used. This is because high-density ceramic capacitors have capacitance that can vary dramatically with applied voltage. We use the actual capacitance with a bias of V_{OUT} (3.3 V) based on data provided by the device manufacturer and used by the EE-Sim design tool. This leads to a total error of:

V_{ERROR} = 66 + 190 + 1.3 = 257.3 mV

257.3 mV is above the 240 mV budget. This is the estimate we are concerned about. At first, the rationale for the formula appears to be sound, but what is wrong with it?

LC Resonant Back-Of-The-Envelope Estimate

The first thing we notice is that the formula completely neglects the presence of the inductor (2.7 µH). During the time the loop is unresponsive, the output is essentially an LC resonant circuit as shown in Fig. 4 (a SIMPLIS simulation).

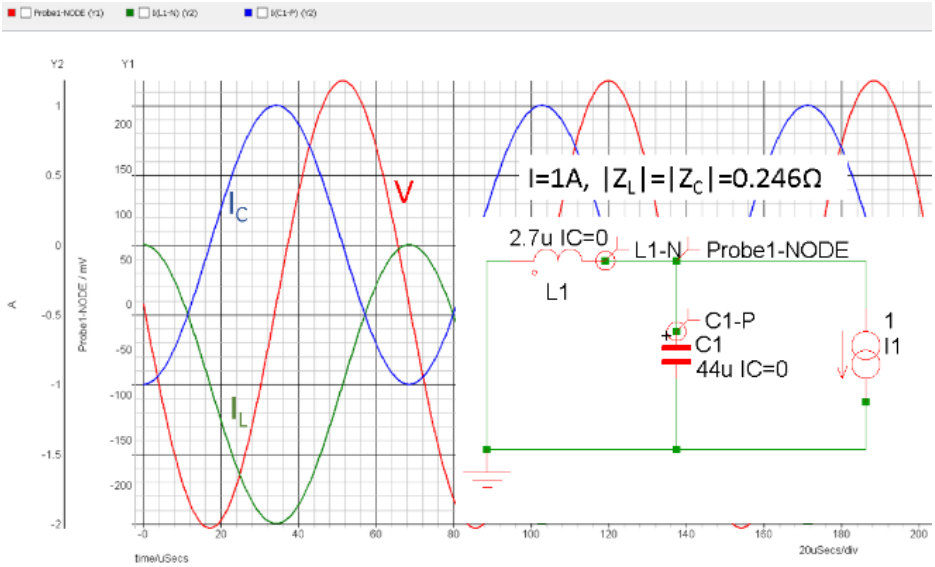

Fig. 4. LC resonant response to current step.

In this case, the circuit tends to develop an oscillation of amplitude:

$$v = ZI \sin 2\pi\, x\, f_{RES}\, x\, t$$

where t is time, I is the 1-A load step and:

$$Z = \sqrt{L/C} = \sqrt{\frac{2.7}{44.6}} = 0.246\Omega$$

$$ZI = 0.246\, x\, 1 = 246mV$$

$$f_{RES} = \frac{1}{2\pi\sqrt{LC}} = \frac{1000}{2\pi\sqrt{2.7x44.6}}k = 14.5kHz$$

Naturally, this oscillation unfolds only until the loop responds after a delay time τ given by equation (3). Accordingly, the sinusoid will stop at:

$$v(\tau) = V_{droop} = ZI \sin(2\pi\, x\, f_{RES} \frac{1}{2\pi f_{BW}}) = ZI \sin\left(\frac{f_{RES}}{f_{BW}}\right)$$
$$= 246\ mVx \sin(\frac{14.5}{18.8}) = 246\ mVx\ 0.697 = 171\ mV$$

With the inductor back in the picture, the estimated droop value is 171 mV, much closer to the simulated 157 mV. With a 171-mV droop estimate, the error is 238.3 mV, still within the 240-mV budget.

Reconciliation

Short of simulating it or building the circuit and exercising it with a current load step generator, we can find the first-order estimate of the droop amplitude with two formulas, one for the linearized droop model:

$$V_{droop}C = \frac{I}{2\pi\, x f_{BW}\, x\, C}$$

and another with the LC resonant model:

$$V_{droop}LC = ZI \sin\left(\frac{f_{RES}}{f_{BW}}\right)$$

Which one should be used in lieu of a full-fledged simulation or breadboard construction? As often is the case, it depends. If your f_{RES} << f_{BW}, then by using the approximation sin x ≈ x in $V_{droopLC}$, we have:

$$V_{droop}LC \approx ZI \frac{f_{RES}}{f_{BW}}$$

And by substituting Z and f_{RES} with their expressions, we have:

$$V_{droop}LC \approx I\sqrt{L/C}\, \frac{1}{2\pi\sqrt{LC}} \frac{1}{f_{BW}} = \frac{I}{2\pi\, x f_{BW}\, x\, C}$$

So, for f_{RES} << f_{BW}, either expression works. Fig. 5 shows the difference between the two approaches and the linearization error.

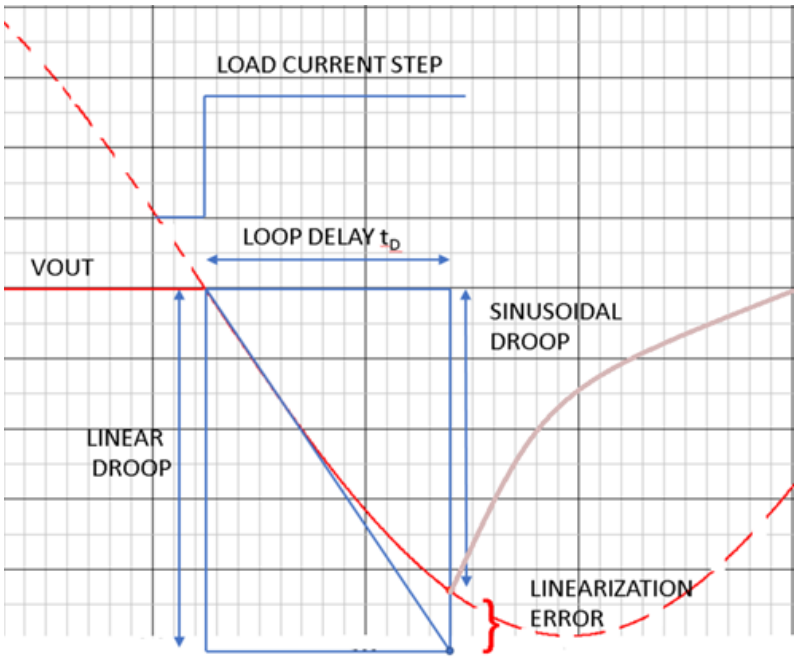

Fig. 5. LC resonant vs. linear models.

In our case, the two frequencies are pretty close, so the CdV/dt-based approximation fails and we really need to use the LC resonant model.

The Simulation Advantage

Maxim's EE-Sim design tool uses SIMPLIS, the simulation engine from Simplis Technologies, to simulate the performance of a circuit. SIMPLIS was developed and optimized for simulating switching circuits like dc-dc converters. Unlike our simple back-of-the-envelope calculations, a simulation takes into account all the factors of the circuit, or at least those that are in the component models.

Naturally, our hand calculations are crude estimates with simplified equations that do not include all the effects of the circuit and neglect the component parasitics (e.g., ESR, etc.). Hence, the simulation provides the most accurate results.

Conclusion

We performed an output voltage error budget analysis for the MAX17242 (see the reference) buck converter design. We simulated the contributions of the ripple and load step voltage droop amplitude to the error using the EE-Sim online dc-dc tool. Our initial hand calculations of the voltage droop appeared to be pessimistic compared to the simulations.

But then we reviewed our assumptions and developed a more accurate back-of-the-envelope approach to the step-response calculation. The result from this approach came much closer to the simulated result. This, and more importantly the simulation result, eased our initial concerns about the ability to meet the error budget.

Reference

MAX17242 synchronous buck converter datasheet.

For Further Reading

1. EE-Sim DC-DC Converter Design Tool

2. MAX17242 3.5V–36V, 2A, Synchronous Buck Converter with 15µA Quiescent Current and Reduced EMI

3. Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7µF Capacitor Becomes a 0.33µF Capacitor, Design Solutions No. 60, Rev 0; November 2017.

About The Authors

Brooks Leman, senior principal member of technical staff at Maxim Integrated, has been developing and applying switching power conversion techniques in Silicon Valley for over 36 years. He holds several patents and has published dozens of technical conference papers, magazine articles, and application notes. He holds BSEE and MSEE degrees from Santa Clara University where he also teaches a power conversion graduate course.

Mark Fortunato is senior principal member of technical staff at Maxim Integrated and has managed the EE-Sim team for the past three years. He has 37 years of experience in analog electronics from dc to 200 GHz including 21 years in the semiconductor industry in roles including field applications, product definition, design management, FAE management and strategic marketing before taking his current role. He has a BS in electrical engineering from the California Institute of Technology and can often be found on hiking trails.

Nazzareno (Reno) Rossetti, Ph.D. EE at Maxim Integrated, is a seasoned analog and power management professional, a published author who holds several patents in the field. He holds a doctorate in electrical engineering from Politecnico di Torino, Italy.

For more information on buck converter design, see the How2Power Design Guide, locate the Popular Topics category and select "Buck Converters".