PCB Board Layout Is Critical When The Power Supply And MCU Live On The Same Board

by Kevin Parmenter, Chair, and James Spangler, Co-chair, PSMA Safety and Compliance Committee

In many simple industrial and consumer products there is simple printed circuit board (PCB) that contains both a microcontroller (MCU) and a simple off-line power supply. In such cases, there are typically two sources of EMI: line conducted EMI from the power supply and radiated EMI from the MCU. When there is a failure in EMC testing, the customer's first reaction is often to blame the power supply. But very likely, it is not the power supply causing the failure, but rather a poor PCB layout that caused the data lines to radiate. This is much like the situation we discussed in last month's column (see "A Power Supply Can't Fix All EMC Woes…"), but here we're looking at a different design scenario (offline power supply + MCU on the same board) and how the EMC problem can be avoided through proper PCB layout.

After reviewing some of the basic requirements of PCB design, we go step-by-step through the details of layout of a PCB for an MCU. We then discuss the special case of what to do when there is no ground plane, as may occur with single-sided or single-layer boards. Next we look at some power-supply related layout problems that can occur and how these can be addressed by proper choice of resistors and decoupling caps. Scans of radiated EMI for the example MCU application demonstrate how the errors in pc board layout led to compliance failures.

Finally, in the last sections of the article, we look at how neglecting manufacturing requirements early in the example pc board design led to problems with the layout that required a redesign. We conclude with lessons learned in laying out the example MCU application.

Every PCB Is Custom

Besides the package (case), one of the largest items for a product is the PCB. In general, the PCB is a custom part number that cannot be purchased as an off-the-shelf item from a distributor. It must be designed at the beginning of a project.

The PCB connects electronic parts of the product to form a system. The layout of the PCB is critical for radiated emissions, and susceptibility to external stray fields that can cause functional failures. The layout is also critical for trace spacing in order meet the shock and fire safety standards. The subject of PCB layout has been discussed in many IEEE-EMC workshops, IEEE APEC EMC Professional Education Seminars,[1, 2, 3, 4, 5] other seminars and workshops easily found through IEEE internet searches, and webinars offered by companies. This topic has also been addressed extensively in books by Henry Ott[6, 7] and Ralph Morrison.[8, 9]

The PCB is a method of connecting various ICs and modules together. The connections are called traces. Connections that contain high-speed clock signals, data signals, and low-frequency display driver signals can become sources of radiated emissions. Signals without a proper return trace become the source of unwanted radiation. Unprotected traces are defined as a wire or PCB trace between ICs on the board, or a connector to the MCU without a proper return path for the current to return to its source.

It has been demonstrated by many presenters at EMC conferences that the return path is not the shortest length of line. The return current follows under the signal trace or next to the signal trace. The space is the smallest distance separating signal and the return path. This will be explained later in the article. If the return is not next to or beneath the signal, this large loop can become a radiator or loop antenna. This concept is explained in more detail in the books by Morrison[8, 9] and Ott.[6, 7]

Laying out a PCB to keep radiation low and below the FCC limits is an engineering art. It often takes three revisions for a PCB to be ready for pre-compliance testing before production. To keep the layout revisions to a minimum and meet production time schedules, the use of PCB tools from a number of commercial vendors is recommended: Altium, Mentor Graphics (PADs), Eagle Pro, etc.

It is also recommended that the project engineer/manager spend time with the PCB layout engineer or technician to identify critical placement of parts and traces. There is often a tradeoff between which traces take priority and how to route the traces to keep EMI within the FCC or International Electrotechnical Commission (IEC) limits.

Besides EMI limits, there are shock hazards and arc spacing limits from Underwriter's Laboratory (UL) and the IEC. They have limits for spacing between high-voltage traces. These spacing limits for the various voltages are defined in the various UL and IEC rules and regulations. There are different distance limits for surfaces over the PCB, through the PCB, traces on the board to the case, and clearance to earth or protected ground.

MCU PCB Layout

First let's start the project with the MCU. Dan Beeker, an automotive field applications engineer at NXP,[4] recommends placing the power supply lines with decoupling capacitors as close to the MCU as possible. He recommends placing the power supply traces first before any other signal traces are placed, including decoupling capacitors. The power supply traces should be wider than the signal traces to handle the MCU current.

Next, place any display driver traces with returns lines. The return lines should not be broken, so that the current flows beneath or below the signal lines. These traces should be narrow in width since they carry little current. Follow this, by placing data communications signal lines such as Universal Serial Bus (USB), Controller Area Network (CAN), Serial Peripheral Interface (SPI) and single-wire CAN with a direct connection between edge connector and the MCU. These lines must have a return path beneath or next to the signal line.

Texas Instruments[10] and Intel[11] have application notes and recommendations on PCB trace routing to reduce EMI. Please follow the recommendations from semiconductor IC companies that have CAN driver ICs for layout guidelines specific to these devices.

Fig. 1 is an example of a mixed-signal trace routing that Dan Beeker and others have recommended. The analog signal shown in Fig. 1 has three lines back to an MCU with A-D capabilities. The ground trace is between the two analog signal traces. These could be differential analog lines or two separate analog signals. This arrangement is referred to as a routed triplet. The example in Fig. 1 is a two-sided board: black is one side while red is the other side. The connector pins are labeled: P for power, G for ground, A for analog, and D for digital.

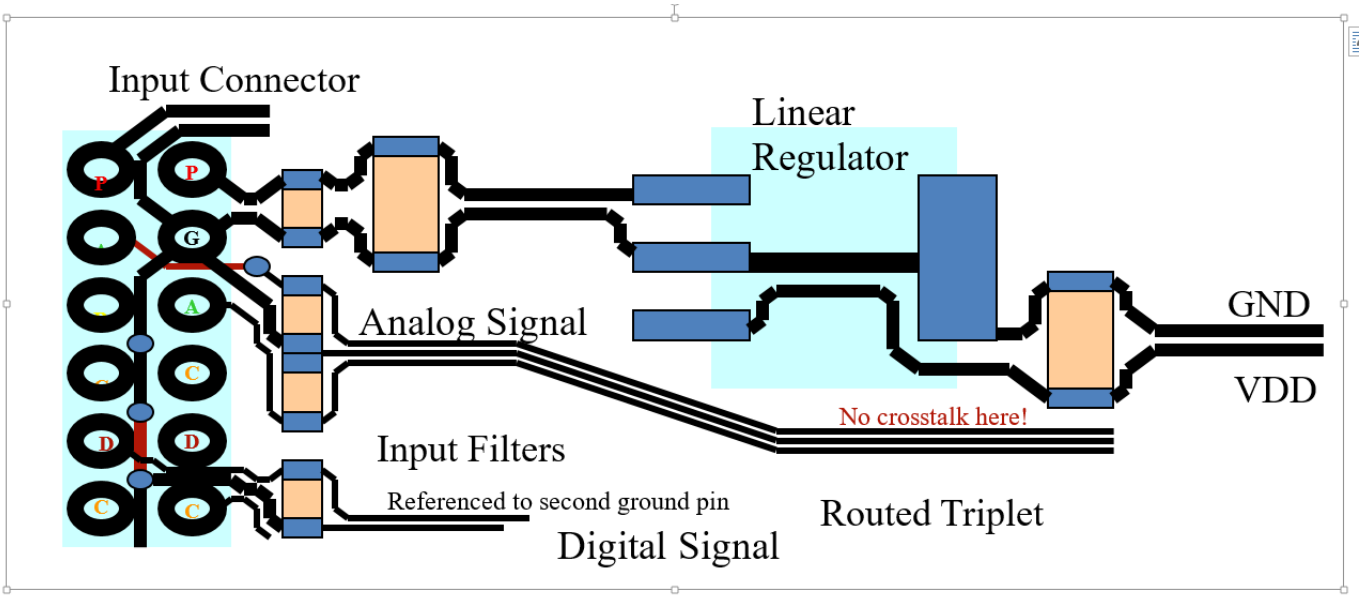

Fig. 1. Mixed-signal layout for both digital and analog signals. (Diagram courtesy of Dan Beeker.)

The MCU with various routed triplets is shown in Fig. 2. There is an internal power supply on the MCU with an external bypass capacitor. The main power supply feed has two capacitors with the smaller part next to the MCU. Note that the ground trace for the routed triplet changes from the black side to the red side. This was needed to maintain the voltage spacing between the IC pins and the ground. These are small signal traces meaning lower voltages and lower currents.

The orange pad is the large ground pad for the MCU, which is on the same side as the black traces. This large area can be used as a heat sink for the MCU. The dots in the orange area feed-thru from the top side to the bottom side of the PCB.

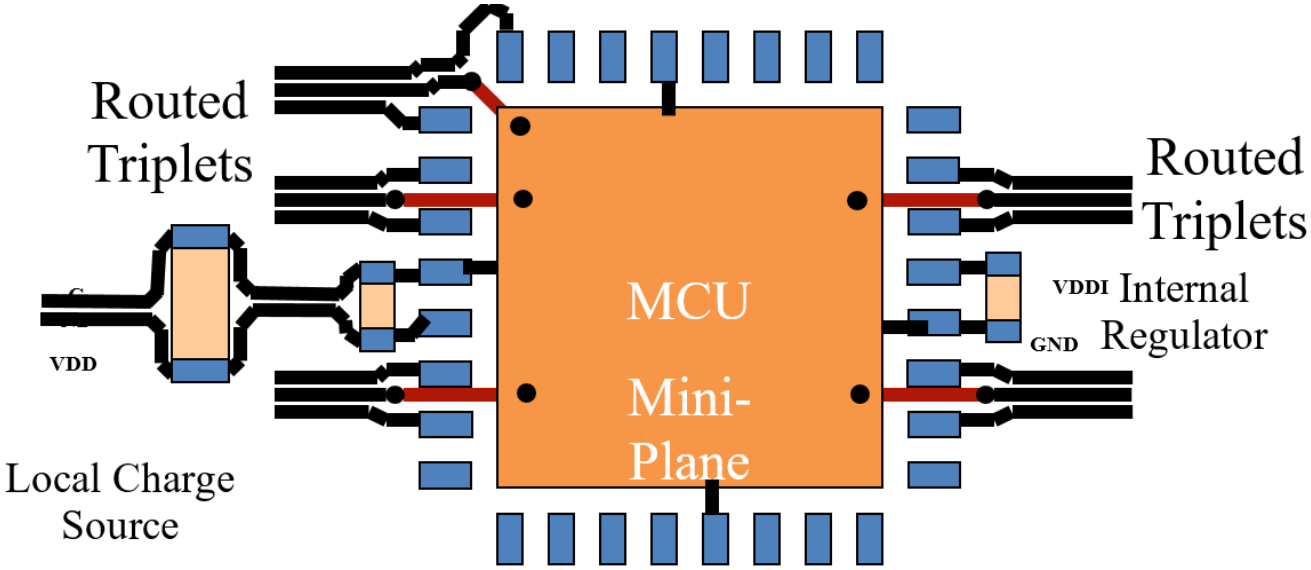

Fig. 2. An application example of routed triplets with an MCU. (Diagram courtesy of Dan Beeker.)

Side-by-Side Traces Instead Of A Ground Plane

In a PCB layout design there are often signal traces next to each other. At times these signals can cross couple and cause unwanted results. This can occur with analog signals of different amplitudes. Fig. 3 shows the coupling when there is no ground return path. This is a single-sided or single-layer PCB concept. Fig. 2 above is a double-sided PCB.

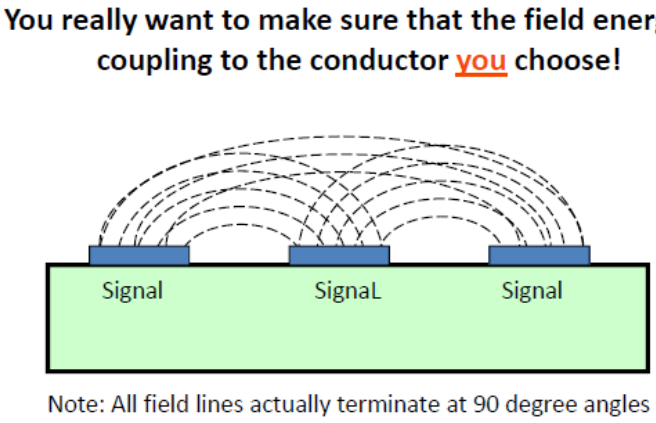

Fig. 3. Signal traces without a ground. (Diagram courtesy of Dan Beeker.)

To solve this cross coupling it's recommended that a ground trace be placed between the traces as shown in Fig. 4. Notice the cross coupling between traces. Since the traces carry small currents and the voltage is low, the trace width can be small. The small trace width and spacing is defined by the PCB manufacturing process and the PCB assembly. The concept of the triplet for analog signals can take more trace area but it eliminates the need for a ground plane in this area where other traces can be routed.

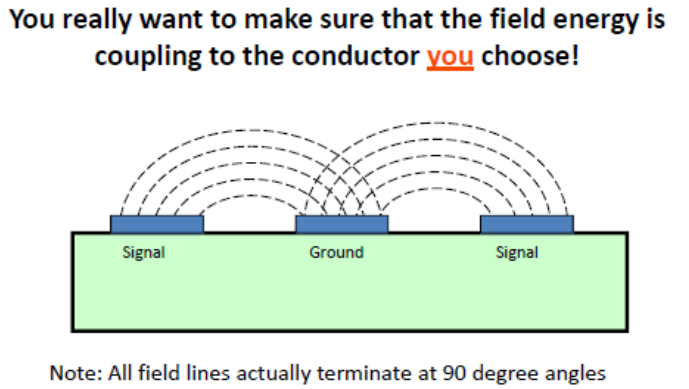

Fig. 4. Signal traces with a ground between the signal lines. (Diagram courtesy of Dan Beeker.)

An Example Of Power Supply Layout Issues

An example solving radiated emissions for a pc board layout with an MCU is given below.

1. A consumer product was upgraded with a new +5-Vdc MCU due to added features and end of life for the old MCU. The new MCU had a higher operating frequency with an internal clock generator.
2. Instructions given to a junior PCB layout technician were incomplete and somewhat lacking.
3. The designer created schematic drawings and did not follow proper IC power supply trace guidelines.
4. The MCU power supply was not properly decoupled and resulted in radiation due to the clock signals radiating through the power supply lines and the display driver traces.

A partial schematic showing the MCU power supply section related to the above issues is presented in Fig. 5; the unit failed Class B FCC limits. The display driver traces are not shown in Fig. 5. In a proper design, each VCC (+5-Vdc power supply input) pin should have two ceramic decoupling capacitors to ground as shown in Fig. 6. There was no issue with the analog VCC input (AVCC). Fig. 6 shows the power supply circuit with a separate decoupling network for each of the VCC pins 5, 17, and 38.

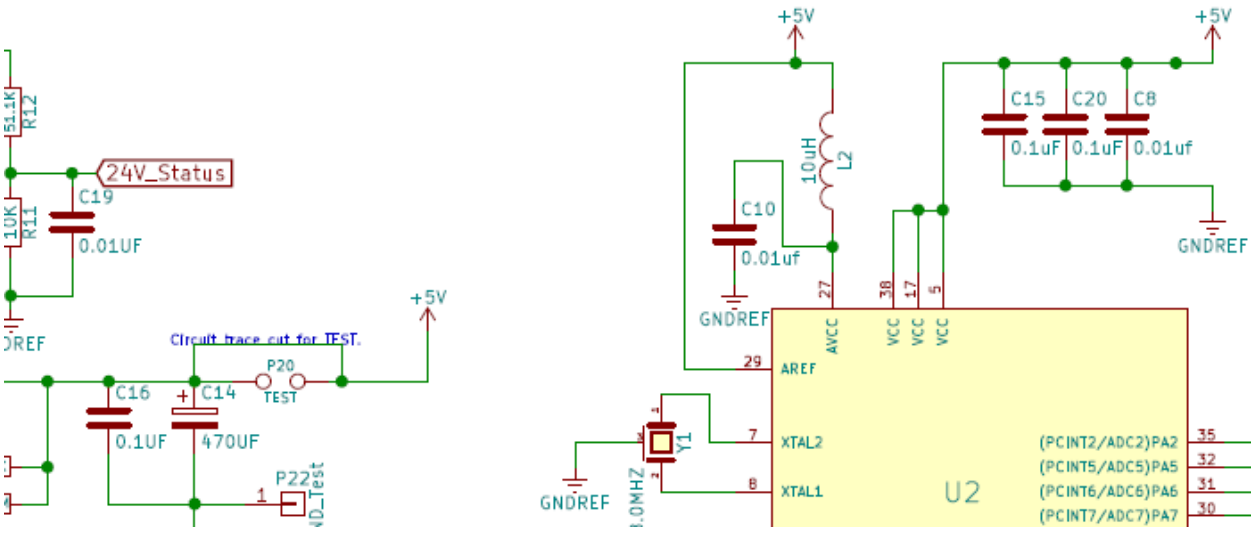

Fig. 5. The unit failed radiated emissions due to the power supply routing.

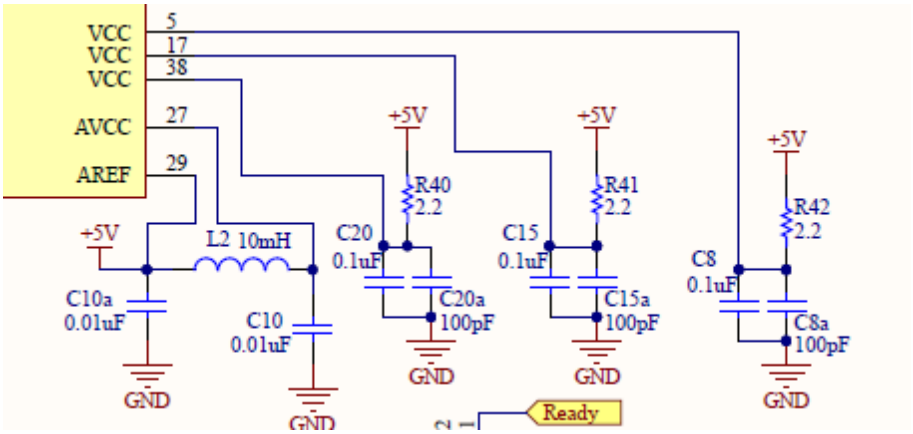

Fig. 6. VCC supply network with a separate decoupling circuit for each power supply input.

In the final design, the series power supply resistors were reduced in value from 2.2 Ω to 1.0 Ω. The current draw for the MCU was less than 100 mAdc from a 5.0-Vdc supply. The voltage drop across the 2.2-Ω resistor was 0.22 Vdc. The impedance of the 0.1-μF ceramic capacitor at 10 MHz was 0.159 Ω and 0.0159 Ω at 100 MHz.

The decoupling capacitors have lower impedance than the series resistor. This keeps the undesired clock noise spikes from radiating. The purpose of the network is to keep the high-frequency noise generated by the MCU internal clock generator filtered by the 0.1-μF and the 100-pF capacitor, and not be conducted throughout the pc board on the +5-Vdc power supply bus. Dan Beeker[4] does not recommend placing a resistor in series with the +5-Vdc bus as shown in Fig. 6, but to use ceramic capacitors close to the MCU.

Radiated EMI Scans

The EMI failed signal scans are shown in Figs. 7, 8, and 9. Some of the issues were with the power supply's lack of decoupling and others were with the display driver signals having an improper ground return. These are just examples of problems that can be eliminated with proper power supply decoupling and a good signal trace layout with a proper return.

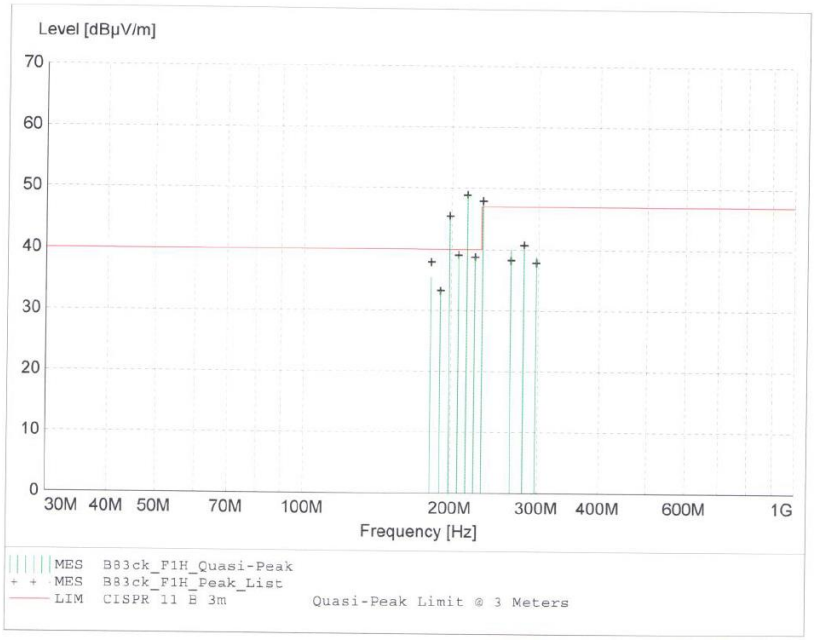

Fig. 7. EMI radiation produced by improper power supply decoupling network and display driver.

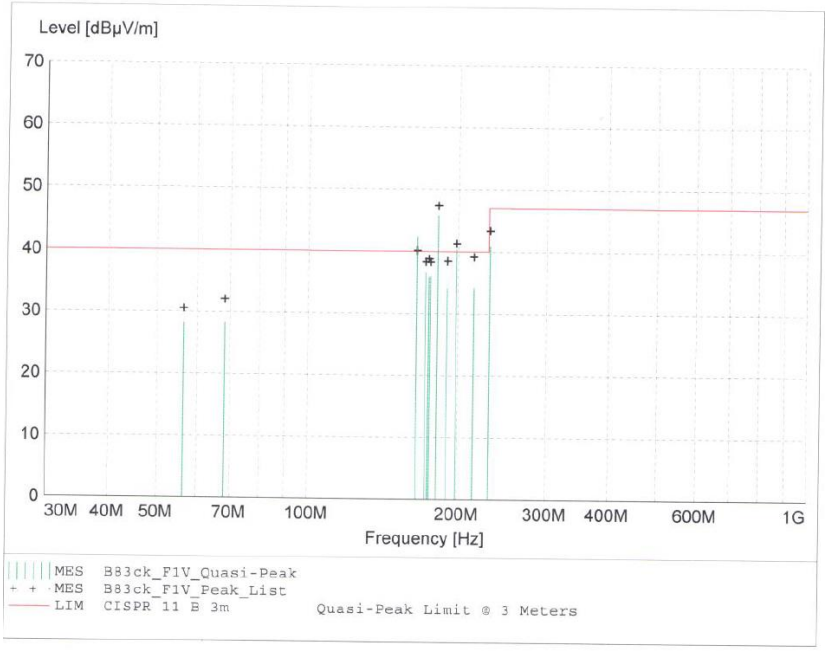

Fig. 8. Improper decoupling network on power supply and display drivers.

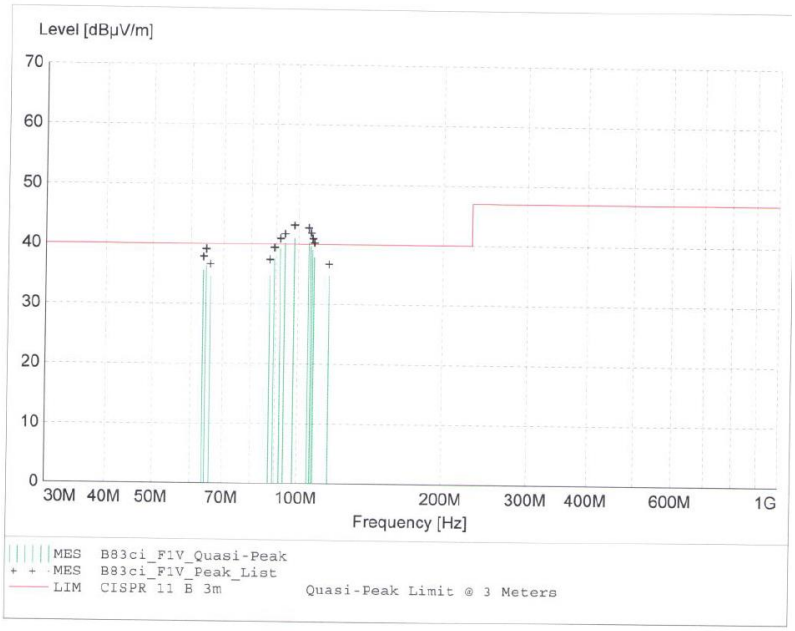

Fig. 9. EMI Radiation on a MCU with display energized.

Manufacturing Issues From Malcolm Baldrige Class

During the 1990s after Motorola won the Malcolm Baldrige Award, Motorola University offered many classes on six sigma, design for assembly, and design for manufacturing. One of the favorite courses was the "tinker-toy" class for building a tower.

The designers had to build a prototype tower from the parts given. The parts used for the prototype were not the same parts used for production, or approved for manufacturing. The purpose was to teach the students that they needed to ask questions about manufacturing, approved parts vendors, timing, purchasing, etc. Needless

to say the novice students failed to consider many of these issues and points were taken away from their design. A great lesson learned, ask questions before jumping to the final design.

Going back to the design shown in Fig. 4, at the start of the project, questions were asked about the size of the SMT parts that manufacturing could place. The customer coordinator indicated manufacturing could handle the 0402 size capacitors and resistors but not the smaller 0201 size parts. But then later at the first PCB layout design review with manufacturing engineers, the concern was raised that the soldering process could not handle surface mount technology (SMT) parts smaller than 0603.

This manufacturing limit was not discussed properly at the beginning of the program. The PCB had been laid out to meet EMC by having the decoupling capacitors next to the processor. The layout used 0402 capacitors and suggested 0201 size capacitors to make sure the parts were next the MCU. The small size 0201 SMT capacitors were shown earlier in this article. See Figs 1 and 2. Such parts are available from a number of distributors.

When the design was presented to the contract manufacturer, assembly and quality issues were raised. The manufacturing equipment could only reliably handle 0603 and 0805 size SMT parts in the placement and soldering process. This required a complete redesign and layout.

After the first PCB review, both the display lines and power supply lines had to be changed. The design engineer was contacted and the redesign process continued a day later by conference calls. It was determined that the data lines to the display did not have proper returns lines to the MCU ground plane. There were 11 display driver interface lines that came from three sides of the MCU package. A special ground layout was required and the trace width was widened. The MCU was re-oriented to allow for ground return lines.

There is additional information for data lines used for communications and PCB traces. TI and Intel[10, 11] publish application notes on USB and other data lines. Many of the semiconductor IC companies supporting the auto industry publish applications and guidelines for Controller Area Network (CAN) pc board layout. Besides CAN, there is a single-wire CAN and LIN bus which is used in the automotive body electronic modules. It is recommended that the design engineer, and if necessary the PCB layout technician, contact the semiconductor manufacturer for additional layout information.

Lessons Learned

The design engineer and PCB layout engineer or technician should have all of the information concerning the project prior to start of the process. The following are some questions that may need to be addressed.

1. What is the MCU or processor to be used?
2. Are there any special layout requirements?
3. What is the manufacturing process?
4. What are the sizes of the parts used in the project?
    a. SMT parts
    b. Thru hole parts
    c. Displays
    d. Connectors
    e. External bus connections
    f. Spacing between traces
5. Time-table and critical path items with other engineers
6. Special purchasing and vendor requirements
7. When and where and how often to meet, engineer and layout tech?
8. When and where are the design reviews?
9. Who is the PCB manufacturer and what is needed on the board?
    a. Solder Mask
    b. Roll-tin plating
    c. Legend
    d. Is conformal coating needed
    e. Hole size and feed-thru sizes
    f. Ground planes, double sided, buried layers (4 layer)
    g. Copper thickness (1 oz, 2 oz. etc.)

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About The Authors

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