The Engineer's Guide To EMI In DC-DC Converters (Part 5): Mitigation Techniques Using Integrated FET Designs

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Parts 1 through 4 of this article series offer a detailed perspective on conducted and radiated emissions from switching power regulators, including a description of the mechanisms for noise generation, measurement requirements, frequency ranges, applicable test limits, propagation modes and parasitic effects.[1,2,3,4] Based on that theoretical foundation, here in part 5 I will present practical circuit techniques to mitigate electromagnetic interference (EMI).

In general, the circuit schematic and printed circuit board (PCB) design are pivotal to achieving excellent EMI performance. Part 3 underscored the imperative to minimize "power loop" parasitic inductance through careful component selection and PCB layout.[3] The power converter integrated circuit (IC) has an outsized impact here, both in terms of its package technology and the EMI-specific features it offers. As outlined in part 2, differential-mode (DM) filtering is mandatory to sufficiently reduce the input ripple current amplitude to the required level for EMI regulatory compliance.[2] Meanwhile, common-mode (CM) filtering is generally required to curtail emissions above approximately 10 MHz. Shielding also offers excellent results at high frequencies.

This article delves into these aspects, offering practical examples and guidelines to mitigate EMI, specifically for converter solutions with integrated power MOSFETs and controller. In general, a converter should pass conducted EMI by a reasonable margin to have any chance of meeting radiated limits. Fortunately, most steps taken to abate conducted emissions are correspondingly effective in mitigating radiated EMI.[5]

Understanding The EMI Challenge

The major source of EMI in dc-dc converters is the fast switching of voltages and currents. The EMI related to a converter's discontinuous input or output current is relatively easy to deal with, but a greater concern relates to the harmonic content of the switching waveforms, in terms of ringing as well as the rise and fall times (dv/dt and di/dt).[3]

$$f_{Ring1} = \frac{1}{2\pi\sqrt{L_{LOOP}C_{OSS2}}} = 160\text{MHz}$$

$$\alpha = -\frac{R_{LOOP}}{2L_{LOOP}}$$

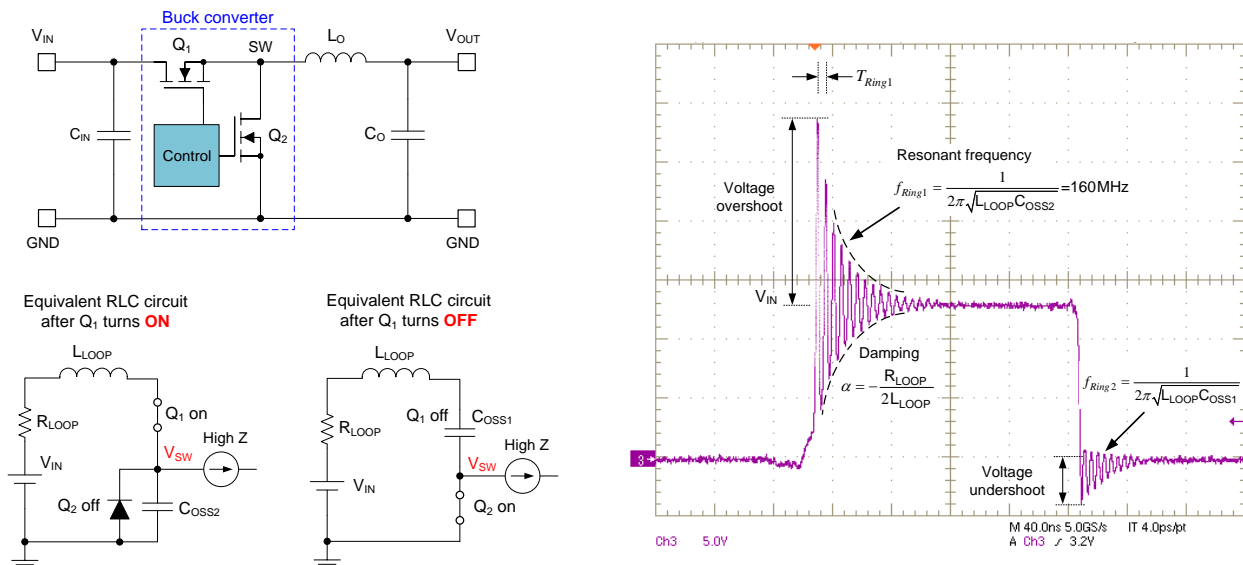$$f_{Ring2} = \frac{1}{2\pi\sqrt{L_{LOOP}C_{OSS1}}}$$

Fig. 1. Switch-node voltage waveform and equivalent circuits during MOSFET turn-on and turn-off switching transitions for a synchronous buck converter.

Fig. 1 shows the switch-(SW) voltage waveform of a noisy synchronous buck converter. The ringing frequency ranges from 50 MHz to 200 MHz depending on parasitics. Such high-frequency content can propagate by near-

field coupling[4] to the input supply lines, to nearby components or to the output bus (for example, a USB cable). Body-diode reverse recovery presents a similar issue, exacerbating the ringing voltage as the recovery current flows in the parasitic loop inductance.

The schematic in Fig. 2 identifies the two critical loops for a buck converter circuit. Minimizing the power-loop area is essential because of its proportionality to parasitic inductance and related H-field propagation. The main design goal is to push the resonant frequency of the parasitic LC tank as high as possible by curtailing the parasitic inductance. This decreases the total stored reactive energy and lowers the switch-voltage peak overshoot.
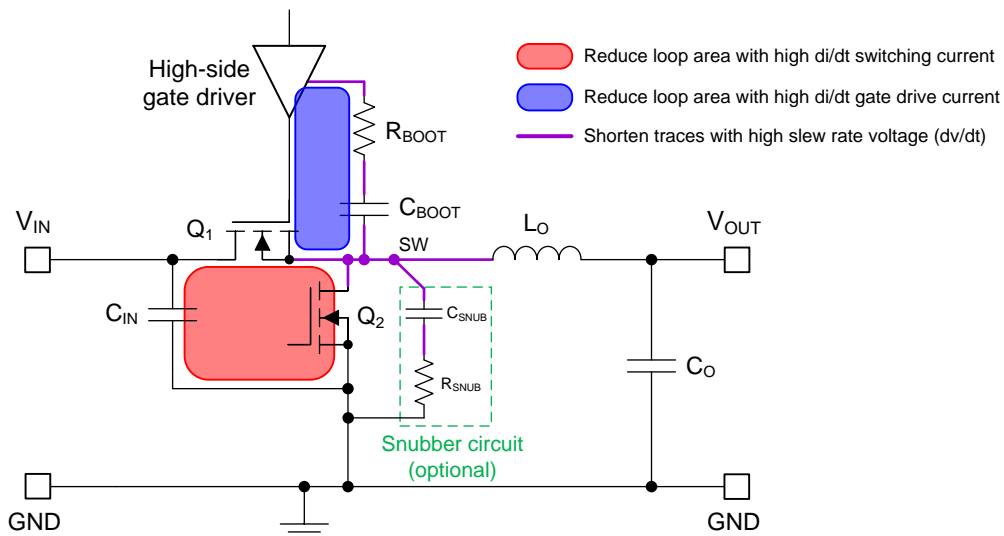

Fig. 2. Simplified synchronous buck converter schematic with highlighting of the loops and traces critical to generation of EMI.

In the boot capacitor loop shown in Fig. 2, an optional series boot resistor, designated R_{BOOT}, controls the turn-on speed of the high-side MOSFET. The boot resistor changes the drive-current transient rate and thus reduces the switch voltage and current slew rates during MOSFET turn-on. Another option is a snubber circuit from SW to GND. Similarly, this snubber should also occupy a minimal loop area based on its transient current spike at each switching transition.

Of course, snubbers and gate resistors increase switching power loss, leading to a tradeoff between efficiency and EMI. Other techniques are required to solve the EMI challenge if efficiency and thermal performance are also important.

Converter PCB Layout

Items 1 through 5 summarize the essential guidelines for PCB layout and component placement for a reduced dc-dc converter EMI signature. I'll provide a PCB layout case study for an EMI-optimized buck converter later in this article.

1. Routing and component placement.
    - Route all power-stage components on the top side of the PCB. Avoid locating the inductor on the bottom side, where it can radiate to the reference plane of the EMI test setup.
    - Place VCC, VDD and/or BIAS bypass capacitors close to their respective pins. Ensure that the AGND pin "sees" the C_{VCC} and C_{BIAS} capacitors first before connecting it to GND.
    - Connect the bootstrap capacitor close to the BOOT and SW pins. Shield the C_{BOOT} capacitor and switch node with adjacent ground copper to reduce CM noise.

2. Ground plane design.
   - Position a layer 2 ground plane in the PCB layer stackup as close as possible to the top layer. This provides H-field cancellation, parasitic inductance reduction and noise shielding.
   - Use low z-axis spacing between the top layer and second layer for optimal image plane effectiveness. Define a 6-mil intralayer spacing in the PCB stackup specification.

3. Input and output capacitors.
   - Place C_{IN} to minimize the loop area formed by C_{IN} connections to the VIN and PGND pins.
   - Ground return paths for both C_{IN} and C_{OUT} should consist of localized top-side planes. Connect dc current routes using multiple external or internal ground planes.
   - Use 0402 or 0603 case size ceramic input capacitors near the VIN and PGND pins to minimize parasitic loop inductance.

4. Inductor and switch-node layout.
   - Locate the inductor close to the SW pin of the IC. Minimize the switch-node copper surface area to prevent excessive capacitive coupling.
   - Confine switch-node noise using adjacent ground guarding and via shielding.
   - Check the inductor dot position to ensure that the end of the inductor winding tied to SW is on the bottom and inside of the winding geometry and shielded by the outer turns of the winding connected to VOUT.
   - Use an e-field-shielded inductor if possible. Connect the shield terminals to the PCB ground plane.
   - Select an inductor with terminations underneath the package. Avoid large sidewall terminations that can act as radiating antenna.

5. EMI management.
   - Route the EMI filter components away from the switch node. Place the EMI filter on the opposite side of the board from the converter if it cannot be sufficiently separated from the power stage.
   - Place cutouts on all layers below the EMI filter to prevent parasitic capacitive paths impacting the filter attenuation characteristic.
   - Place a resistor (preferably less than 10 Ω) in series with C_{BOOT}, if needed, to slow down a buck converter's high-side MOSFET turn-on, reducing the switch-node voltage slew rate, overshoot and ringing.
   - If a switch-node RC snubber is required, connect the smallest footprint component to SW (usually the capacitor).
   - Use a four-layer PCB with inner ground planes to achieve much improved performance relative to a two-layer design. Avoid disruption of the high-frequency current paths near the IC.

EMI Input Filter

Fig. 3 shows a typical multistage EMI input filter. Low- and high-frequency sections provide DM noise attenuation, and an optional π-stage with a CM choke delivers CM attenuation. An electrolytic capacitor, designated C_{BULK}, has an inherent equivalent series resistance (ESR) that sets the required damping to reduce the effective Q-factor at the converter input and maintain input filter stability.[6]

The self-resonant frequency (SRF) of the DM inductor limits the achievable high-frequency DM attenuation of the first filter stage. A second filter stage is often essential to provide supplemental DM attenuation at a high frequency using a ferrite bead, with impedance typically rated at 100 MHz. Ceramic capacitors, designated C_{F1} and C_{F2}, shunt noise to ground.

In general, the DM filter inductance is sized to attenuate the fundamental- and low-frequency harmonics. Use the minimum inductance possible to meet the low-frequency filtering demands, as a higher inductance with more turns increases the inductor's equivalent parallel capacitance (EPC) and thus the SRF, compromising its performance at high frequencies.
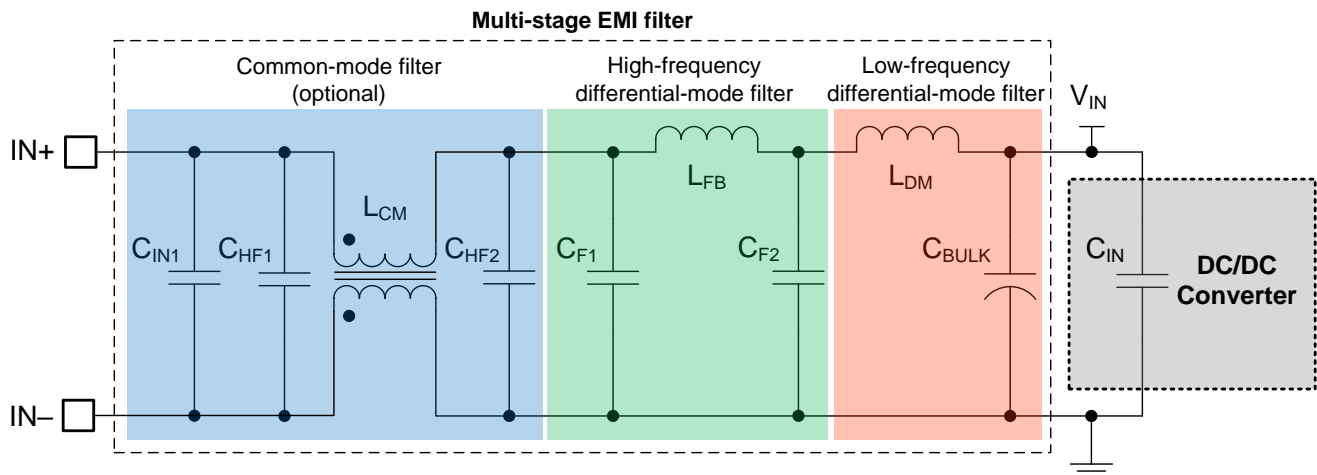
Fig. 3. Three-stage EMI input filter with DM and CM stages.

The CM choke, designated L_{CM}, offers a high impedance to CM currents, and its leakage inductance also provides DM attenuation. Nevertheless, this component is undesirable in certain applications where the ground connection must remain intact, making quieter converter designs that obviate the need for a CM choke more favorable.

To demonstrate the effectiveness of a CM choke, Fig. 4 illustrates the Texas Instruments LM53603, a 36-V, 3-A dc-dc converter solution using a two-layer PCB.[7] The power stage is located on the top layer and the EMI input filter is on the bottom. As the layouts in Fig. 4 show, via stitching the ground plane copper around the filter provides a shielding effect. Also, inserting copper plane cutouts on all layers underneath the filter stage avoids any parasitic capacitance that may form between VIN and GND traces, providing a path for noise currents to bypass the CM choke and compromising the filter's impedance characteristic.

Fig. 5 presents CISPR 25 conducted emissions measurements from 150 kHz to 108 MHz for the converter design in Fig. 4. The results are provided with and without the CM choke. Using a Rohde & Schwarz spectrum analyzer, peak and average detector scans are denoted in yellow and blue, respectively. The limit lines in red are the Class 5 peak and average limits (peak limits are generally 20 dB higher than the average limits).

Power stage and EMI input filter
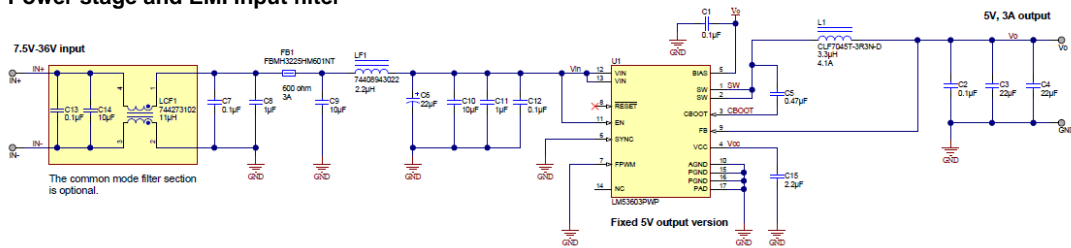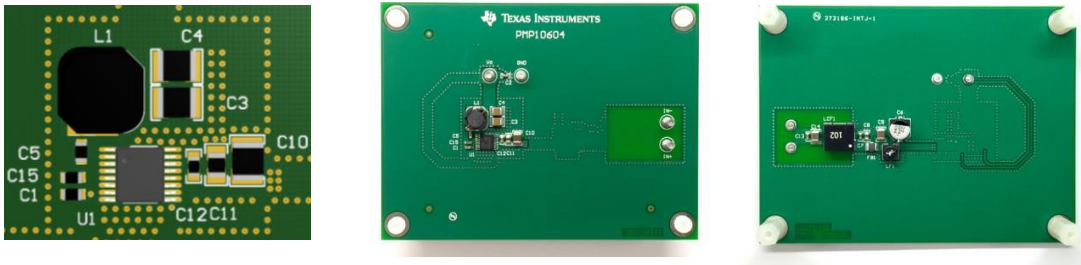

PCB layout implementation

Fig. 4. Dc-dc converter schematic and PCB layout implementation.
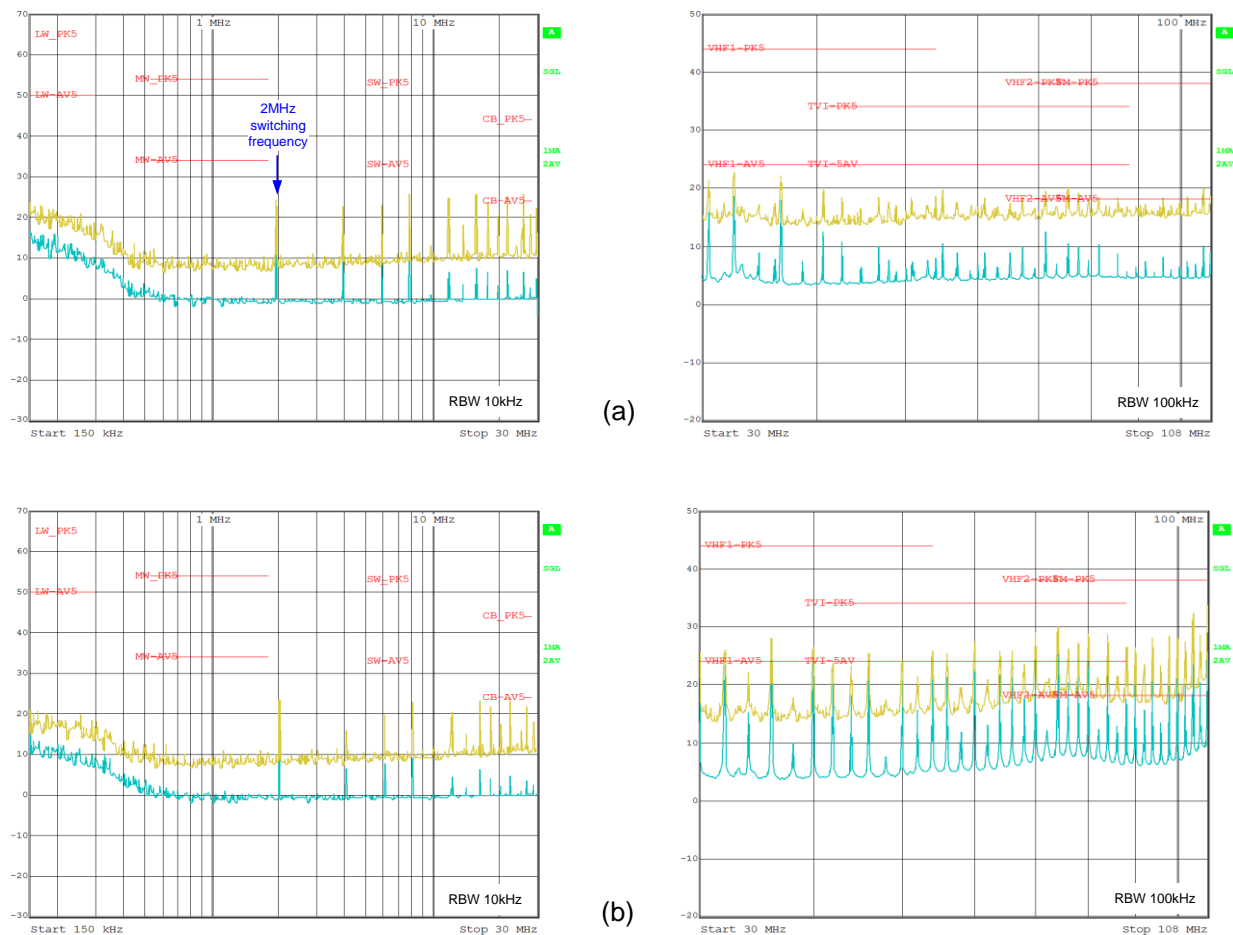

Fig. 5. CISPR 25 conducted EMI measurements with CM choke (a) and without CM choke (b).

Metal Case Shielding

Another very effective way to optimize high-frequency EMI performance is to add a metal case shield[5] to block the radiated electric field. The case is typically made of aluminum and implemented as a frame (open-top) or closed-top design. The shield covers all power-stage components except the EMI filter and is connected to ground on the PCB, essentially forming a Faraday cage with the PCB ground plane.

The result is a dramatic reduction in radiated noise coupling from the switching cell to the EMI filter or onto long input wire connections (which also act as an antenna). Of course, additional component and assembly costs are incurred, and thermal management and testing are more difficult. The case of an aluminum can electrolytic capacitor may also provide e-field shielding and can be tactically positioned on the board for this purpose.

DC-DC Converter Case Study

Fig. 6 is a schematic of a 60-V, 1.5-A monolithically integrated synchronous buck converter circuit[8] with several features in place for optimal EMI performance. The schematic also shows a two-stage EMI input filter stage designed to meet EMI specifications for automotive or noise-sensitive industrial applications. To help translate to an optimized PCB layout, the schematic highlights the high-current traces (VIN, PGND, SW connections), noise-sensitive nets (FB) and high dv/dt circuit nodes (SW, BOOT).
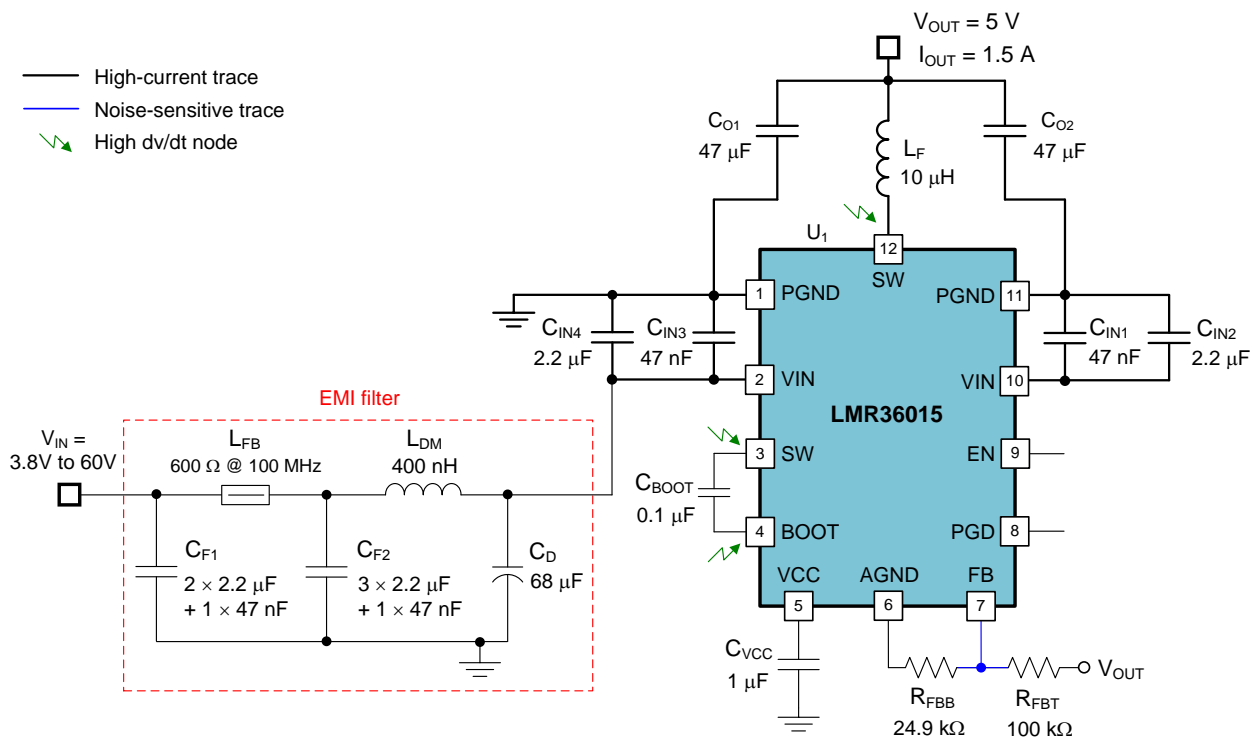

Fig. 6. Dc-dc converter with EMI-optimized package and pinout. Included is a two-stage EMI input filter.

Pinout Design

The converter IC in Fig. 6 has the benefit of a symmetrical and balanced pin arrangement for VIN and PGND. It uses two input loops in parallel that result in effectively half the parasitic loop inductance. These loops are labeled IN1 and IN2 in the PCB layout shown in Fig. 7.

Two capacitors with a small 0402 or 0603 case size, designated as C_{IN1} and C_{IN3} in Fig. 6, are placed as close as possible to the IC to configure the minimum input loop area. The circulating currents create opposing magnetic

moments that result in H-field cancellation and hence lower effective inductance. To further reduce parasitic inductance, a continuous ground plane for return current underneath the IN1 and IN2 loops on layer 2 of the PCB (immediately below the top layer power circuit) supports a field self-cancellation effect.

Using two ceramic output caps, C_{O1} and C_{O2}, one on each side of the inductor, similarly optimizes the output current loops. Having two parallel ground return paths from the output splits the return current in two, helping to mitigate the "ground bounce" effect.
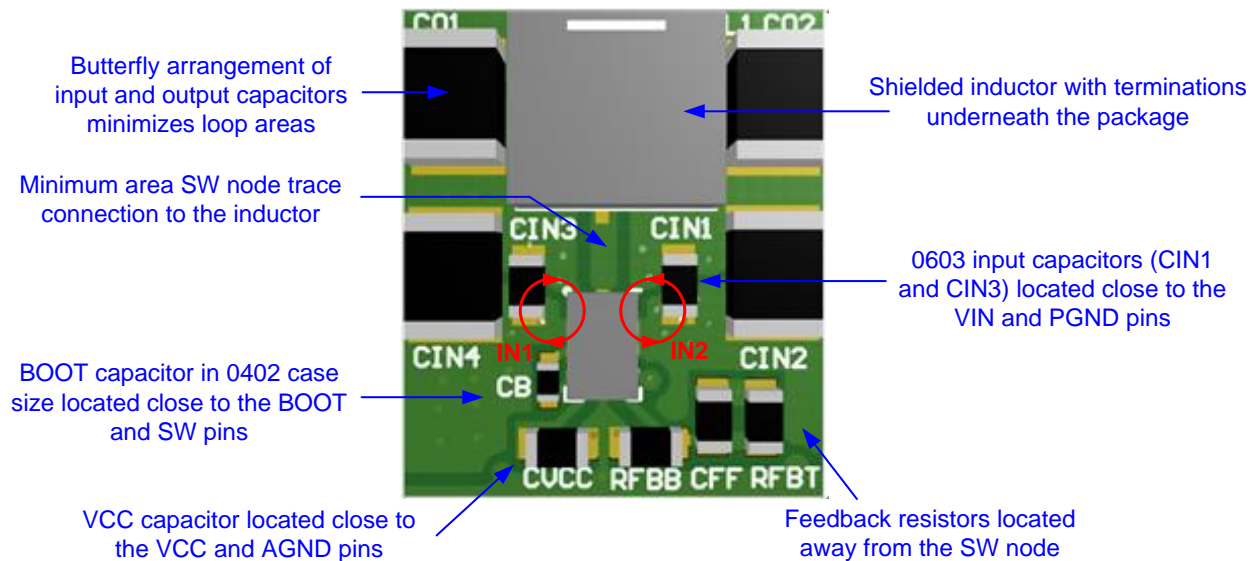

Fig. 7. Power-stage layout routed only on the top layer of the PCB.

The SW pin is located at the center of the IC such that the radiated e-field is shielded by adjacent VIN and PGND pins on both sides of the IC. Ground plane copper shields the polygon pour connecting the IC's SW pin to the inductor terminal. The single-layer SW and BOOT layout implies that vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test.

Package Design

In tandem with optimized pinout, power converter IC package design is a key attribute in the quest to improve EMI signature. For example, the HotRod package technology from TI uses a flipped-chip-on-leadframe (FCOL) technique that eliminates power device wire bonds that typically cause high package parasitic inductance.

Fig. 8 shows that the IC is flipped upside down and copper posts (otherwise known as bumps or pillars) on the IC are soldered directly to the lead frame. This construction method enables high density and a low profile, as each pin is attached directly to the lead frame. Most important from an EMI standpoint, the HotRod package lowers package parasitic inductance versus traditional wire-bond packages.[9]

Traditional wire-bond QFN package
Copper/gold/aluminum bond wires connect IC to pins
⇒ high package parasitic resistance and inductance

HotRod FCOL package
Die is flipped and placed directly onto the leadframe
⇒ **low** package parasitic resistance and **inductance**
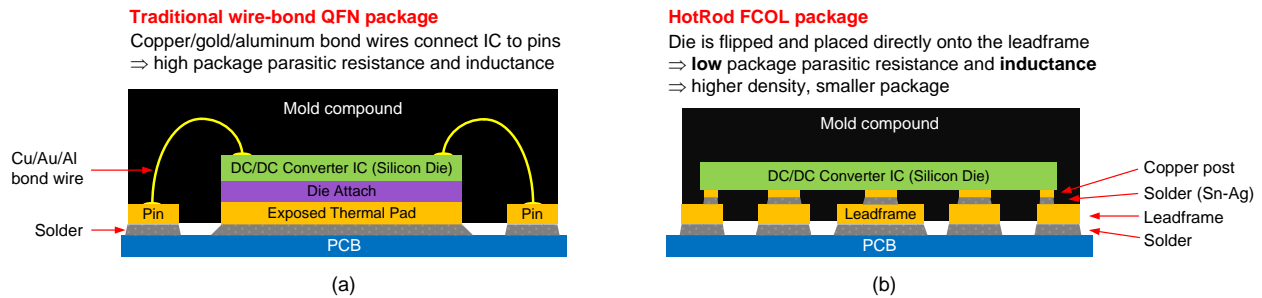⇒ higher density, smaller package

(a)   (b)

Fig. 8. Comparing the package construction of a conventional wire-bond QFN (a) with
that of TI's HotRod FCOL (b).

Not only does the HotRod package result in much lower ringing at the switching commutations (50-MHz to 200-MHz frequency range), it also reduces both conduction and switching losses. Fig. 9 shows the concomitant improvement in switch-node voltage ringing. Fig. 10 shows the conducted emissions measured from 150 kHz to 108 MHz for the converter in Fig. 6. The results are in compliance with CISPR 25 Class 5 requirements.[10]
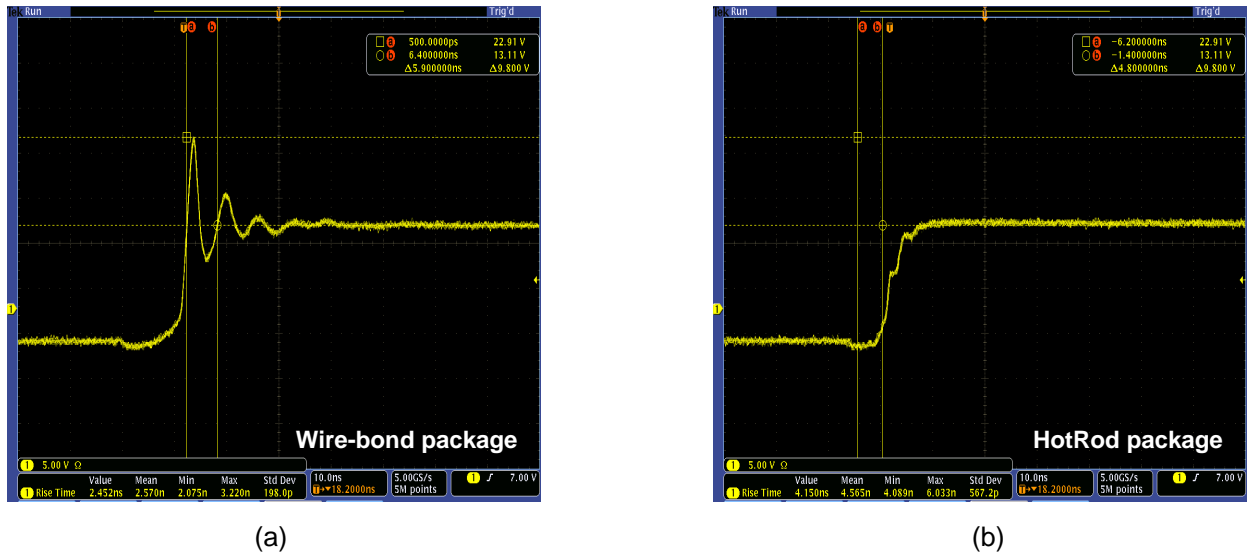

(a)   (b)

Fig. 9. Switch-node voltage waveform with a traditional wire-bond converter (a) versus the same
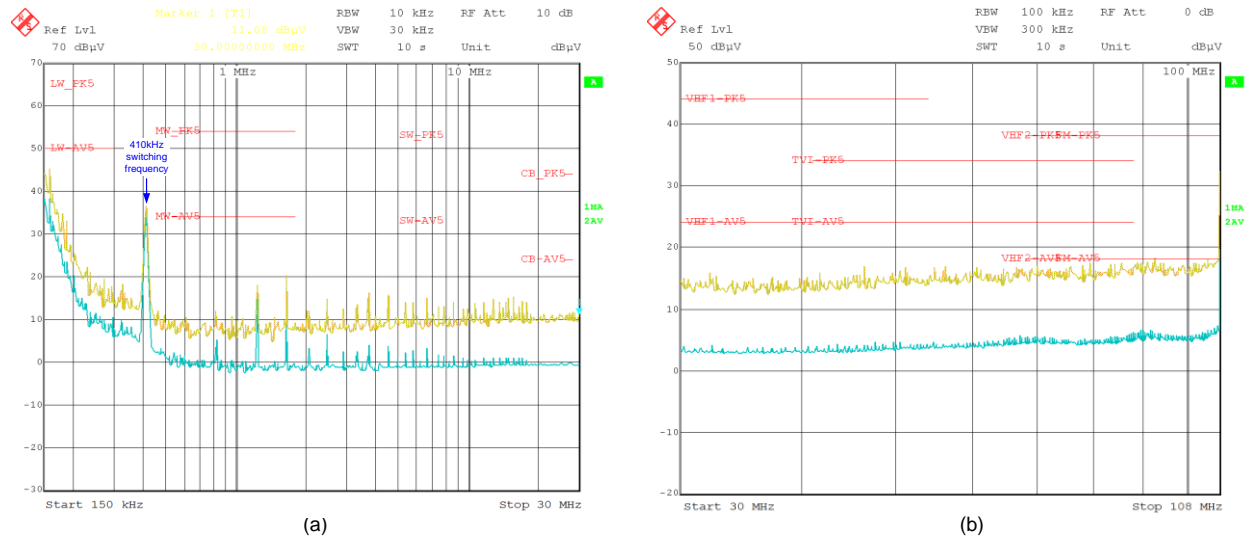waveform with a HotRod FCOL converter (b).

Fig. 10. CISPR 25 conducted emission results, 150 kHz to 30 MHz (a) and 30 MHz to 108 MHz (b).

Summary

In this article I discussed EMI abatement techniques for dc-dc regulator circuits that use a power converter IC. PCB layout steps to reduce EMI are to minimize the current "hot loop" area in the layout, avoid disruption of the current path, use a four-layer PCB with inner ground planes for shielding (yielding much better performance than a two-layer PCB), and route minimal switch-node copper area to reduce e-field radiated coupling.

Converter package type is an important selection criterion, as new device generations show significantly improved performance in terms of switch-node ringing and pinout design for optimal capacitor placement. From an input filtering standpoint, low-frequency noise (generally less than 10 MHz) is relatively straightforward to suppress with a conventional LC filter stage, whereas high-frequency noise (above 10 MHz) typically needs an additional CM choke and/or a ferrite bead filter stage. A metal case shield soldered to the PCB ground plane also effectively mitigates high-frequency emissions.

In the next installment of this series, I'll explore EMI abatement techniques for dc-dc regulator circuits using a controller driving discrete power MOSFETs, which is more challenging from an EMI perspective.

References

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About The Author

Timothy Hegarty is an applications engineer for Power Products Solutions at Texas Instruments. With 20 years of power management engineering experience, he has written numerous conference papers, articles, seminars, white papers, application notes and blogs.

Tim's current focus is on enabling technologies for high-frequency, low-EMI, isolated and nonisolated regulators with wide input voltage range, targeting industrial, communications and automotive applications in particular. He is a senior member of the IEEE and a member of the IEEE Power Electronics, Industrial Applications and EMC Societies.

For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".