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Random PWM Quiets Noise And Reduces Emissions In Three-Phase Inverter Applications

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In power electronics, several pulse width modulation (PWM) schemes have been successfully employed depending on the particular application. Most of the conventional PWM schemes, being deterministic in nature, produce a predetermined harmonic content. This can create a number of issues in real-world applications like the production of acoustic noise, radio interference, and mechanical vibration.[1-4] In applications where interference with the environment and other equipment needs to be mitigated, for example in industrial motor drives, traction drives, electric vehicles, the conventional PWM schemes are inherently noisy and additional equipment like electromagnetic interference (EMI) filters needs to be added.[5]

One available option to cope with these issues is to increase the switching frequency of the conventional PWM schemes i.e.>18 kHz.[6] However, this causes the switching losses to increase significantly. In such applications, random pulse width modulation (RPWM, and also known as spread spectrum switching or spread spectrum frequency modulation) has been found to be effective in mitigating the cited issues without the need of considerably increasing the switching frequency.

In RPWM the width of each switching pulse varies stochastically. This causes the harmonics cluster to spread over a large range thus reducing the size of separate filters or entirely avoiding the use of filters in certain applications. The RPWM technique has successfully been utilized in many power electronics applications such as industrial motor drives where the acoustic noise needs to be checked.

Usually, high-frequency PWM and RPWM signals for sophisticated commercial systems are implemented using digital signal processors (DSPs) and field programmable gate arrays (FPGAs). However, these devices are more generic, powerful, and flexible which makes them quite expensive. Fortunately, similar precision and high-frequency timing requirements needed for RPWM generation can be met with a low-cost Dialog GreenPAK CMIC.

Many suitable RPWM schemes, especially for open-loop applications, can be implemented using Dialog CMICs. Thus, the explicit programming or coding of embedded DSPs, MCUs or FPGAs is replaced by a simple interface provided in the GreenPAK designer. In addition, the size of the overall control circuit is considerably reduced.

There are several ways of producing the RPWM for three-phase inverter applications. In this article, a suitable RPWM technique is presented that can be implemented using the available GreenPAK CMIC's resources. The RPWM technique is implemented using the dual-matrix CMIC SLG46620 [7]. Appropriate theoretical proposals and experimental results are also presented including the output-voltage waveforms and their harmonic content that would justify the proposed strategy. The reference section includes links to the design files required to implement the solution described here.

Proposed RPWM Scheme

The block diagram of the RPWM scheme driving a three-phase inverter is shown Fig. 1.

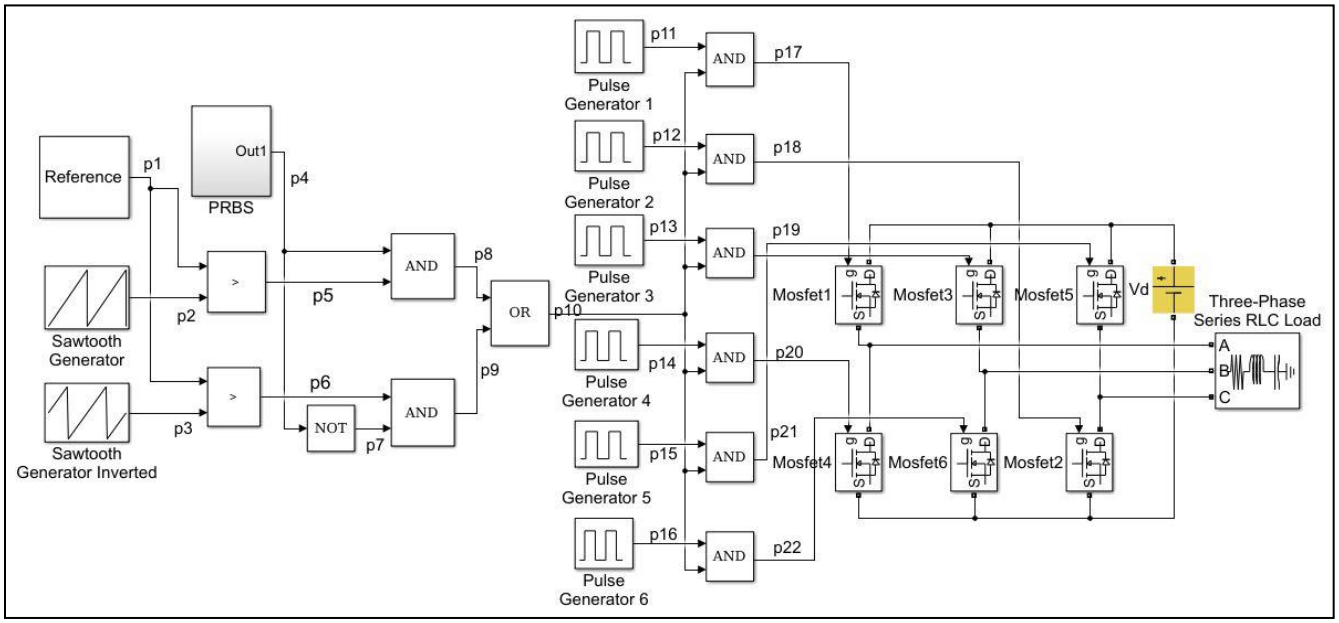

Fig. 1. Block diagram of the proposed scheme for RPWM generation in a three-phase inverter.

Two saw-tooth signals, labeled as p2 and p3 (with values ranging from 0 to 1), 180°C phase apart, are compared with a constant value p1 (with value ranging from 0 to 1) to give different types of pulses labeled as p5 and p6. The waveforms of these pulses (p5 and p6) are shown in Fig. 2.

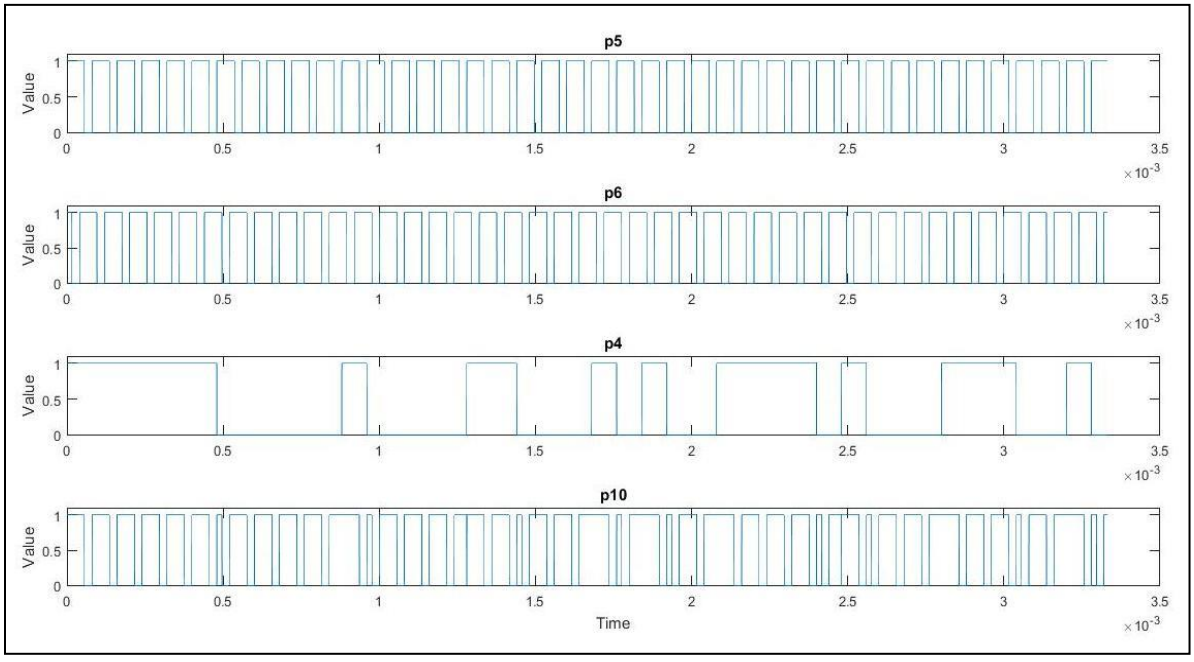

Fig. 2. Simulated signal waveforms at several stages in the RPWM scheme.

A binary pseudo-random number generator (labeled as p4) with the waveform shown in Fig. 2 is employed to randomly select a pulse out of the signals p5 and p6 using the logical operators as shown in the above block diagram. This generates a train of pulses p10, which is also shown in Fig. 2. The signal p10 is passed through

AND gates along with 10-ms long pulses generated by pulse generators 1 through 6 and tagged as p11, p12, p13, p14, p15, and p16.

Note that, the pulse generator output pulses have 60°C phase difference relative to each other for a full 180°C conduction mode. Finally, after AND operations, the signals p17, p18, p19, p20, p21, and p22 become the gate-driving signals for the power switches employed in the power stage of the three-phase inverter.

The switches (usually MOSFETs or IGBTs) are switched on and off according to the applied gate signals to obtain the three phase balanced voltage waveforms at the output of the inverter.

A simulation is carried out in Matlab/Simulink environment for a 50-Hz (fundamental) RPWM three-phase inverter system and the phase-phase output waveforms are shown in Fig. 3. Effectively, the output-voltage waveforms are modulated by the stochastic signal p10 and shifted from one another by 120°C.

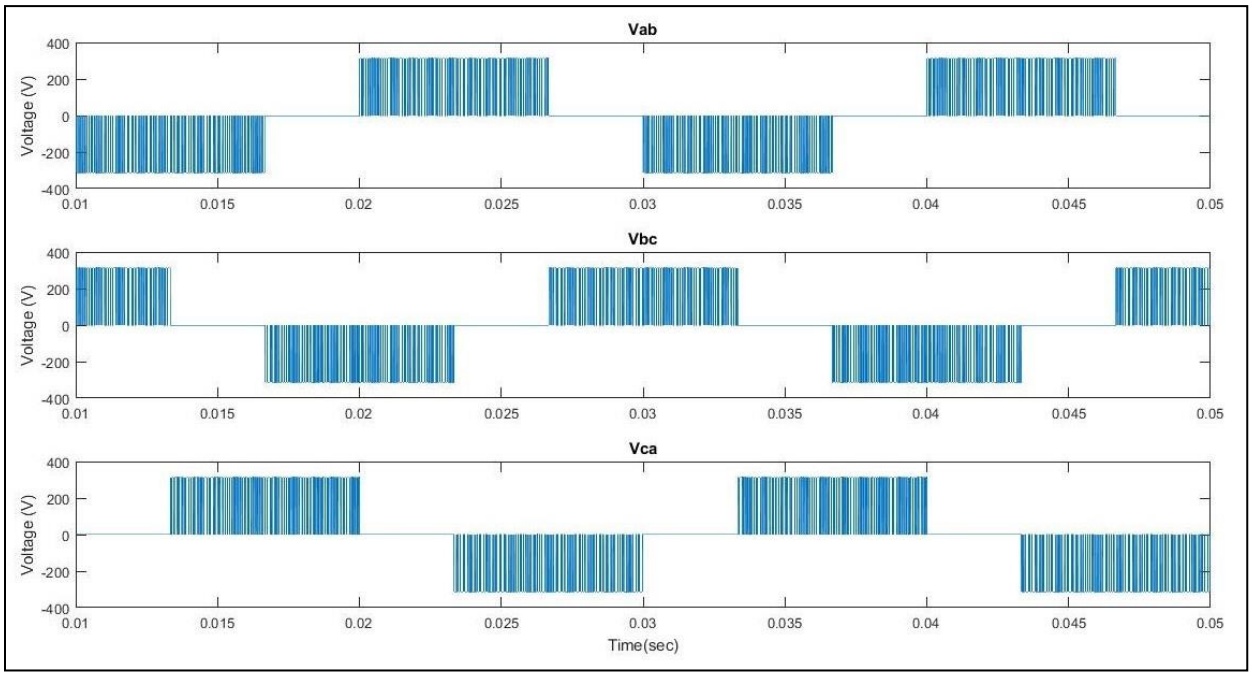

Fig. 3. Simulated output phase-phase voltage waveforms.

Selection Of The Reference Value

The reference signal p1 provides a way to control the spectral content of inverter outputs for a particular application according to the subjective acoustic response. Variation of the reference from 1 to 0.5 flattens out the spectral content mitigating the spikes at the multiples of the switching frequency. However, it also reduces the magnitude of the fundamental component of the signal. Fig. 4 illustrates how the spectral content of the output phase-phase voltage changes by decreasing the reference value from p1 = 0.8 to p1 = 0.5, for Vdc = 312 V and carrier frequency = 12.5 kHz.

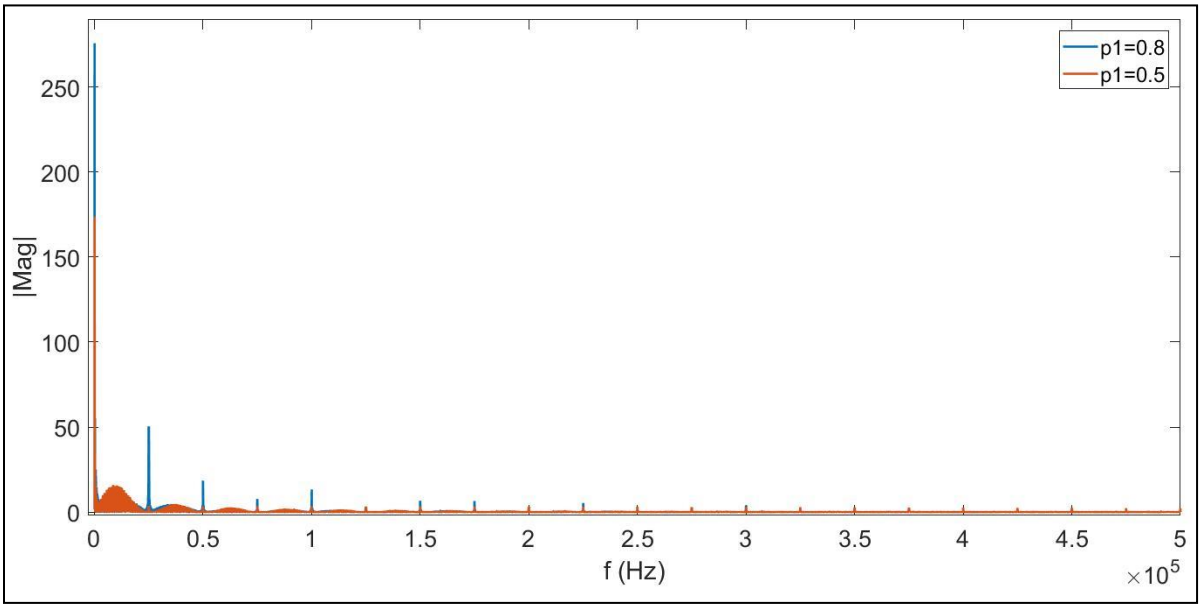

Fig. 4. Variation in frequency spectrum with change in reference value.

Decreasing the value further from 0.5 is not recommended as it starts to increase the spikes at the multiples of the switching frequency and the fundamental component is also reduced.

System Design And Configuration Of The CMIC

Fig. 5 shows how the selected SLG46620 CMIC fits into the entire scheme. The basic operation of the CMIC is to generate the random PWM-modulated signals that are applied at the gate terminals of the switching devices used in the inverter power stage. The SLG46620 CMIC is a member of the GreenPAK family of devices and configuration of this device, which is performed using GreenPAK Designer software,[8] is described in this section.

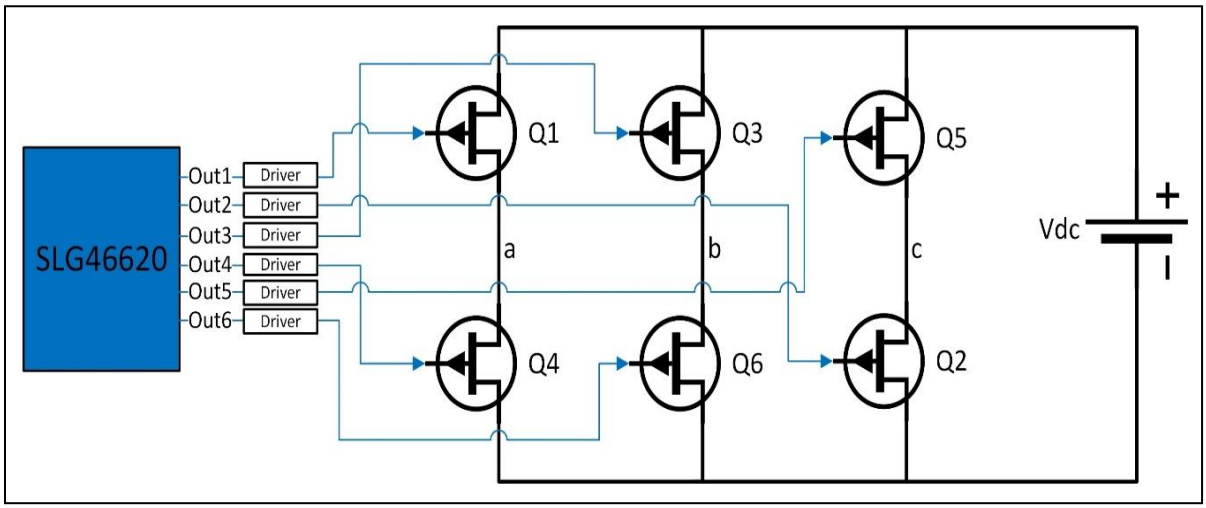

Fig. 5. The role of the SLG46620 in the RPWM scheme.

The fundamental frequency of the inverter output voltage is chosen to be 50 Hz. The SLG46220 is chosen because it provides sufficient resources to carry out the intended design. The SLG46620 has two Connection Matrices, which are used to create the internal routing for internal digital signals inside the device, once it is programmed. The Matrix 0 and 1 designs are shown in Figs. 6 and 7, respectively.

In Matrix 0 a pseudo-random signal (PBRS) P0 is produced by connecting DFFs in a concatenated fashion and using a XOR gate in a feedback loop as shown in Fig. 6. The DFFs are driven by a 12.5-kHz clock signal from OUT0 of the oscillator block.

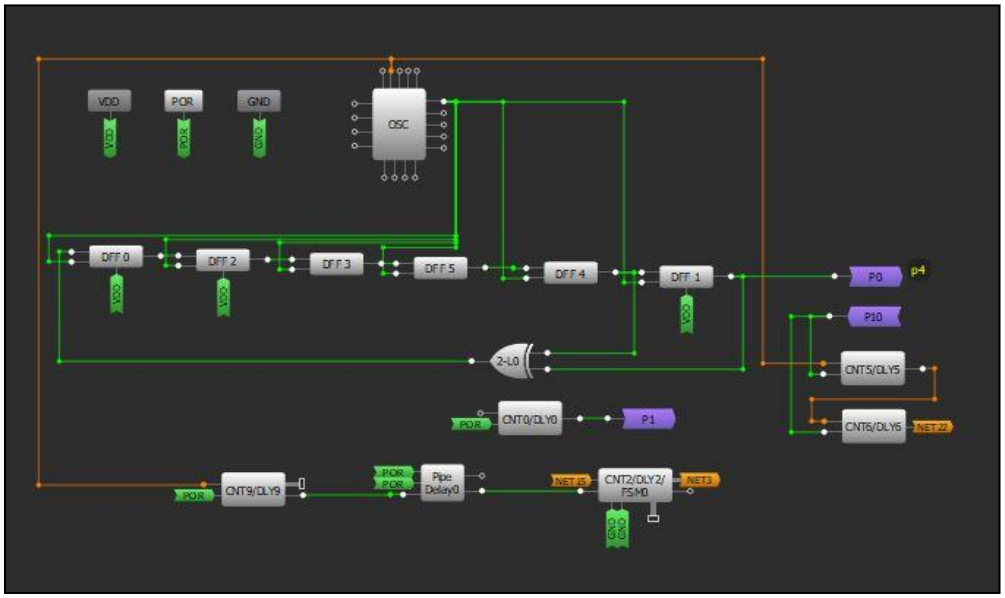

Fig. 6. Design matrix 0.

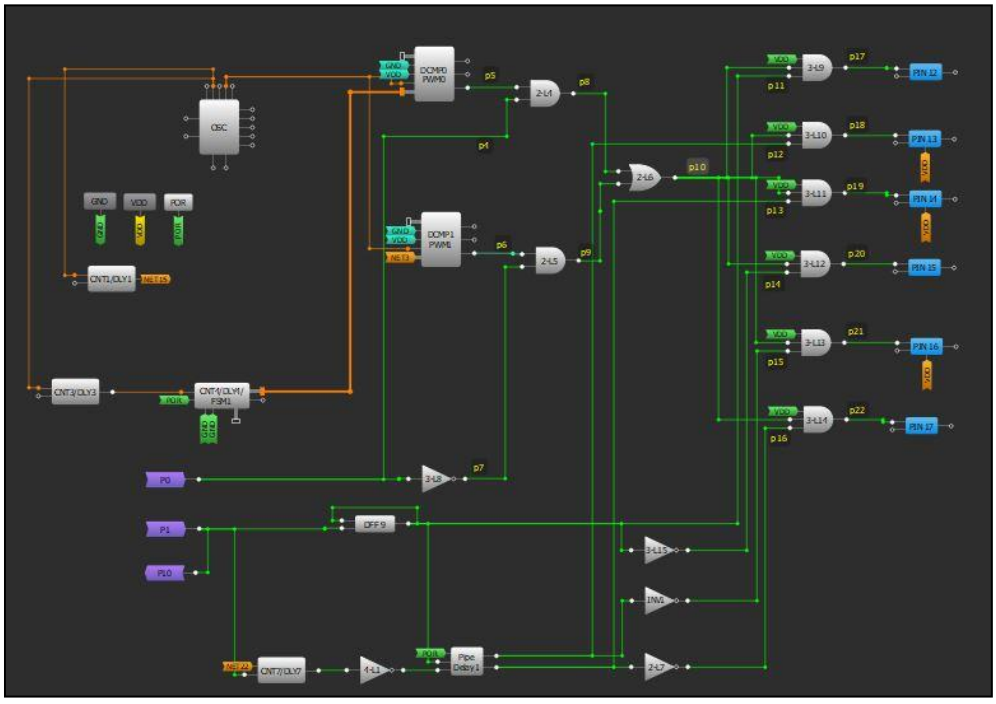

Fig. 7. Design matrix 1.

For the sawtooth carrier signal generation, the use of FSM blocks is proposed. Both FSM0 and FSM1, configured in set mode with UP = 0, are fed by counters CNT1/DLY1 and CNT3/DLY3 respectively, which create pulses having a frequency of 1.6875 MHz. The counter value in both FSMs is set as 134 (output period 80 µs) to achieve the desired 12.5-kHz discrete sawtooth signal. To achieve 180°C phase shift between the two saw-tooth signals FSM0 is enabled 40 µs after FSM1 using a pipe delay fed by CNT9/DLY9.

The two sawtooth carrier signals are fed to DCMP0 and DCMP1, via the Q byte output ports of FSM0 and FSM1, for comparison with a constant reference signal (configured inside the registers DCMP0 and DCMP1) as shown in Fig. 7. Since the counter runs up to a value of 134 the reference value is given with respect to 134 e.g. 67 would be equivalent to the value of 0.5 (67/134).

The outputs of the two DCMPs (p5 and p6) are further passed through to two AND gates along with the output signal from the LFSR (p4) and its inverted value (p7). An OR gate is fed with the output of these AND gates to randomly obtain one of the two outputs of the DCMPs. The output of the OR gate (p10) is further used to modulate the driving signals of the inverter.

The counter CNT0/DLY0 is configured to produce pulses with a 10-ms period in order to have output voltages of 50-Hz frequency (fundamental). These pulses are fed to a DFF configured in an inverting mode, with the output fed back to the input, to produce a 50-Hz square-wave pulse train. To ensure that the output pulses labelled as p11 through p16 are 60°C phase apart, the use of a pipe delay block is proposed.

The counters CNT5/DLY5, CNT6/DLY6 and CNT7/DLY7 are cascaded to provide pulses with a period of 3.33 ms. These pulses are fed to a pipe delay through a not gate since the pipe delay creates delay by counting the number of input rising edges whereas the counters get reset to 0 with the reset input. This creates coinciding falling edges with a period of 3.33 ms. Out 0 and 1 of the pipe delay provide 3.33 ms and 6.66 ms time delays respectively to the input pulse.

The three signals i.e. input and the two delayed outputs of the pipe delay are further inverted to provide a total number of 6 pulses (p11 to p16) that are 60° phase shifted to each other. These 50-Hz, 60°C phase-shifted pulses are further passed to AND gates along with the random pulse train (p10) to provide the final driving signals for the three-phase inverter.

Experimental Results

A hardware prototype depicted in Fig. 8 was developed to experimentally validate the proposed RPWM scheme. To ensure that both switches in the same leg do not turn on at the same time a dead band was produced in hardware.

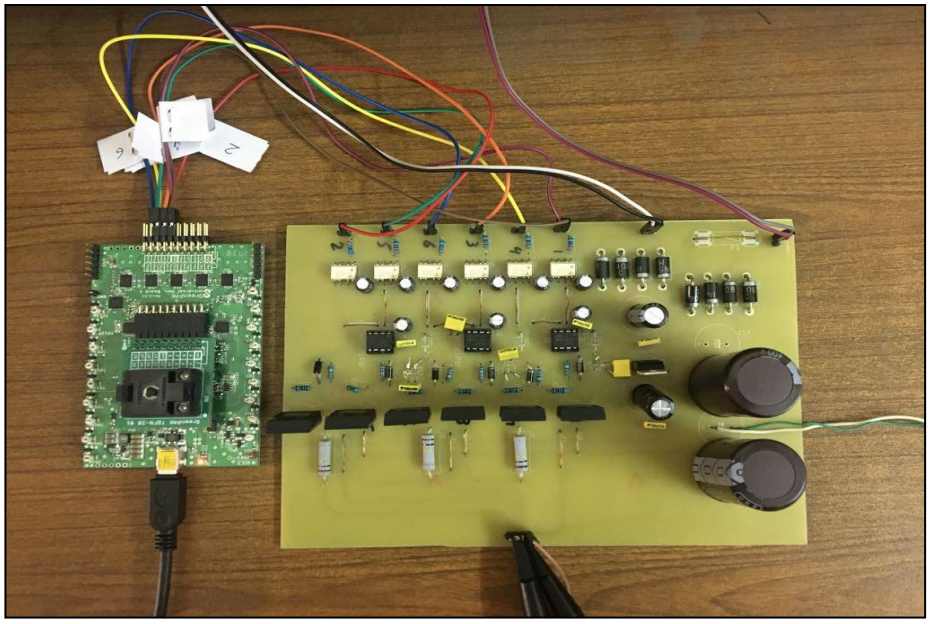

Fig. 8. Prototype hardware.

Fig. 9 shows the magnified waveform of the output phase-phase voltage. It is evident that the waveform is randomly modulated as desired.

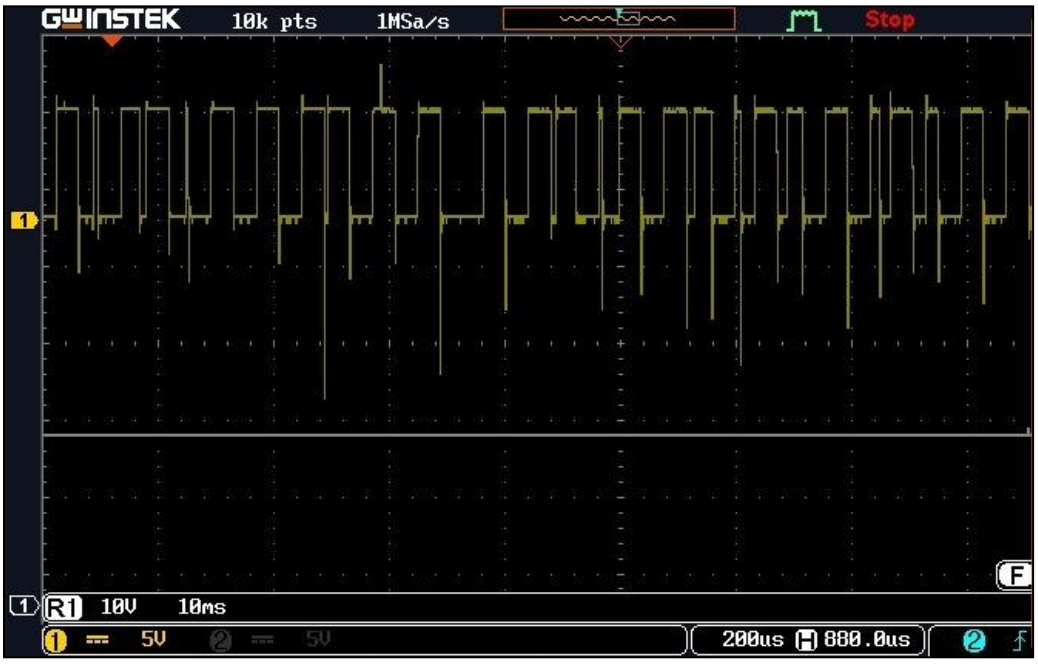

Fig. 9. Magnified phase-phase output voltage waveform.

In Fig. 10 the output phase-phase voltage signals Vab (in yellow) and Vac (in blue) are shown. Moreover, the FFT plot of Vab (in red) for a reference value ≈ 0.8 (107/134) is also depicted. Though the spread in the frequency spectrum is evident, a spike at twice the switching frequency i.e. 25 kHz is observed as the theory suggests.

Fig. 10. Vab, Vac and FFT for a reference value of ≈0.8.

Fig. 11 depicts the output phase-phase voltage signals Vab (in yellow) and Vac (in blue) as well as the FFT plot of Vab (in red) for a reference value = 0.5 (67/134). It can be seen the spectrum gets flatter and significant spread is also achieved.

Fig. 11. Vab, Vac and FFT for a reference value of 0.5.

For related documents and software, see the company website.[9] Download the free GreenPAK Designer software[8] to open the .gp files[10] and view the proposed circuit design. Use the GreenPAK development tools[11] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes[12] featuring design examples as well as explanations of features and blocks within the Dialog IC.

Conclusion

RPWM signals for three-phase inverters can be generated using different techniques and usually expensive DSPs and FPGAs are used in industrial applications to achieve the desired results. In this article, a suitable RPWM generation technique for three-phase inverter applications using a low-cost CMIC has been outlined. Through appropriate simulations and experimental results, it has been established that the proposed technique is functional and the SLG46620 IC provides sufficient resources to carry out the intended results.

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For more information on techniques for reducing emissions, see How2Power's Power Supply EMI Anthology. For more on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC inverters".