Symposium Tackled EOS And ESD Challenges Across The Electronics Spectrum Including Power Design

by David G. Morrison, Editor, How2Power.com

The recent EOS/ESD Symposium and Exhibits, held September 20-28 in Reno, NV, drew a total of 572 attendees to participate in tutorials, exhibits, workshops, discussion groups, technical sessions, invited talks and hands-on sessions on EOS and ESD topics. The symposium, which celebrated its 40th anniversary this year, was a unique forum for engineers to address their ESD challenges by learning best practices and discovering the latest technology for ESD control, protection and design. Moreover, it addressed EOS and ESD issues at the device, board and system level, making it relevant to engineers across the electronics spectrum, including developers of power semiconductors, power converters and power systems.

As Kevin Parmenter, chair of the PSMA Safety and Compliance Committee, observes, there are several trends in the EOS and ESD area that are particularly relevant. "In the power electronics industry, the end equipment must survive IEC tests for EFT (electrical fast transients) and ESD and more organizations are considering EFT and ESD problems to be solved as part of a comprehensive EMI-RFI mitigation plan." He adds that these requirements are compounded by those in automotive and other markets, which have their own ESD and EFT protection requirements such as those spelled out in IEC, EN and SAE specs.

The proliferation of digital interfaces is another factor. "With more digital ports on everything, including power electronics with PMBus interfaces, those ports are subject to EFT-ESD testing and protection is needed to achieve compliance to the relevant system-level standards," says Parmenter. Another growth area that merits attention is isolation. Kevin notes that "with more isolation in systems, the isolators will be subjected to ESD-EFT testing and events. These devices must work properly and last for a long time even when subject to these ESD-EFT events."

As electronic systems of all types advance, their vulnerability to EOS/ESD events grows and the need to understand these threats through better modeling and testing becomes more imperative. Designers also need to understand how standards in this field are evolving. A look at the 2018 symposium program reveals how the conference helps engineers in these pursuits. Note that there were tracks here addressing requirements of both design and manufacturing.

Among the many interesting sessions held at this year's symposium, certain ones were of particular interest to engineers in power electronics. These included the keynote "Electrified Automobility—Protecting Driver and Electronics" by Hans Stork, senior vice president and chief technology officer (CTO) at ON Semiconductor. His talk specifically addressed the needs of power devices in automotive applications:

Hans Stork's keynote reviewed recent progress in high power integrated circuit processes for drivetrain and other mechanical functions, discrete power devices for battery management and electromotor control, and image sensors for ADAS support, highlighting unique restrictions to manage stress conditions.

"*With the expected rapid increase of automotive electrification, all but a few functions of the automobile will be electronic. Power devices and image sensors are becoming essential components to realize the future of "automobility". They will need to survive the extreme use/stress conditions (temperature, humidity, vibration) and meet the consumer expectations (zero failures and affordable cost). This talk will review recent progress in high power integrated circuit processes for drivetrain and other mechanical functions, discrete power devices for battery management and electromotor control, and image sensors for ADAS support, highlighting unique restrictions to manage stress conditions. The challenge of simultaneously*

meeting a wide range of power density, temperature, cost, and reliability requirements is feasible thanks to ongoing progress in understanding, modeling, and innovation."

In the tutorial sessions, one that stood out for its relevance to power electronics was "ESD Design in HV Technologies" taught by Lorenzo Cerati, STMicroelectronics and Yiqun Cao, Infineon Technologies.

"*This tutorial gives an introduction to ESD design in high voltage technologies for integrated circuits with pin voltages from 12 volts upwards. After a short introduction of typical applications and requirements, an overview of different technologies and the typical device portfolios in these technologies will be given. Different ESD protection concepts are introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback devices, active clamps, etc.). Finally, HV technology and design related challenges regarding ESD protection are discussed, with a special focus on the formation of parasitic bipolar devices and the impact on the circuit's ESD performance. The attendee will gain a good basic knowledge of the main characteristics of HV technologies, the different ESD protection concepts, and ESD protection challenges that are specific for HV technologies…*"

For those developing power chips, a tutorial on "Design for EOS Reliability" given by Charvaka Duvvury, ESD Consulting, LLC seemed especially helpful as it addressed "designs in low voltage CMOS, mixed voltage technologies, analog designs, and high voltage designs".

In the technical sessions, among the many papers that may be useful in power electronics, there were two that seemed pertinent to power supply applications. One was "Modeling the Transient Behavior of MOS-Transistors during ESD and Disturbance Pulses in a System with a Generic Black Box Approach" by Michael Ammer, Infineon Technologies, Federal Armed Forces Munich; Andreas Rupp, Yiqun Cao, Infineon Technologies; Martin Sauter, Linus Maurer, Federal Armed Forces Munich. This talk was focused on protection of smart power devices:

"*On-chip ESD protection in smart power technologies is often done with MOSFETs, either self-protecting or as dedicated ESD-protection. Turned on by intrinsic capacitive coupling they show dynamic channel current as well as special high current effects. A generic approach to model this transient behavior for system ESD simulation is presented*."

Another interesting paper was "Power-Rail ESD Clamp Circuit with Polysilicon Diodes Against False Trigger During Fast Power-ON Events" by Jie-Ting Chen and Ming-Dou Ker, National Chiao-Tung University".

"*A new power-rail ESD clamp circuit with both timing and voltage-level detection mechanisms is proposed against false trigger events. The diode string is used to detect the overstress voltage level during ESD events. By using the polysilicon diode, the standby leakage current along the proposed power-rail ESD clamp can be effectively reduced."*

In addition to the extensive conference program, the symposium also hosted an exhibition with over 40 companies presenting a range of products and services for static protection, control, testing, and analysis. These exhibits were not just for conference attendances as they were open to the public.

Attending this type of expo provides very practical and immediate benefits for engineers seeking to address ESD challenges. As Jim Miller, the 2018 EOS/ESD Symposium general chair, noted "The exhibits offer a unique opportunity to meet professionals with hands-on experience on static control methods, evaluation techniques, ESD testing hardware, and many other ESD solutions." A full list of participating companies is listed in the program (see page 41).

This article has provided just a small sampling of talks given at the symposium and notes on the exhibition. No doubt many of the other talks addressed general EOS/ESD design and test issues that may be relevant in your work in the power electronics field. For more about this year's symposium, browse the full program for the 2018

EOS/ESD Symposium and note those sessions, speakers and companies of interest. Then mark your calendars for next year's EOS/ESD Symposium, which will be held September 11-20, 2019 at the Riverside Convention Center in Riverside, CA. Take advantage of this highly focused industry gathering to address your EOS/ESD challenges.

For those interested in presenting at next year's symposium, see the 2019 call for papers or if you are a student, see the special call for student papers. To see a list of who's already signed up to exhibit next year, or for more information on how your company can exhibit, see symposium exhibits. For further information about next year's symposium, contact Lisa Pimpinella at 315-339-6937 or info@esda.org.