

Closing The Loop Of An Active-Clamp Forward Converter

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Active-clamp forward (ACF) converters are popular in the world of high-frequency dc-dc bricks: near-zero-voltage switching, reduced-size magnetics and high-efficiency designs are among the benefits brought by an ACF. If designing the power stage requires care as for any high-power design, the complicated control-to-output transfer function of the converter requires a good understanding of compensation strategies to meet design goals such as crossover and phase margin.

This article describes in detail how to compensate an ACF. After reviewing the operation of an ACF power stage, the article introduces the ACF transfer function, explains its components, shows Bode plots for a design example based on the NCP1566 active-clamp PWM controller, and discusses selection of the crossover frequency. The impact of the pulse-width modulator (PWM) on the transfer function is also explained, along with a technique for accounting for the PWM.

Next, the design of a type-3 compensator, which is required by the ACF, is described. This is followed by a strategy for applying this compensator to the ACF, which is demonstrated using a Simplis simulation of the aforementioned design example. The complete circuit for the design example including the compensator is then presented; its key features, circuit elements and additional design considerations are discussed.

Finally, a common technique for making the Bode plot measurements of the loop's gain and phase margins is reviewed and the benefits of using a low-cost oscilloscope and frequency response analyzer (Cleverscope) to make these measurements are highlighted. Loop measurements taken on the design example are presented and discussed.

Power Stage Operation

Fig. 1 shows the simplified sketch of an ACF whose operation details are described in reference [1]. Basically, transistor Q_1 operates as in a classical forward converter but when it turns off, the demagnetization process involves a resonant cycle between clamp capacitor C_{clp} and primary inductance L_{mag} .

Part of the energy stored in the magnetizing inductance transfers the capacitance lumped at the drain connection and $v_{DS}(t)$ rises until it finds a path through the Q_2 body diode. This latter is then shorted by turning Q_2 on in the zero voltage switching (ZVS) condition: Q_1 's drain is now clamped to V_{in} plus V_{clp} , the voltage across C_{clp} . Considering the resonant cycle between L_{mag} and C_{clp} , the circulating current eventually reverses and finds a path through Q_2 (still on) and the magnetizing inductance L_{mag} .

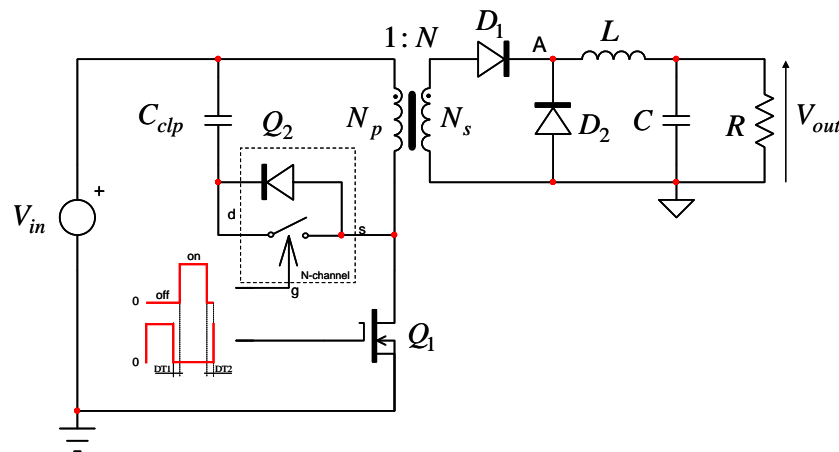


Fig. 1. An active-clamp forward converter can be operated at a high switching frequency because of its use of zero-voltage switching.

At some point, the controller will instruct Q_2 to open, forcing the current to leave the mesh including C_{clp} , naturally finding its way through the input source V_{in} and the drain lumped capacitance: the drain node voltage starts decreasing towards ground until a new switching cycle takes place with reduced turn-on losses.

As illustrated in Fig. 2, a dead time is inserted between the MOSFETs' transitions, giving time to the resonating drain-source cycle now involving L_{mag} and C_{lump} to reach a valley point. For certain operating conditions (lower output current), the drain wave touches ground, leading to zero turn-on losses.

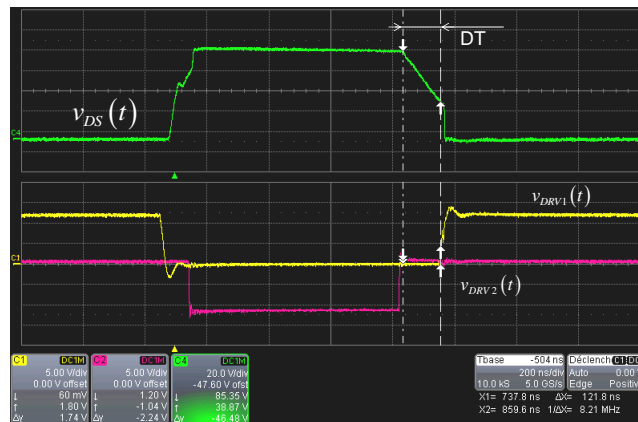


Fig. 2. When the dead time is well adjusted, near-ZVS operation can be obtained.

The Transfer Function

Before compensating a converter or any system, you need the control-to-output transfer function of the power stage. In other words, if you stimulate the control input—the pulse width modulator (PWM) in this case—with a sinusoidal waveform, how does the information propagate through the power stage and create a response in the output? The mathematical relationship linking the response to the stimulus is the transfer function H we need.

The control-to-output transfer function of an ACF operated in voltage mode has been derived in reference [1] and describes the converter via a fourth-order polynomial form:

$$H(s) = \frac{V_{out}(s)}{D(s)} = H_0 \frac{1 + \frac{s}{\omega_{2F}}}{1 + \frac{s}{\omega_{0F}Q_F} + \left(\frac{s}{\omega_{0F}}\right)^2} \cdot N \left(V_{in} - D_0 r_{on1} M_0 \frac{s C_{clp}}{1 + \frac{s}{\omega_{0M}Q_M} + \left(\frac{s}{\omega_{0M}}\right)^2} \right) \quad (1)$$

The equation is made up of two parts: the left-hand term is that of the classical forward converter in which

$$\begin{aligned} H_0 &= \frac{R_{Load}}{R_{load} + r_L} \\ \omega_{2F} &= \frac{1}{r_C C_{out}} \\ \omega_{0F} &= \frac{1}{\sqrt{L_{out} C_{out}}} \sqrt{\frac{r_L + R_{load}}{r_C + R_{load}}} \\ Q_F &= \frac{L_{out} C_{out} \omega_{0F} (r_C + R_{Load})}{L_{out} + C_{out} [r_L r_C + R_{load} (r_L + r_C)]} \end{aligned} \quad (2)$$

The second term in equation (1) represents the addition of the active-clamp circuitry and the influence of the resonating network built around C_{clp} and L_{mag} :

$$\begin{aligned} \omega_{0M} &= \frac{1 - D_0}{\sqrt{L_{mag} C_{clp}}} \\ Q_M &= \sqrt{\frac{L_{mag}}{C_{clp}}} \frac{1 - D_0}{r_{on2} (1 - D_0) + D_0 r_{on1}} \\ M_0 &= \frac{V_{clamp}}{(1 - D_0)^2} \end{aligned} \quad (3)$$

In these expressions, r_L and r_C are the equivalent series resistances (ESRs) of the output inductor (L_{out}) and capacitor (C_{out}), respectively; r_{on1} designates the main switching transistor $r_{DS(on)}$; r_{on2} represents the active-clamp transistor $r_{DS(on)}$; N is the transformer turns ratio while D_0 expresses the static duty ratio.

From this expression in (1), we can obtain a Bode plot graphing the magnitude and phase response along a 10-Hz to 100-kHz frequency range (Fig. 3). Values for the various components are those of a 3.3-V/30-A dc-dc brick built around an NCP1566 active-clamp PWM controller from ON Semiconductor.^[2] The active-clamp section is purposely undamped and assumes a low $r_{DS(on)}$ MOSFET for Q_2 .

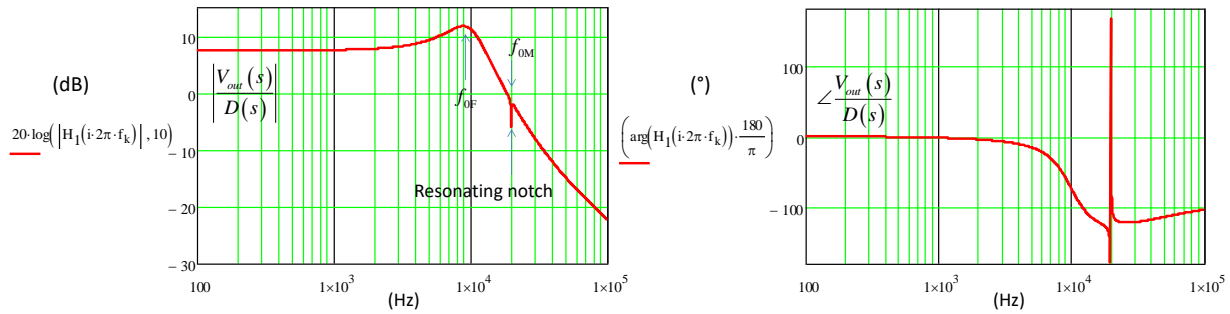


Fig. 3. The control-to-output transfer function shows a resonating notch stressing the phase where the double zeros appear.

You can observe a magnitude glitch associated with a severe phase distortion as the frequency reaches the resonance described by equation (3). The magnitude dip is imputed to the sudden increase of resonating currents in the primary side which induces a voltage drop across the primary-side power MOSFET Q_1 . This drop subtracts from the input voltage V_{in} as described by the right-side term in (1) and creates the observed notch on the response.

As recommended by references [3] and [4], it is wise to select a crossover point located before the minimum resonant frequency of $L_{mag}-C_{clp}$ considering the severe phase lag at this point. However, if proper damping is applied across the active-clamp circuit, then crossover can be extended.

The impact of such a decision on the main MOSFET drain-source peak voltage during transient conditions must be carefully studied as shown in reference [5]. Fig. 4 illustrates the same transfer function now damped by the $2.5-\Omega r_{DS(on)}$ of Q_2 : the magnitude and phase responses are very close to that of a classical forward converter and f_c can be chosen beyond the resonating notch.

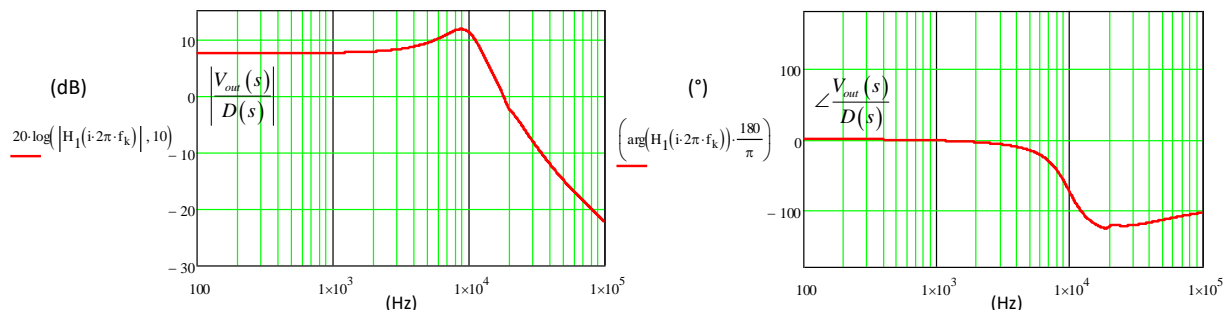


Fig. 4. When damped, the resonant glitch effect is attenuated and you can push crossover beyond resonance.

The Pulse Width Modulator

The expression given in equation (1) does not include the contribution of the PWM block. In an isolated dc-dc converter, an optocoupler will bias the controller feedback pin to control the duty ratio as the regulation loop lies in the secondary side. An implementation commonly found in high-power converters is the shunt regulator: rather than pulling down a pin to ground via a common-emitter configuration, the optocoupler connects to the controller by its emitter and injects a current (Fig. 5). This current is internally mirrored to pull down an internal node loaded by a $50\text{-k}\Omega$ resistance. This voltage biases the PWM comparator and ensures regulation.

This technique minimizes the Miller effect of the optocoupler considering the quasi-constant V_{CE} voltage as the drop across the input dynamic resistance is small: the optocoupler pole is pushed towards higher frequencies and will be less of a concern for closing the loop. The dynamic resistance r_d is equal to $400\ \Omega$ but plays no role

in the frequency analysis. It would have an impact if one would connect a capacitor from the feedback pin to ground. However, besides this configuration, the resistance is ac-transparent as the optocoupler alone fixes the injected current. This current undergoes a division by 10 (noted as *div* in equations that follow) and through the pull-up resistance, fixes the internal operating point.

On the inverting pin, timing capacitor C_{ramp} is charged by a current depending on the input voltage. As such, the slope of the artificial sawtooth will be tied to the input voltage, dynamically changing the gain as V_{in} varies. This configuration implements what we call a *feedforward* action. It is possible to show^[6] that the small-signal gain of this modulating cell is equal to:

$$G_{PWM} = \frac{D(s)}{V_{err}(s)} = \frac{1}{k_{FF} V_{in}} \quad (4)$$

with

$$k_{FF} = \frac{1}{F_{sw} R_{ramp} C_{ramp}} \quad (5)$$

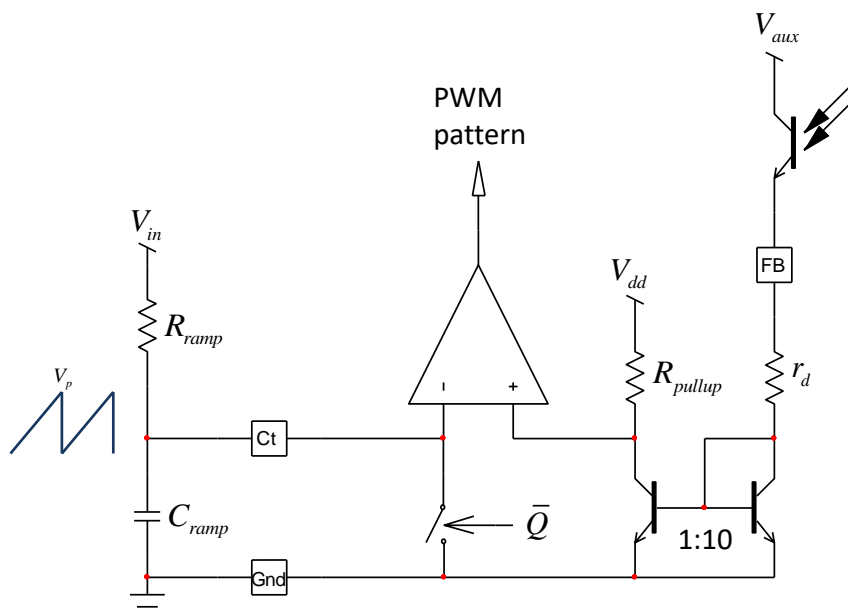


Fig. 5. The optocoupler injects current in the feedback pin to adjust the controller duty ratio.

In equation (1), you see the term V_{in} appearing on the right side of the equation. It tells you that the dc gain (for $s = 0$) of the transfer function will vary in relationship with the input voltage. Consequently, the crossover frequency and possibly stability can be affected. By including the PWM transfer function described by equation (4), the division by V_{in} in the denominator cancels the contribution of the input voltage, stabilizing the loop gain and crossover frequency along the input range.

In this case, the transfer function simplifies to the following expression if we consider a fully-damped response where the resonant contribution is neglected as in Fig. 4:

$$H(s) = \frac{V_{out}(s)}{V_{err}(s)} \approx \frac{H_0}{k_{FF}} \frac{1 + \frac{s}{\omega_{zF}}}{1 + \frac{s}{\omega_{0F}Q_F} + \left(\frac{s}{\omega_{0F}}\right)^2} \cdot N \quad (6)$$

A Type 3 Compensator

To design the loop gain of our ACF converter, we will need the transfer function linking the PWM pattern $D(s)$ —the stimulus—to the observed variable, $V_{out}(s)$ —the response. We will apply the selected design strategy via a poles-zeros placement to ensure converter robustness and a good transient response.

Fig. 6 represents a typical configuration involving a type 3 compensator whose isolation is provided by the optocoupler. This optocoupler itself is affected by a current transfer ratio (CTR) and a pole whose position depends on the loading resistance.

In this application, a shunt-regulated feedback input reads the optocoupler current. The loading resistance r_d is quite small, implying a rather high-frequency optocoupler pole that we must characterize anyway to later neutralize it.^[7] Please note the LED connection to a quiet V_{cc} point (or auxiliary voltage V_{aux}) in the secondary side, perfectly ac-decoupled from V_{out} . It is important to underline this point otherwise a fast lane (another modulation path) will be created, distorting the frequency response of the compensator.^[7]

The ac current in the LED (neglecting its dynamic resistance) is given by

$$I_{LED}(s) = -\frac{V_{op}(s)}{R_{LED}} \quad (7)$$

in which V_{op} is the op-amp ac output voltage. Considering a perfect op-amp, this voltage is defined as

$$V_{op}(s) = -\frac{Z_f(s)}{Z_i(s)} V_{out}(s) \quad (8)$$

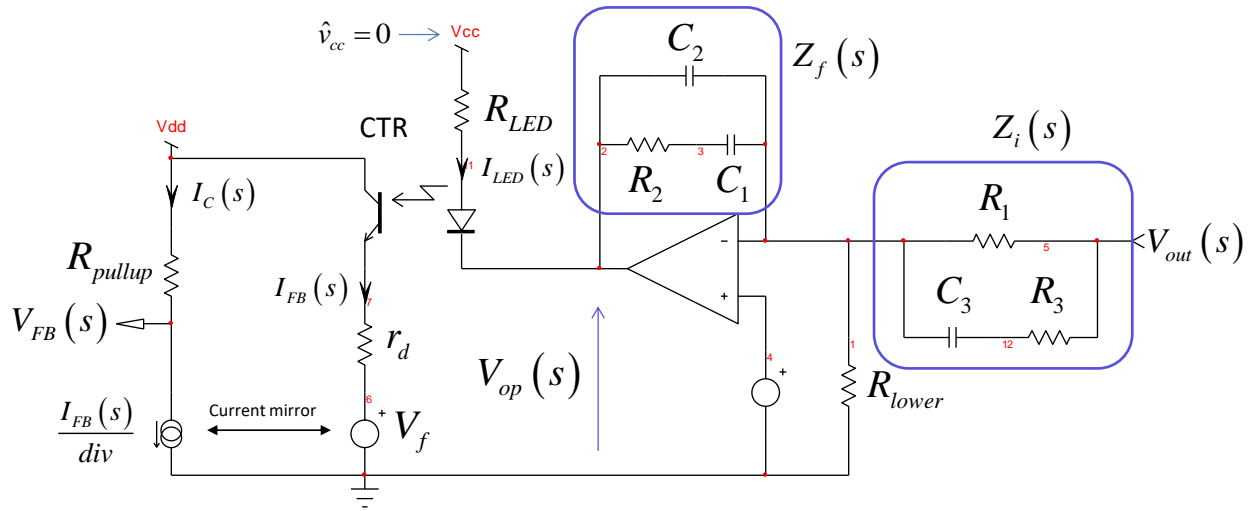


Fig. 6. A type-3 compensator is necessary to close the loop with a voltage-mode active-clamp forward converter. In this example, R_{pullup} is 50 k Ω , R_{LED} is arbitrarily fixed to 1 k Ω while R_1 is 1662 Ω .

Z_f and Z_i are the impedances circled in the Fig. 6 schematic. From these two networks, we can already infer the position of the zeros of the transfer function we want, using the fast analytical circuits techniques.^[8] For which impedance combination of Z_f and Z_i will the output V_{FB} be nulled despite an excitation in V_{out} ?

There are two conditions:

1. If Z_i magnitude becomes infinite when V_{out} is tuned at s_z , then $V_{FB}(s_z) = 0$ V. Z_i is made of a numerator and a denominator $D(s)$. When $D(s_z) = 0$, this impedance is infinite. As thus, the pole of this first-order network is the zero we are interested in. The time constant affecting Z_i is obtained by temporarily disconnecting C_3 and "looking" at the resistance offered through its connecting terminals. In our head, the time constant is $C_3(R_1 + R_3)$ and the network pole or the transfer function zero is simply $\omega_{z_1} = 1/[C_3(R_1 + R_3)]$.
2. The output null is also obtained when the series combination of R_2 and C_1 forms a transformed short circuit. This impedance is defined as $Z_f(s) = R_2 + 1/sC_1$. You obtain the zero position solving $Z_f(s) = 0$ leading to the definition of the second zero located at $\omega_{z_2} = 1/R_2C_1$.

Accounting for these results and by manipulating the equations, we can show^[6] that equation (8) updates to

$$V_{op}(s) \approx -V_{out}(s) \frac{R_2 \left(1 + \frac{1}{sR_2C_1}\right) (1 + sC_3R_1)}{R_1 (1 + sR_3C_3) (1 + sR_2C_2)} \quad (9)$$

when considering $R_3 \ll R_1$ and $C_2 \ll C_1$.

The LED current is obtained by substituting equation (9) into (7):

$$I_{LED}(s) = V_{out}(s) \frac{R_2}{R_{LED} R_1} \frac{\left(1 + \frac{1}{sR_2 C_1}\right) (1 + sC_3 R_1)}{(1 + sR_3 C_3)(1 + sR_2 C_2)} \quad (10)$$

The output voltage V_{FB} is the optocoupler emitter current scaled by the current mirror division ratio div :

$$V_{FB}(s) = -\frac{I_{FB}(s)}{div} R_{pullup} \quad (11)$$

The emitter current is the LED current affected by the CTR:

$$I_{FB}(s) = I_{LED}(s) CTR \quad (12)$$

Combining all these expressions with equation (10) we have the complete transfer function we want:

$$\frac{V_{FB}(s)}{V_{out}(s)} = -\frac{R_{pullup} CTR}{R_{LED} \cdot div} \frac{R_2}{R_1} \frac{\left(1 + \frac{1}{sR_2 C_1}\right) (1 + sC_3 R_1)}{(1 + sR_3 C_3)(1 + sR_2 C_2)} \quad (13)$$

It can be expressed in the following *low-entropy* format featuring an inverted zero in the numerator:

$$\frac{V_{FB}(s)}{V_{out}(s)} = -G_0 \frac{(1 + s_{z_1}/s)(1 + s/s_{z_2})}{(1 + s/s_{p_1})(1 + s/s_{p_2})} \quad (14)$$

in which we have

$$G_0 = \frac{R_2}{R_1} \frac{R_{pullup} CTR}{R_{LED} \cdot div} \quad (15)$$

$$\omega_{z_1} = \frac{1}{R_2 C_1} \quad (16)$$

$$\omega_{z_2} = \frac{1}{R_1 C_3} \quad (17)$$

$$\omega_{p_1} = \frac{1}{R_3 C_3} \quad (18)$$

$$\omega_{p_2} = \frac{1}{R_2 C_2} \quad (19)$$

Now that we have our compensator transfer function on hand, we need a means to adjust the wanted gain or attenuation at crossover. This is obtained by selecting the right value for R_2 while considering the other component values fixed by design or imposed by the manufacturer (R_{pullup} in the circuit for instance). The magnitude of equation (12) is determined as follows:

$$|G(f_c)| = \frac{R_2}{R_1} \frac{R_{pullup}}{R_{LED} div} \frac{CTR}{R_2 C_2} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (20)$$

From which you can extract the correct value for R_2 knowing that $|G(f_c)|$ represents the wanted gain or attenuation at the selected crossover frequency f_c :

$$R_2 = |G(f_c)| \frac{R_1 R_{LED} div}{R_{pullup} CTR} \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (21)$$

Once R_2 's value is known, you can pursue the calculations for the rest of the compensation elements using equations (15) to (18).

The Compensation Strategy

With the complete type 3 transfer function on hand, we can think of a compensation strategy based on the power stage response of the converter we want to stabilize. We have several options to obtain this response. We can either compute it with Mathcad and the analytical expression we gave in (1) or measure it on the bench. For this last option, we need working hardware. Another viable alternative is the SIMPLIS simulation circuit of Fig. 7.

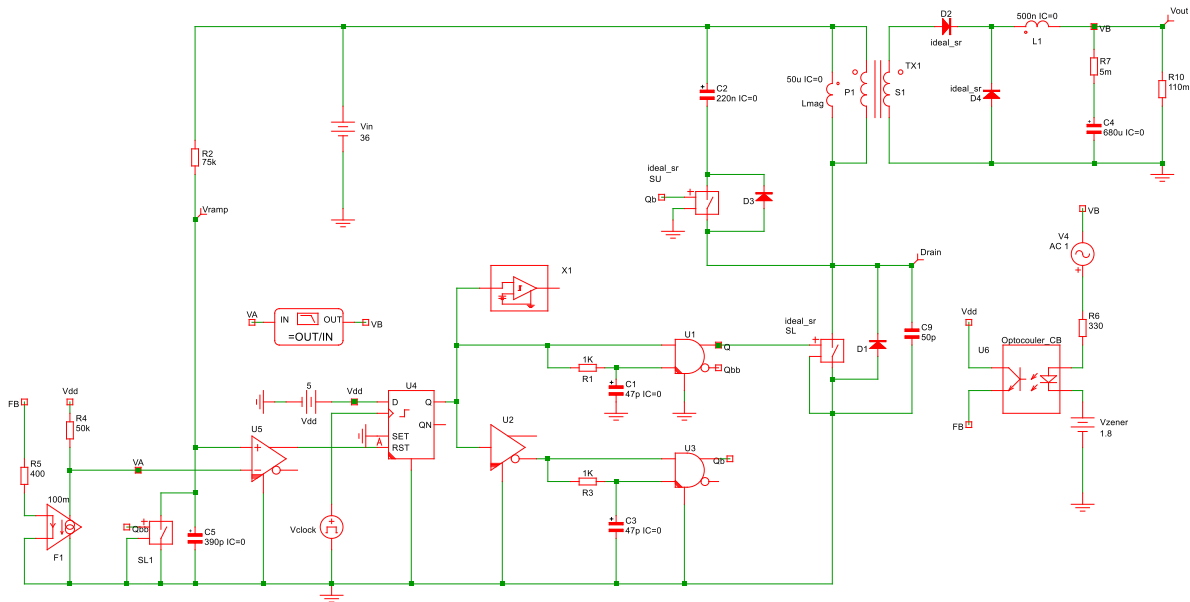


Fig. 7. This simple closed-loop ACF template operates with the demonstration version Elements.

SIMPLIS is a piece-wise linear (PWM) simulator which lets you extract the small-signal response from a switching converter. Considering the simple simulated circuit, the control-to-output response or $V_{out}(s)/D(s)$ can be obtained in a few seconds from the demonstration version Elements.^[9]

The phase and magnitude graphs are given in Fig. 8. This response corresponds to that of a converter delivering 3.3 V/30 A from a 36-V to 72-V input line. The main controller is an NCP1566 from ON Semiconductor which operates at a 500-kHz switching frequency. The transformer turns ratio is 6:1 while the secondary-side inductor is 0.5 μH. The glitch incurred to the active-clamp resonating network is well under control and we can safely crossover beyond it. We will select a 30-kHz crossover frequency f_c for this example.

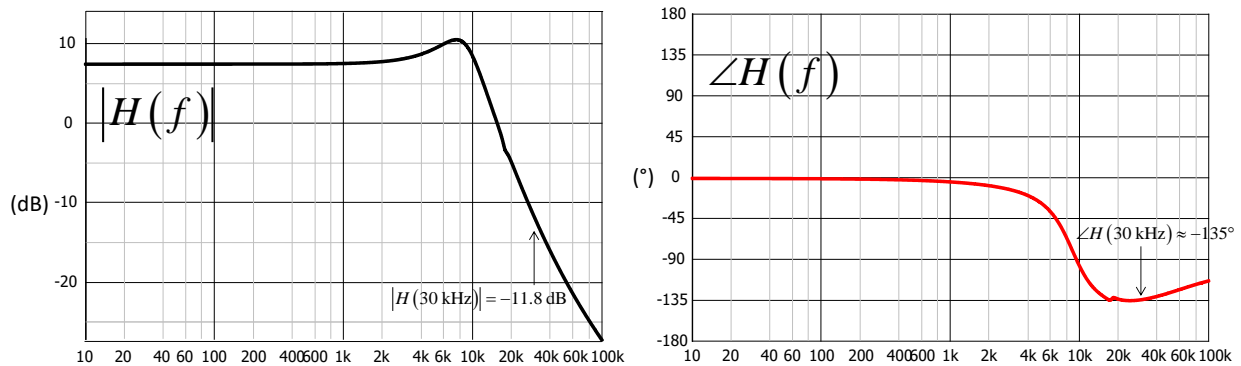


Fig. 8. The switching waveforms confirm the operating point while the small-signal response gives information we need for the stabilization process.

From these graphs, we can extract the following information: the magnitude attenuation at 30 kHz is around 11.8 dB while the phase lag at this frequency reaches 133°. Having these data on hand, the compensation strategy is carried out with the following procedure:

1. Place a double zero slightly below the output filter resonance calculated at to 8.7 kHz. Normally, if the converter transitions in DCM, you can place a zero at resonance and a second one lower. This ensures a

good phase margin in light-load conditions. In this example, the self-driven synchronous rectifiers will ensure CCM operation even at no load.

2. Place a pole f_{p2} at half the switching frequency or 250 kHz.
3. Evaluate the necessary boost in phase, given a phase margin target of 60°:^[6]

$$\text{boost} = \varphi_m - \arg H(f_c) - 90^\circ = 70 - (-103) - 90 \approx 105^\circ \quad (22)$$

This value confirms a type 3 is needed as a type 2 would be limited to 90° as a maximum value.

4. The compensator will cascade two zeroes and two poles. If we ignore the contribution of the pole at the origin, the phase boost produced by these poles/zeros pairs is

$$\text{boost} = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) + \tan^{-1}\left(\frac{f_c}{f_{z2}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p2}}\right) \quad (23)$$

The double zero is already fixed as well as the second pole f_{p2} . The angle of interest to determine the position of f_{p1} is:

$$\theta = \tan^{-1}\left(\frac{f_c}{f_{p1}}\right) = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) + \tan^{-1}\left(\frac{f_c}{f_{z2}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p2}}\right) - \text{boost} \quad (24)$$

Thus, we need to position the second pole so that our phase boost equals 105°:

$$f_{p1} = \frac{f_c}{\tan(\theta)} = 23.6 \text{ kHz} \quad (25)$$

5. The normalized component values computed by the Mathcad sheet^[2] give the following results: R_2 is 390 Ω (CTR = 1) while $C_1 = 100$ nF, $C_2 = 22$ nF, $R_3 = 27$ Ω and $C_3 = 22$ nF.

Crossing over at 30 kHz or so implies a fast op-amp whose own response will not affect the type-3 shape you intend to build. The paper in reference [10] explains how a poorly-selected op-amp can impact the final compensator performance, severely degrading the phase margin. In this example, we have chosen a TLV271 and the original type 3 phase and magnitude responses were not impacted by this circuit.

Also, pay attention to the optocoupler, which also impacts the compensator response. A PS2801 is a classic in these dc-dc converters. As aforementioned, the shunt-based feedback path imposes a reasonable collector current and fixes the emitter voltage, reproducing a cascode-like configuration: considering a near-constant V_{ce} voltage, the Miller effect is considerably reduced, naturally relegating the optocoupler pole to higher frequencies. However, at a 30-kHz crossover frequency, it can still potentially crop the expected phase margin and we have compensated its presence via a simple capacitor in parallel with R_{LED} in Fig. 6.

We can now plot the loop gain $T(s)$ and check what margins we have. Fig. 9 shows the loop gain plotted with Mathcad. It confirms our theoretical 30-kHz crossover frequency together with the expected 60° phase margin.

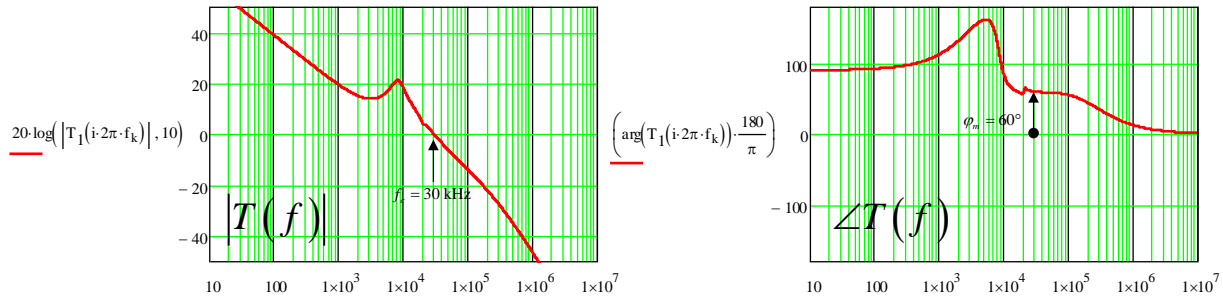


Fig. 9. The loop gain confirms the selected crossover frequency with the right phase margin.

The Final Circuit

Fig. 10 shows the primary-side schematic diagram while the secondary side appears in Fig. 11. The NCP1566 packs all the necessary features to build rugged and energy-efficient active-clamp converters.

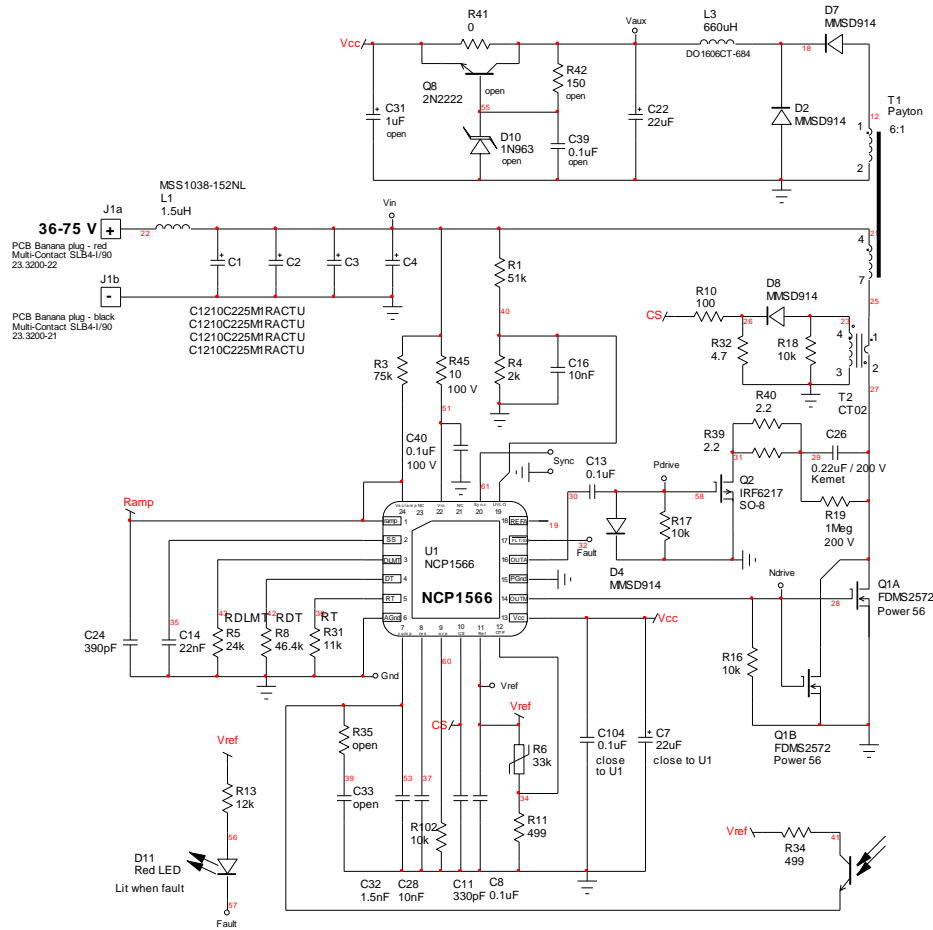


Fig. 10. In the ACF design example presented in this article, the primary side uses a controller specifically designed for active-clamp converters, the NCP1566.

The part includes various protections and an adaptive dead time, which improves efficiency as the circuit enters light-load operation. The startup sequence is ensured by an on-board high-voltage current source also

operating as a dynamic self-supply (DSS): in case the auxiliary winding takes time to supply the controller, the DSS provides energy to the IC until the auxiliary voltage builds up and turns the current source off.

When skipping cycles in light- or no-load conditions, the auxiliary winding is likely to collapse as a result of the very narrow pulses. The DSS will automatically activate in this mode, self-supplying the controller.

The power stage uses a planar transformer from Payton and feeds the output inductor through a pair of self-driven synchronous rectifiers. The active-clamp forward converter lends itself very well to driving these transistors directly considering an extended demagnetization cycle in the primary time: the drive voltage in the secondary side is present 100% during the off-time and ensures smooth operation for these voltage-controlled rectifiers. It is not the case with a classical forward where the V_{in} voltage disappears from the secondary side as soon as the primary inductance is demagnetized.

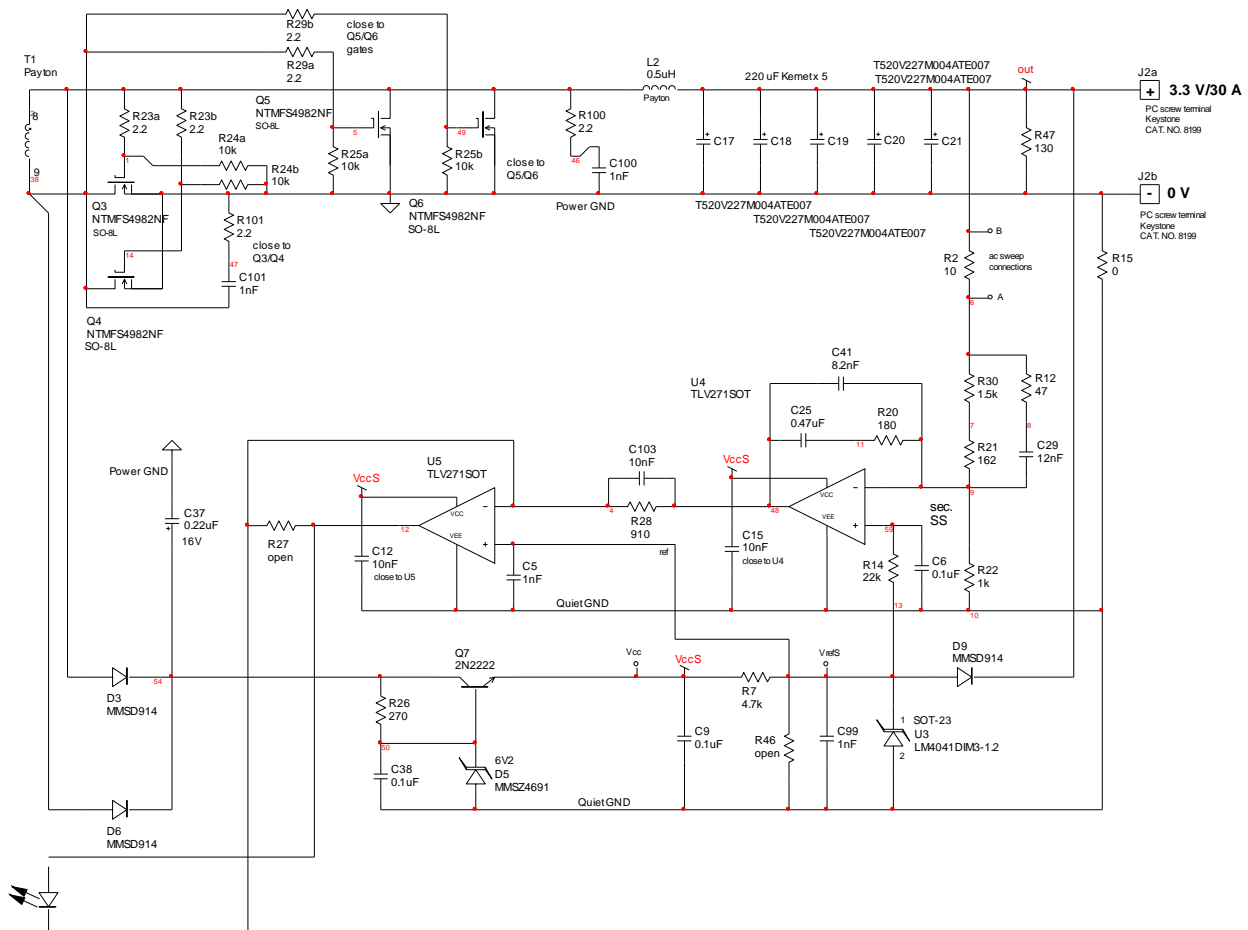


Fig. 11. The secondary side of the example ACF design implements two op-amps and a voltage reference.

The loop is built around two op-amps. The first one U_4 is used for the type 3 compensator while U_5 drives the LED, nicely suppressing the current interaction with V_{out} (no fast-lane issue). Please note that the compensation values are slightly different from the calculated ones and this is the difficulty associated with these dc-dc modules.

Our calculations deal with the small-signal response only and when component values were plugged into the converter, the loop was well stabilized as expected. However, what matters also with these converters is how V_{out} rises at power up. The rise must be monotonic, without double slope. This is a large-signal operation until V_{out} stabilizes to its regulated value. During this time, it is difficult to predict how the various capacitors will charge and how they will affect the output voltage rise.

One way to impose a monotonic start up is to soft-start the secondary-side reference voltage U_3 via R_{14} and C_6 . As soon as the converter starts, the auxiliary voltage across C_{37} quickly rises up (C_{37} needs to be a small capacitor) and, via the low voltage across C_6 , it forces op-amp U_4 to take the lead, forcing V_{out} to follow the exponential charge of C_6 .

In this case, the primary-side soft-start duration is reduced to limit the stress on the semiconductors but must be limited to this role otherwise the two soft-start processes (primary and secondary) may fight and distort the output voltage rise. A bit of adjustment is necessary there.

Loop Measurements

The circuit in Fig. 11 shows the presence of a 10- Ω resistance (R_2) in series with the upper resistance of the voltage sensing divider. This resistance maintains loop closure and does not affect regulation due to its low value. By connecting a transformer across this resistance as shown in Fig. 12, it is possible to obtain the open-loop transfer function of the converter without physically opening the loop. This technique was pioneered by Middlebrook in the 70s and is described in details in reference [11].

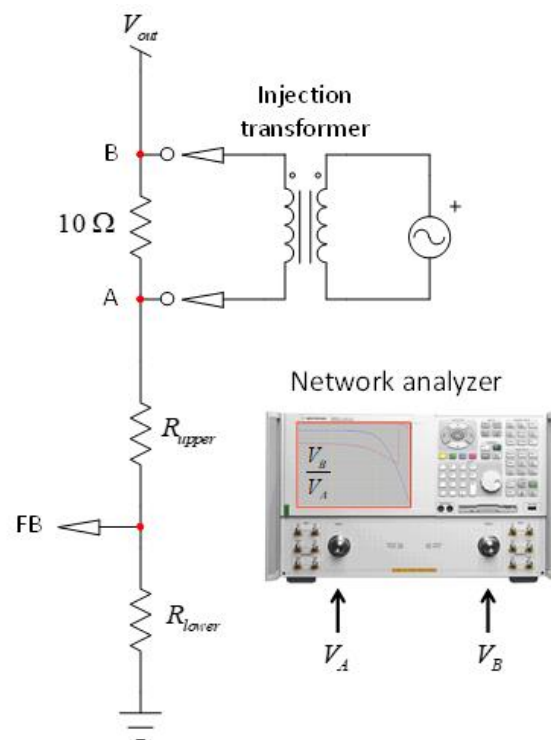


Fig. 12. The 10- Ω resistance lets you sweep the converter and obtain the transfer function of your choice.

I recommend including this resistance in the prototype stage with two simple hooks for connecting probes. When you deal with multilayer printed circuit boards populated with tiny components you can't really do a lot when the board is back from assembly. It is complicated and risky to cut traces to insert a small resistance and

later connect probes onto it. It is easier and more comfortable to include these extra pads during the layout stage.

To measure the loop, I have successfully tested the CS328A instrument manufactured by Cleverscope^[12] in New Zealand. The device packs a two-channel 14-bit oscilloscope and a frequency-response analyzer (FRA) for a very competitive price. No need to insert an isolation transformer as the CS328A embeds a solid-state injector and you simply connect the probes to the power supply.

The instrument first does a rough sweep and fine-tunes the injection level to maintain an adequate signal-to-noise ratio without affecting linearity. As the instrument permanently displays the observed waveform, you can immediately check if saturation occurs during the sweep. This is a cool feature which avoids connecting another oscilloscope to monitor ACF operation in parallel with the FRA.

The resulting sweep is given in Fig. 13 and shows the correct crossover frequency with a bit of phase distortion around it. Further analysis actually revealed that the front-end EMI filter was guilty of resonance around this point and needed adequate damping. Once done, the glitch disappears as expected.

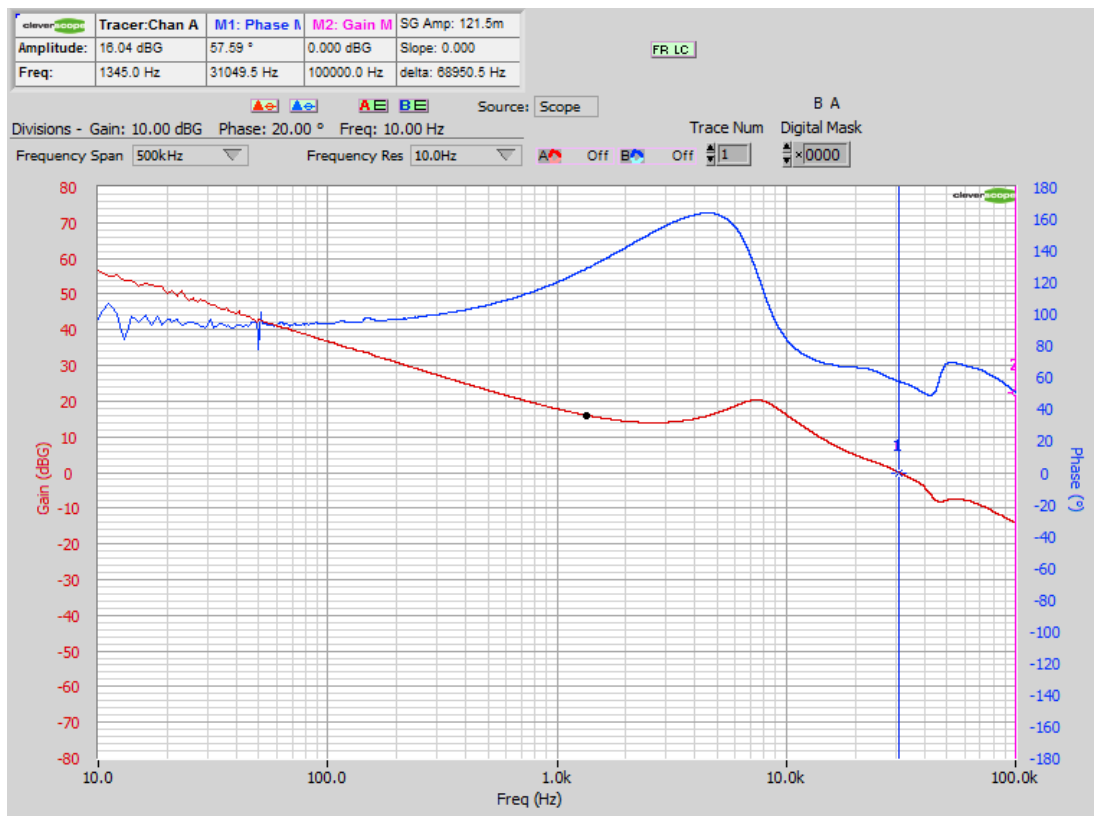


Fig. 13. The measurement confirms the 30-kHz crossover with adequate phase margin and shows a glitch induced by the front-end EMI filter.

Conclusion

This article described a possible compensation strategy for an active-clamp forward converter operated in voltage-mode control. Combining tools such as simulation and a mathematical solver is the best way to approach design and understand the role of each element. The compensation strategy will then be thought to compensate for component variability, later verified by bench measurements. Once the model is considered faithful to the hardware, sweeping these contributors in the simulation environment is mandatory to make sure they are well neutralized by the adopted compensation scheme.

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About The Author



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For further reading on power supply compensation, see the How2Power [Design Guide](#), and do a keyword search on "compensation."