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ECCE 2019 Plenary Explores Power Electronics On The Grid, 99% Power Efficiency And More

by David G. Morrison, Editor, How2Power.com

With the IEEE Energy Conversion Congress & Expo (ECCE 2019) just a little more than two months away, details of the extensive technical program are coming to light, starting with the plenary session. The plenary at this year's ECCE, which will be held Sept 29-October 3 at the Baltimore Convention Center in Baltimore, Maryland, will shine a light on developments in power electronics applications on the grid, in motor drives and in military systems. It will also present innovative ideas on more fundamental topics in power electronics such as co-design of power circuits and thermal management and the pursuit of ultra-high efficiency and power density.

Two of the three application-oriented talks will highlight the growing role of power electronics on the grid, while the other will discuss the use of new GaN devices in motor drives. Meanwhile, the talks on co-design and ultra-high efficiency explore areas that are expected to broadly impact the future of power electronics and electric machines. This article offers a preview of four of these talks and introduces the speakers.

"Integration Of Gallium Nitride In Power Applications: Achievements And Challenges"

Presented by Alain Charles, VP, Technology Development Center, Infineon Technologies America, El Segundo, Calif.

About The Talk

The U.S. Department of Energy has recognized the opportunity to dramatically reduce usage of electricity in homes and businesses through adoption of variable speed motor control. An estimated 535 x 1012 BTUs of energy could be saved annually in the U.S. through use of variable speed drives (VSDs) in home appliances and an additional 461 x 1012 BTUs when commercial appliances are considered. In total, this is the equivalent of reducing the annual release of greenhouse gases due to the usage of 5.5 million short tons of coal.

Today VSDs are inverterized based on state of the art (SOA) silicon-based power solutions using either six FREDFET power MOSFETs or six IGBT/FRD pairs together with a gate driver IC capable of driving all six switches as a voltage source.

However, a proposed concept is to leverage existing 600-V normally off (e-mode) CoolGaN switches for use in our VSD "power stages," which feature package integration of six GaN HEMTs. The reverse recovery performance of CoolGaN, provides substantial advantage in terms of turn-on loss at full and partial load, enabling >50% reduction in power loss. For successful adoption in motor control, three elements of a GaN-based solution are required:

- A low-cost driver IC which provides current source drive signal as the CoolGaN gate is current driven, and protection functions (to control slew rate to <5 V/ns). The IC must also cost no more than existing low-cost voltage source ICs used with silicon. This presentation will describe the proposed solution to realize this IC based on junction-isolated level-shifting technology.
- Cost-competitive GaN devices. For $R_{DS(ON)}$ values in the 1-Ω range, CoolGaN die are 5x to 6X times smaller than FREDFETs so that even with higher wafer cost per area the GaN die cost will be lower than silicon. On top of that, the lateral nature of the GaN device brings the potential further advantage of monolithically integrating the six GaN switches into one die. This presentation will show the challenge of doing so, due to the back gating of the high-side switch by the low-side switch and also the common silicon substrate. A proposed remedy to these challenges will be presented.
- A low-cost surface-mount package solution achieved through the simplification of the 12- x 12-mm QFN package due to the monolithically integrated GaN switches, which reduces the number of components in the package from seven (or 13 in the case of IGBTs) to two.

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About The Speaker

Alain Charles is a 30 years' semiconductor industry veteran. He received his Ph.D. in 1989 from the Institut National des Sciences Appliquées (INSA) de Toulouse (France) for his work on optical lithography for microelectronics.

Through his international career, Charles was involved in most of the key technology changes of the semiconductor industry, ranging from developments such as subwavelength pattern printing, to larger wafer (300-mm) technology development to power efficiency and introduction of wide-bandgap semiconductors.

His international career started in driving optical lithography efforts at Motorola's Mesa site (Arizona) and later ST Microelectronics' factory in Carrollton, Texas. He later joined the Motorola-Siemens Joint venture pioneering 300-mm silicon manufacturing in Dresden, Germany, and was part of the team that produced the first 64-Gbit DRAM on 300-mm wafers in 1998.

He then managed Fab5 and Fab3 engineering teams at Silicon Foundry Chartered Semiconductor (today Global Foundries) in Singapore. In 2003, Charles joined International Rectifier's power device technology development team in Newport (Wales, UK), which lead finally to his heading the silicon technology development team for all discrete power devices from company headquarters in El Segundo, California. After Infineon's acquisition of International Rectifier, Charles took the worldwide responsibility for the gallium nitride technology development initiative within the company.

"Emerging eT&D Grids: Energy Storage, Electrification, And The Increasing Role Of Power Electronics"

Presented by Babu Chalamala, Head of the Energy Storage Technology and Systems Department, Sandia National Laboratories, Albuquerque, NM

About The Talk

Emerging electronic transmission and distribution (eT&D) grids will evolve rapidly, accommodating the changes in generation mix and load profile that are associated with increasing renewable and distributed generation, electrification and bidirectional power flows. For eT&D grids to operate reliably with a high degree of autonomy, there is a greater need for energy storage systems and intelligent power conversion systems with advanced circuit topologies and high-speed communication infrastructure.

Current challenges for the future eT&D grids include limited scale of energy storage deployments along with low penetration of power electronics in the current grid infrastructure. As we look into a future with 70% to 80% renewables in the generation mix and higher amounts of dc loads including electric vehicles and appliances, the load profile and operational aspects of the grid will experience changes that are not well forecast. In this presentation, Chalamala will review the state of eT&D grid development, expected developmental pathways, and projections for the eT&D grid in the distant future.

About The Speaker

Babu Chalamala is head of the Energy Storage Technology and Systems Department and laboratory program manager for Grid Energy Storage at Sandia National Laboratories, Albuquerque, NM. Prior to joining Sandia in 2015, he spent twenty years in industry R&D, mostly recently as a corporate fellow at MEMC Electronic Materials/SunEdison where he led R&D and product development in grid scale energy storage. Before that, he was involved in two startup companies for eight years.

Chalamala spent the early part of his research career at Motorola and Texas Instruments where he made contributions to electronic materials and display technologies. He has a B.Tech. in Electronics and Communications Engineering from Sri Venkateswara University and a PhD in Physics from the University of North

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Texas. An IEEE Fellow, he served on the editorial boards of the Proceedings of the IEEE, IEEE Access and IEEE Journal of Display Technology. He currently serves on the as vice chair of IEEE PES Energy Storage and Stationary Battery Committee and as a member of the IEEE Fellow Committee.

Chalamala has also been active in the Materials Research Society, where he served as a general chair of the 2006 MRS Fall meeting. He currently serves on the MRS Government Affairs and Award Committees, and is author of over 120 papers, several edited volumes, and awarded 10 U.S. patents.

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"Co-Design: A Paradigm Shift to Enable Next-Generation Power Modules"

Presented by Lauren Boteler, U.S. Army Research Laboratory (ARL), Advanced Power Electronics Group

About The Talk

The Army is moving to a more-electrified force for an increasing number of applications including vehicles, renewables, tactical energy networks, communications, and weapons systems. Current power electronics devices are unable to realize their full potential due to the challenges of standard packaging including thermal dissipation, reliability, and parasitic inductance. As technology advances, the electrical, thermal, and reliability needs of these systems must be simultaneously accounted for due to the need for more power in smaller units with no loss in performance.

Unfortunately, most research has focused on solving only one technical challenge: a better heat sink, a better circuit design or a more reliable material. When thermal design is treated as a discrete step and not addressed until the end of development, systems become large, overly complex, and inefficient. This presentation will introduce the concept of co-design, a paradigm shift which moves away from the siloed approach to design and transitions into multi-disciplinary design to enable holistic improvement for next-generation power electronics.

The presentation will cover the current thermal and packaging challenges associated with power modules and will define the three key enabling capabilities to enable future power modules and next-generation cooling solutions: (1) parametric modeling tools, (2) additive manufacturing and (3) transient thermal mitigation.

About The Speaker

Lauren Boteler leads the thermal and packaging research programs as part of the Advanced Power Electronics group at the U.S. Army Research Laboratory (ARL). She received her PhD degree in mechanical engineering from the University of Maryland. Her work at ARL, beginning in 2005, has included electronics packaging and thermal management solutions for a wide range of Army applications.

Her focus is on design tool development and package integrated thermal solutions including 3D chip stacking, power electronics, laser diodes, double side cooling, and phase change materials. More recently, Boteler has initiated a research program in Advanced Power Electronics Packaging and Thermal Management which defined the four main challenges and opportunities of power electronics packaging: co-engineering/co-design, transient thermal mitigation, additive manufacturing, and high-voltage packaging.

Boteler is an adjunct professor at Johns Hopkins University and was awarded the 2018 ASME EPPD Woman Engineer of the Year award for her contributions to the electronics packaging community.

"Ultra High Power Density Demands 99% Efficiency and 99% Duty Ratio"

Presented by Don Tan, NGAS Distinguished Engineer and Power Products Manager at Northrop Grumman

About The Talk

Recent technology progress demonstrated effective ways of obtaining 99% power efficiency. The near adiabatic power conversion technology, for instance, needs no dedicated thermal management. Yet ultra-high power

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density has eluded many designs. The most recent technology trend in power conversion, particularly for dc-dc, suggests a significant increase in power density is within reach.

Ultra-high power density in commercial products demands a 99% efficiency and a virtual full duty ratio (say, 99%). The path forward requires a systematic approach in leveraging distributed low-profile packaging, minimum inductive storage, capacitive energy transfer, partial power processing, integrated WBG devices, modularity and scalability. It is anticipated that the power electronics industry will achieve an order of magnitude improvement in achievable power density within the coming years.

About The Speaker

Don Tan is NGAS Distinguished Engineer and Power Products Manager at Northrop Grumman. He earned his Ph.D. degree from Caltech and is an IEEE Fellow (since 2007).

Well-recognized as an authority in near adiabatic power conversion and energy systems, he has pioneered many breakthrough innovations with high-impact industry firsts and record performances. Tan's technologies have attracted significant customer funding and led to four product lines for the company and with hundreds of designs and thousands of delivered flight hardware that [are] "significantly enhancing national security".

Tan has given more than 50 keynotes and invited talks. He serves frequently on national and international funding, review, award, and prestigious position selection committees.

In the fifth talk in the plenary session, John Willison, executive deputy to the commanding general at RDECOM, will discuss "Power and Energy in Future Military Systems". More details will be provided on this talk as they become available.

For more information about the ECCE 2019 plenary session, contact the plenary session chair Issa Batarseh. For other information on the upcoming conference, see the ECCE 2019 website. And for general background on the conference and news about past and future ECCEs, see How2Power.com's ECCE section.

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