

## **Novel Switched-Capacitor Converter Supports 48-V Power Architecture In Data Centers**

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Adoption of 48-V main bus architectures is driving down operating costs for leading data center operators by reducing distribution losses by a factor of 16 compared to 12-V power delivery.<sup>[1]</sup> Building on this overall efficiency gain, engineers are fine-tuning down conversion topologies for board-level power delivery. The goal is to balance cost and efficiency as deployments scale to the level of 13 million new servers installed in data centers every year.

The principal driver in the evolution of 48-V power distribution in data centers is the overall power required to operate these massive server farms. Data center energy usage has increased at an average annual rate of 6% since 2006, according to the Electric Power Research Institute (EPRI). Because of this rapid increase, U.S. data center power demands are forecast to reach 73 billion kWh by 2020.<sup>[2]</sup> At the same time, the power demands of individual server racks are growing. As requirements per rack surpass 15 kW, the conduction losses of current across 12-V distribution architectures (which are four times the level of a 48-V bus) become unacceptable.

This move towards 48-V systems has triggered rapid innovation in the design of board-level power supplies. In March 2016, working through the Open Compute Project, Google released specifications for a high-efficiency direct conversion 48-V board for server racks.<sup>[3]</sup> A year later, at APEC 2017, Google described a two-stage solution with the switched-tank converter (STC), a transformer-less approach for conversion from 48 V to 12 V for distribution and voltage regulation (VR) at the point of load (POL).

Another example of innovation in this area is the zero-voltage-switching switched-capacitor converter, or ZSC, developed by Infineon (patented<sup>[4]</sup>). The operating principle of the ZSC topology is based on the Dickson charge pump; the voltage step down is achieved via capacitive energy transfer. It is a soft-switching approach that utilizes loop parasitic inductance with no saturation limit, rather than physical inductors, to achieve LC resonant operation with reduced inrush current during charge transfer. However, it does employ a single, small external inductor that carries a small ac current to support zero voltage turn-on, which yields a small physical design (Fig. 1). This article describes the principles of operation of the ZSC and offers tips for successfully implementing this topology.

### **ZSC Operation**

The ZSC is a resonant switch converter that is operated in an over-resonant fashion. The inductor and capacitor (L-C) networks generate current and voltage waveforms that vary in a sinusoidal manner in each switching period. Optimum efficiency occurs when the switching frequency matches the LC resonant frequency so that switching is both zero voltage and zero current. While a perfect match is impossible, the ZVS inductor compensates the mismatch to force the voltage to zero before each MOSFET switch is switched on.

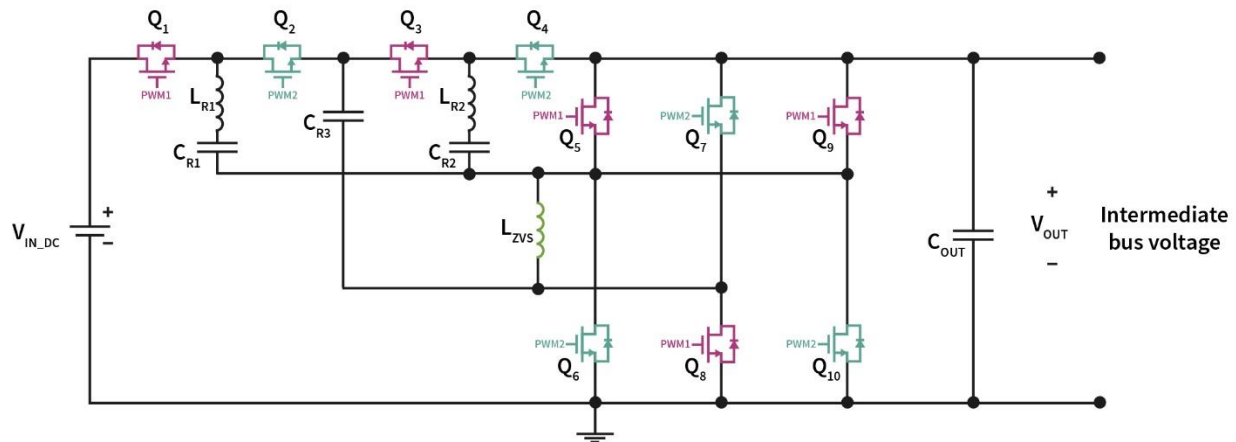


Fig. 1. ZSC schematic. The ZSC is a soft-switching converter that uses loop parasitic inductance, rather than physical inductors, to achieve LC resonant operation. But it does include a small inductor, which carries a small ac current, to support zero voltage turn-on.

In this scheme, the dominant contributors to loop inductance are the MOSFETs (specifically, the clips, bond wires, and lead frame of their packages) and capacitors. The PCB also contributes to inductance around the loop, though it has been observed that a  $\pm 50\%$  change in PCB inductance results in just a 0.22% impact on overall efficiency.

Because of the over-resonant operation and the addition of the ZVS inductor, perfect PCB layout is not required. However, for optimum efficiency, power shape routing should be robust to minimize  $I^2R$  losses while having small commutation loops to minimize ac losses. PCB design recommendations are available to guide the physical design process to ensure peak performance.

The company offers several different evaluation boards with ZSC reference designs of differing power levels and space requirements. The 1-kW design occupies an area of 650 mm<sup>2</sup>, while the space-saving 350-W design occupies just 357 mm<sup>2</sup> and has a width of just 7 mm. For all designs, the FETs are placed on the top layer, while driver ICs are placed on the bottom layer. Resonant and flying capacitors are populated on both layers. The ZVS inductor can be placed top or bottom for maximum flexibility.

In general, board design considerations for the ZSC should include:

- Via-on-pad is preferred if it is supported in manufacturing, using vias optimized for high power
- Gate-drive signal routing should not break any power plane, with gate and source traces routed differentially
- I/O voltage levels are stabilized by placing decoupling capacitors as close as possible to ICs.
- Total trace width calculation, depending on the current level, should be equalized for all resonant and flying cap tanks.

Additional optimizations to reduce PCB losses in a high-current design include a high number of vias (16 for MOSFET drain and eight for the source) and four vias per capacitor terminal. Vias should not be placed too close together, as this close proximity can form a barrier that blocks return currents on the GND layer.

Lab tests of a 4-to-1 configured board, driven by 54-V input to generate 13.5 V to the intermediate bus, show impressive performance. The inductor  $L_{ZVS}$  assures zero-voltage switching of all of the MOSFETs under all conditions. Hence, this topology offers extremely high efficiency across the entire load range (98.4% at 250 W and 96.5% at 1 kW) as seen in Fig. 2.

**Infineon's ZSC topology (54 → 13.5 V)**

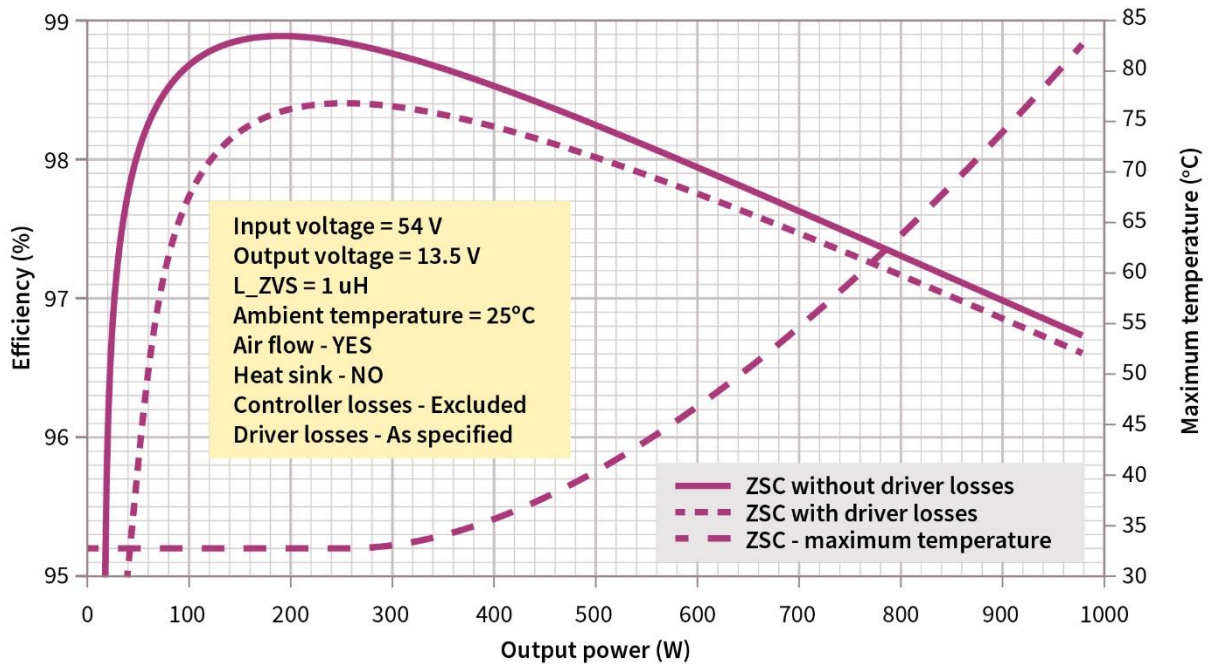


Fig. 2. ZSC efficiency curve for a design that steps down 54 V to 13.5 V.

With the ZVS inductor guaranteeing zero voltage switching, efficiency is very high as shown in Fig. 2. The ZVS inductor in conjunction with the over-resonant operation allows production designs to use standard tolerance capacitors. Utilizing the PCB loop inductance for  $L_{R1}$  and  $L_{R2}$  also helps to improve the power density of this solution due to the elimination of ac and dc resistance losses associated with physical inductors.

An end-to-end (54 V to 13.5 V to 1.8 V) downconverter evaluation design combines the ZSC eval board with a second-stage multiphase buck regulator (Fig. 3). Production-grade designs of this solution achieve greater than 94% efficiency across the 150-W to 300-W output power range and remain above 90% through 600 W.

Since the soft-charging topology of the board is naturally bidirectional, the converter design can easily be adapted for boost operation from 12 V to 48 V, with no modifications to the ZSC components or microcontroller required. The only change needed is the addition of an E fuse on the 12-V input to limit inrush current to the repurposed design, which reaches efficiency levels of 98% in the medium output range (Fig. 4). The E fuse also provides enable and disable functions.

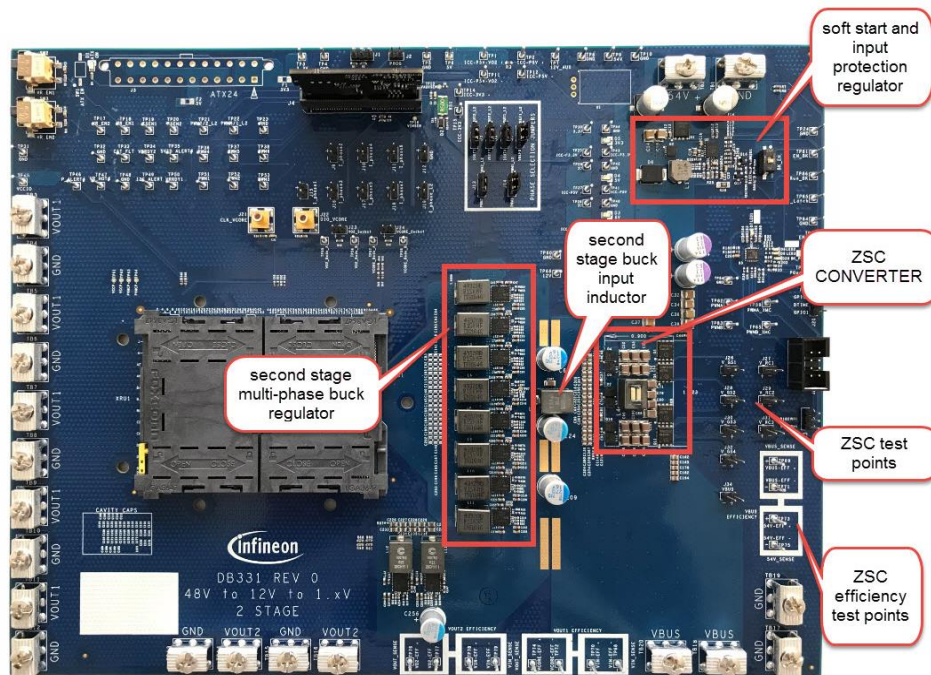


Fig. 3. The DB331 eval board implements a reference design for a two-stage power converter that steps down 54 V to 1.8 V. The first stage ZSC is followed by a multiphase buck converter.

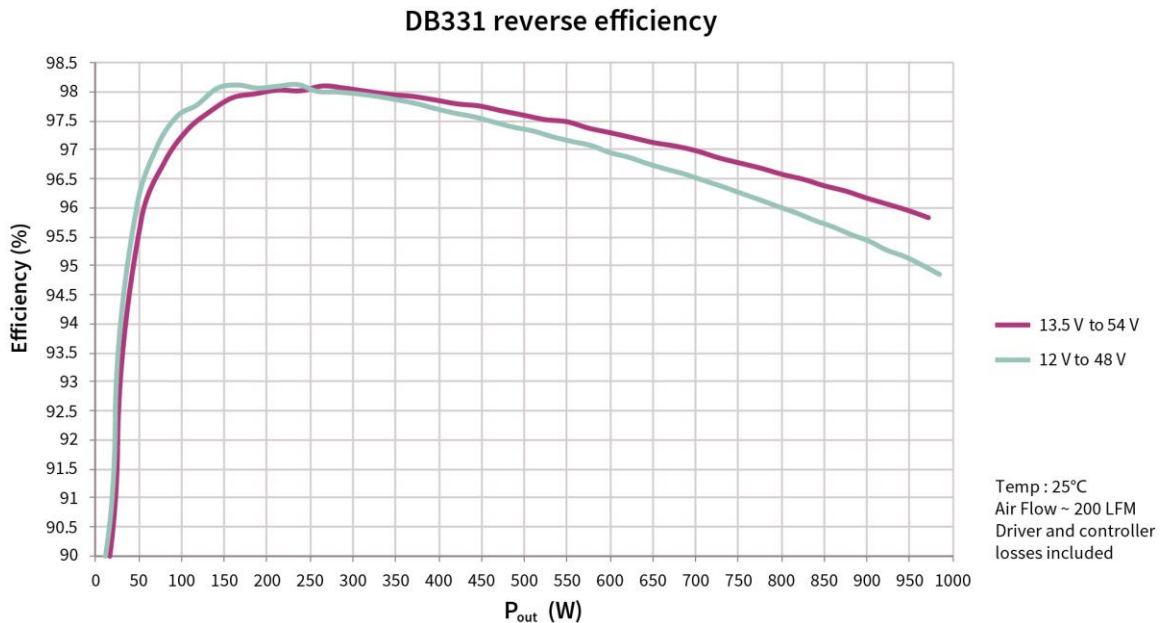


Fig. 4. Reverse efficiency curve for the DB351 bidirectional eval board. Because the topology is bidirectional, the ZSC can be operated as a boost converter and achieves efficiency that is comparable to operation in the stepdown mode.

The ZSC board can be implemented as a voltage regulator module (VRM) or down (VRD) design depending on system requirements and limitations. It can be configured to accommodate different conversion ratios (2:1, 4:1, 6:1, 8:1, 10:1 or 12:1) by adjusting the number of FETs in the design. In addition, because the impedance of the converter is very low, it lends itself to parallel operation naturally.

While the main processor on the board may be operating at around 1 V, there are many other components within the same board that require different voltage inputs. Because of its flexibility and configurability, the ZSC can be tailored to provide power to the entire board.

In a typical 4:1 setup, the ZSC converts 48 V down to 12 V, where it can be further bucked down to around 1 V. However, not all boards are set up in this style, and the flexibility of ZSC to operate in different ratios as mentioned above is useful in other designs as well. Much smaller 2:1 ZSC converters with smaller POL solutions can also be placed throughout the board to generate the desired output voltage.

To tackle I<sup>2</sup>R distribution losses on large PCBs, a smaller 2:1 converter can be placed on the input bus to reduce the power distributed throughout the board to 24 V. Near the XPU core power, another small 2:1 converter can be used to generate the 12-V input required for multiphase products. This flexibility is not provided by module-based solutions, which only focus on the main processor power.

Future iterations that are likely to further improve efficiency will see the integration of MOSFET or driver stages. Each successive improvement of 0.1% to 0.3% percent will aid data center operators in their quest to lower operating costs through efficient computing and concurrent reduction in building heat loads. The ZSC board is available upon request and more information is available online.<sup>[5]</sup>

## References

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3. "[Google Contributes 48V DC Data Center Rack to Open Compute](#)," Data Center Knowledge, March 9, 2016.
4. "[Method and apparatus for zero-current switching control in switched-capacitor converters](#)," U.S. patent no. 10,122,256, Babazadeh et al., November 6, 2018.
5. [Infineon's 48 V Ecosystem for Data Centers](#).

## About The Author



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*For more information on power converter design for the data center, see the How2Power [Design Guide](#), locate the Application category and select "Data Centers". Also, locate the Power Supply Function category and select "DC-DC converters."*