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How To Drive Rad Hard E-Mode GaN Transistors Efficiently And Safely

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A portfolio of high reliability, radiation hardened (rad hard) eGaN HEMT devices represents an exciting development for the space circuit design community. These transistors offer the designer a vastly improved C_{iss} * $R_{DS(ON)}$ figure-of-merit (FOM) as well as much faster switching times when compared to conventional rad hard silicon MOSFETs.

Naturally being a newer technology, there are potential interface-related questions about the technology. In particular, designers new to the application of rad hard eGaN HEMT transistors typically want to understand how to deal with the narrower gate-source voltage operating range of the eGaN HEMTs as compared to that of the familiar silicon MOSFETs.

For example, all available die and discrete-packaged Freebird Semiconductor eGaN HEMT devices have a usable gate voltage range of +6 V to -4 V, with +5 V being the optimum desired on-state drive level. This compares to the ±20-V range, and a +12-V optimum on-state drive level, for a conventional rad hard, non-logic-level silicon MOSFET.

For a space-level application design, there are additional complications. One is the need to balance service life environments, with such considerations as the fact that full enhancement of the eGaN HEMT device (and the corresponding maximum current-carrying operating point) is not reliably achieved until a minimum gate-source potential of approximately +4.2 V is reached.

Additionally, many designers design to a typical data sheet transfer curve in regard to V_{gs} versus I_d. However this practice discounts the effects of aging, radiation, temperature, processing, device parameter variations such as changes in transconductance, and the operating stresses presented to the device during its lifetime in the required spaceborne environment. Therefore, all the factors that influence the choice of the correct gate-source voltage in a space application need to be understood by the designer.

In this article, we explain why the 4.2-V gate-drive level is recommended for optimum efficiency of rad hard eGaN HEMTs, and why the 6-V absolute maximum should not be exceeded. Next we discuss how device packaging and the source-sense connection help to manage switching transients at the gate terminal.

We continue this discussion by explaining and simulating the effects of device characteristics and pc-board parasitics on these transients, demonstrating the effects of loop inductance on the overshoot seen at device turn-on and the use of damping resistance to limit this overshoot. The impact of device characteristics and pc board parasitics on device turn-off are also discussed and demonstrated including the effect of the Miller capacitance. The reason for using different internal values of pull-up and pull-down resistance within the e-GaN HEMT is explained.

Within this discussion, we offer tips on selection of the damping resistance value, sizing of the source sense connection and other layout considerations.

The Right Gate-Source Voltage

Typical data sheet parametric guidelines demonstrate an eGaN HEMT saturation at ~3.5 V of gate-source drive. Given that, you might ask "So why does Freebird recommend a 4.2-V drive, minimum?"

The reason for the higher guideline level is based on the need to satisfy requirements within the high-reliability spaceborne environment. Driving our technology under recommended guidelines will ensure end-use designers obtain the maximum benefit in their application for both the performance and reliability of the device. Freebird Semiconductor considers our eGaN HEMT devices to be power switches and we do not recommend linear mode operation.

Our years of experience in the high-reliability eGaN HEMT radiation hardness arena mandates such a conservative approach to driving gates, eliminating any potential for not *effectively* saturating the device. Such conditions would cause a loss of efficiency in the application due to the resulting $\Delta R_{DS(ON)}$ increase over life, etc. We therefore highly recommend that any half-measures of gate drive are abandoned in favor of the level that will give the best chance of a long-term successful application outcome.

A reasonable designer might ask, "What about the losses incurred by the gate at the higher V_{gs} operating point?" We'll answer this with a design example.

Consider the power dissipation at again say, 4.2 V and a gate leakage current of 1 mA. This is 4.2 mW of power dissipation. One must also consider the additional ac losses due to the greater voltage level (from 3.5 V) or $P_{GATE(AC)} = C_{iss} * (4.2^2 - 3.5^2) * f_s$. If we assume the device operates at 1 MHz, this loss is $1000 * 10^{-12} * 5.39 * 10^6$ for a typical device, or a 5.4 mW. So the combined differential loss at a V_{gs} of 4.2 V, assuming no dc gate loss at 3.5 V, is 9.6 mW.

Now consider that the HEMT operating at a V_{gs} of 3.5 V might have an $R_{DS(ON)}$ that varies 1 to 2 mΩ over its operating life, etc. at that operating point. The losses incurred for such a deviation are proportional to $Id^2 * \Delta R_{DS(ON)}$.

So what happens if this same device is operating at a drain current of 10 A with the 2-mΩ incremental increase in on-resistance? The result will be a 200 mW increase in the device's power dissipation just from this "under-drive" situation alone, or an over 20 times increase in power dissipation versus just increasing the gate drive potential to 4.2 V. Weighing the consequences, moving to the 4.2-V drive level (despite the *now-antiquated strictures* to "properly de-rate") is a no-brainer!

Now, the flip side of the minimum gate-drive requirement is the absolute maximum gate-drive potential. As was previously mentioned, Freebird Semiconductor specifies our absolute maximum gate-source voltage as +6.0 Vdc to ensure long-term high-reliability operation. The reason is that it is essential to not exceed the maximum (or minimum) gate-source voltage because potential damage may be done to the gate over time by the associated voltage overstress.

While it is tempting to think that this maximum voltage restriction can be explained by the breakdown characteristic of the gate-source junction, as shown in Fig. 1, the reason is not that simple. Fig. 1 shows the gate-source current (I_{gss}) for the various Freebird discrete product offerings for different V_{ds} breakdown voltages. Although an eGAN HEMT may be destroyed by dissipating excessive power in a single catastrophic overvoltage event (the gate-source junction may be thought of as a voltage-offset metal-semiconductor junction), irreparable damage to the gate structure of an eGAN HEMT is typically done by repeated voltage overstresses.

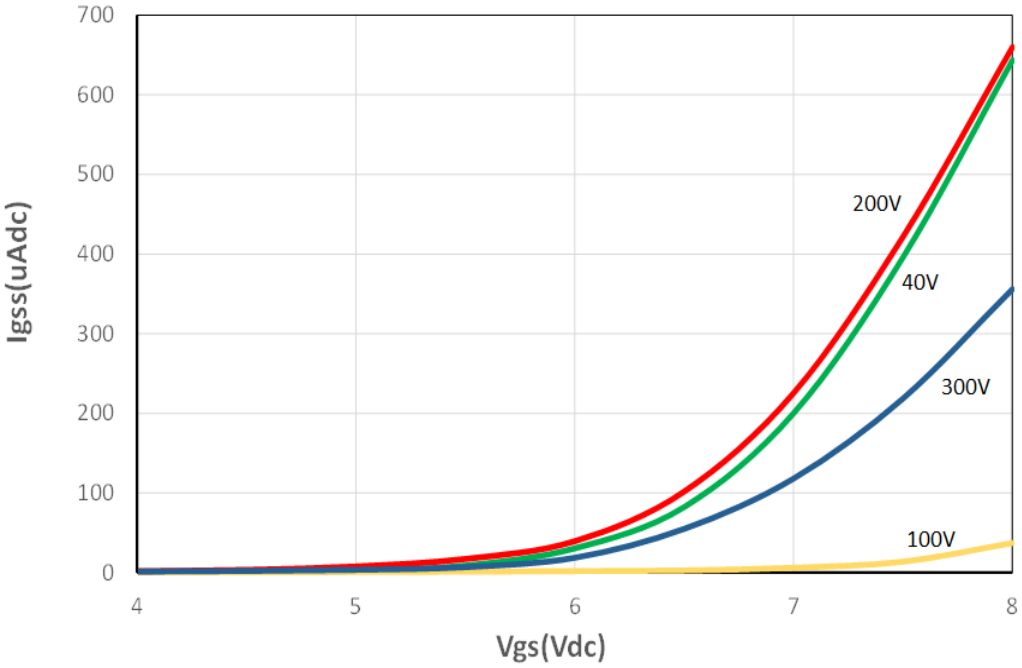


Fig. 1. A typical Freebird eGAN HEMT gate-source forward breakdown characteristic plotted at various V_{ds} breakdown voltage levels.

Excursions in gate voltage beyond the +6-V rating will cause increasingly larger currents to be drawn by the gate, depending on the device characteristics. This destructive process occurs as a result of the energy supplied to the gate by the uncontrolled transient. The point at which each device will fail due to overvoltage insult to the gate will depend on the physical size of the die (determining the thermal resistance), the internal gate series resistance and any minor imperfections in the gate-source/drain structure. Of course, the magnitude, frequency, duration and total number of insults also will influence the likelihood and timing of a failure.

The repeated voltage overstress events essentially damage the gate structure in a "death by a thousand cuts" manner. Eventually, because of this increased current drawn by the gate, the gate will experience what amounts to a death spiral of increasing gate current along with the excessive gate-related power dissipation, and the HEMT will catastrophically fail.

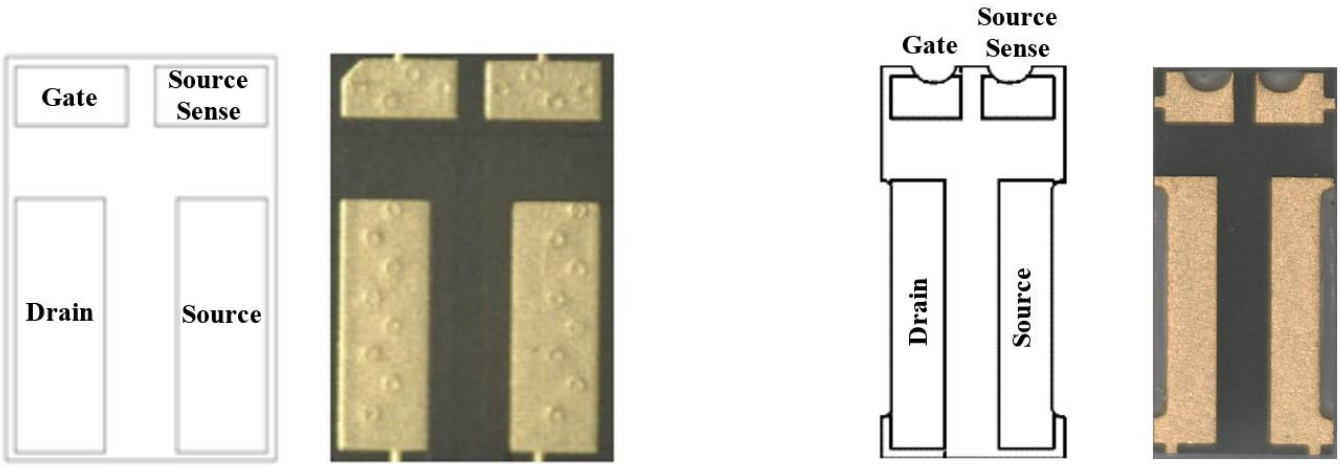
Consequently, it may seem like the designer does not have much room for error in applying and properly driving HEMT devices! However, device packaging and a careful design approach *eliminate* all these gate-drive concerns.

The Essential Source-Sense Connection

The sensitivity of the eGAN HEMT to gate-source overvoltages requires that the designer be mindful of the accuracy/tolerance of the bias level of the power supply that powers the gate driver. The designer *must* additionally ensure that under all transient switching conditions the gate-source potential is never allowed to exceed +6 V peak during switching transients. To this end, the packaging for the Freebird discrete eGAN HEMT and die products have been optimized to assist the designer in minimizing ringing and other transients due to gate/drain current interactions resulting from parasitic inductances.

For example, the I/O pads on the Freebird FSMD-B SMT package are shown in Fig. 2a and on the FDA1 die adapter package in Fig. 2b. Each Freebird SMT or die adapter package provides four separate I/O pad connections to the eGAN HEMT within: gate, source sense, drain and source.

The source sense pad adjacent to the gate pad enables the designer to optimize the gate-drive loop independently of the high-current drain-source output loop, as shown in Fig. 3b. The source sense pad is connected directly to the source on the die *internal to the package*—making it a true Kelvin connection and thus eliminating deleterious load current and gate current interactions. Internal to the package the source and source sense pads have the same reference potential, that of the source of the internal eGAN HEMT transistor.



(a) *(b)*

Fig. 2. Freebird Discrete eGaN HEMT packaging. Bottom views are shown for the company's FSMD-B package (a) and FDA1 package (b).

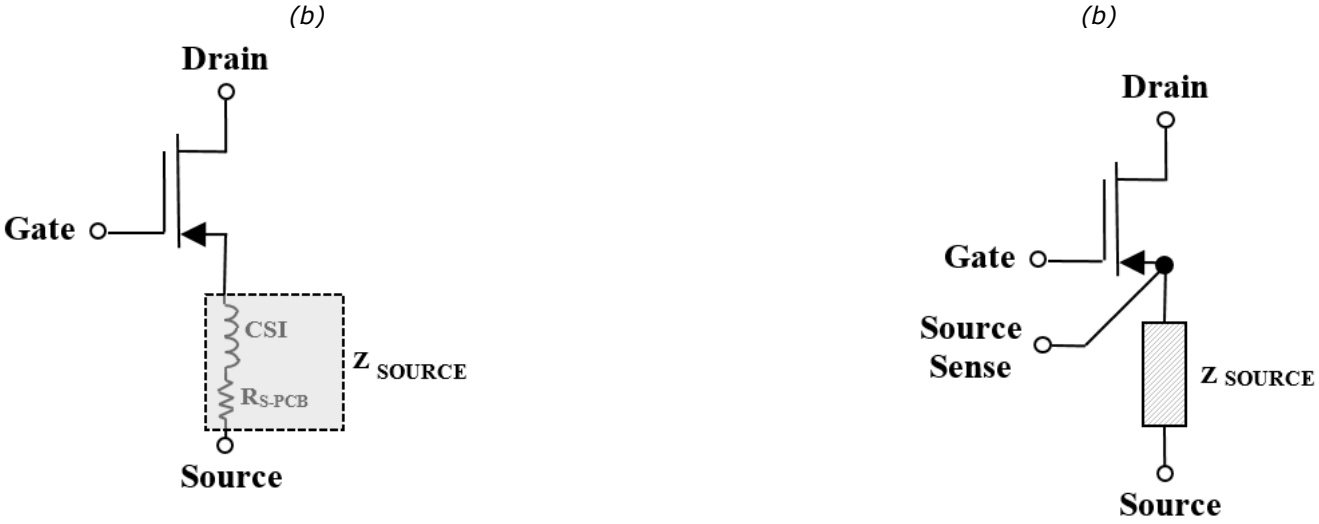


Fig 3. A Freebird source sense connection. A HEMT is shown schematically without (a) and with (b) the source sense connection.

An immediate benefit to the designer is that the high-current, high-di/dt drain current cannot influence the transient-sensitive gate current loop due to external (to the package) parasitic inductances and resistances in series with the high-current source terminal (Z_{source} in Fig. 3a.). During current commutation, common power source inductance (CSI) is separated from gate return. This prevents the voltage induced by dI_d/dt across the power source inductance from being subtracted (added) from (to) the gate-drive voltage during turn-on (off), as shown in Fig. 3a.

Even for very small parasitic inductances, those induced voltages may be high due to the very fast switching times of the eGaN HEMTs. Source inductance common to the gate drive and power loops (common source inductance or CSI) is a major contributor to losses and erratic operation during current commutation.

Turning The E-Mode GaN HEMT On And OFF

However, just providing the source sense pad on the Freebird SMT packages is not enough to prevent harmful transient voltages from appearing at the gate terminal of the HEMT device. The most important consideration for reducing or eliminating voltage overshoot in the gate current loop during device turn-on is to reduce the parasitic inductance in the gate current loop that will affect the gate turn-on current, $I_{g(on)}$, shown by the green arrows in Fig. 4.

The total loop area of this high transient current path determines, in large part, the parasitic inductance present in this current loop. In the equivalent turn-on circuit in Fig. 4b, it can be clearly seen that the gate driver pull-up resistance (R_{Dpu}) and the HEMT gate resistance (R_G), the loop inductance (L_{LAY}) and the input capacitance (C_{iss}) form a series R-L-C resonant circuit. In the equivalent circuit, R_{Dpu} is the pull-up resistance of the gate driver, R_G is the internal gate resistance of the HEMT and C_{iss} the gate-source input capacitance of the HEMT.

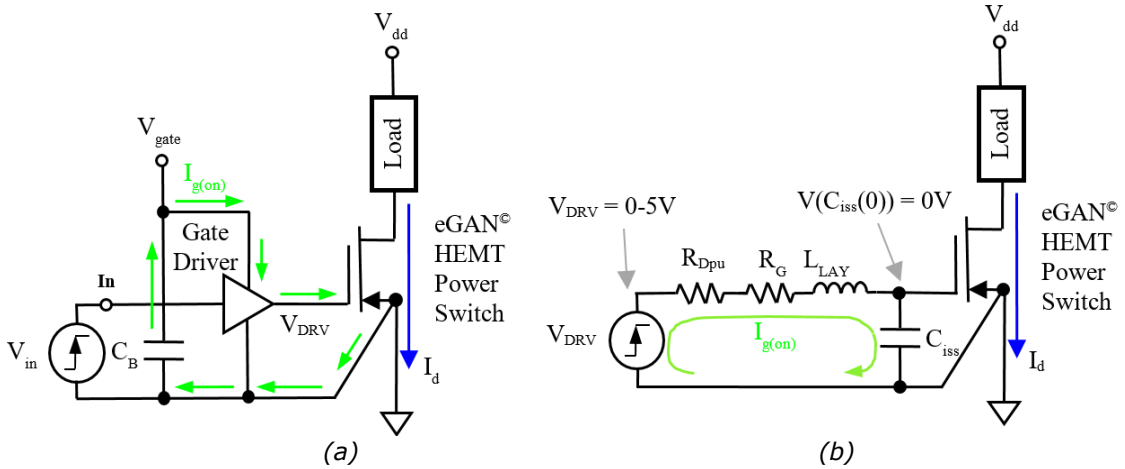


Fig 4. An eGaN HEMT at turn-on. Current flow is shown for HEMT and gate driver (a) and the equivalent circuit including parasitic elements (b).

The quantities/parameters R_{Dpu}, R_G and C_{iss} are all fixed for a given circuit design and the components selected. They are data sheet parameters for the HEMT and the gate driver, so the principal goal for the designer is therefore to keep L_{LAYOUT} as small as possible by making the connections from the output of the gate driver to the HEMT gate, from the power input of the gate driver to the gate driver power supply bypass capacitor (C_B) and from the source sense pad to the power supply bypass capacitor as short as possible. And, if possible, route the gate drive and return paths on separate board layers over each other to cancel inductances.

It is recommended that the source sense connection in the gate loop be implemented as a small copper etch area on the PCB, and not just an etch trace. This implementation mimics, on a smaller scale, the properties of a ground plane. The gate power supply bypass capacitor should be located and connected directly across the power supply and ground pins of the gate driver IC—or as close as possible to the high-current driver elements of a discrete gate driver circuit.

The connection from the output of the gate driver should be as short as practically possible. The width of this connection should be at least one-half of the length in order to minimize unwanted parasitic/passive elements.

In practice, it is nearly impossible to reduce the loop area enough to prevent unwanted loop inductance. This might happen because of proximity limitations due to component sizes or printed circuit board mechanical restrictions, or simply because of parasitic inductances, mostly wire bonds) in component packages.

Fig. 5 shows the PSPICE simulation output for the gate-source voltage of an FBG10N30B eGaN HEMT (R_G = 0.6 Ω and C_{iss} = 700 pF) with a gate-driver pull-up resistance of 2 Ω and with series inductance values (L_{LAY} in Fig. 4b.) ranging from 1 nH to 20 nH in 1-nH steps. It is clear that for series inductance values up to approximately 7.5 nH, the gate voltage does not exceed the absolute maximum value of +6 V. A close-up of the gate-source voltage for inductance values up to 7.5 nH is shown in Fig. 6, proving that the gate-source voltage does not exceed +6 V.

Now, for the larger values of series inductance unavoidably present in the gate circuit, all is not lost, as the designer has a valuable option to reduce the magnitude of the parasitic resonance peak voltage: damping resistance. This damping resistance (R_D) should be placed in series with the output of the gate driver and the HEMT gate. The total series resistance in the gate circuit then becomes R_{Dpu} + R_G + R_D.

For example, Fig. 7 shows the gate voltage simulation results for the full 1- to 20-nH range of series inductance values with an added damping resistance value of 2 Ω. It can be seen in Fig. 7 that even up to the maximum 20-nH inductance level, the gate-source voltage does not exceed the +6-V maximum rating of the device. These results demonstrate the value and effectiveness of the judiciously-chosen, added gate-damping resistance.

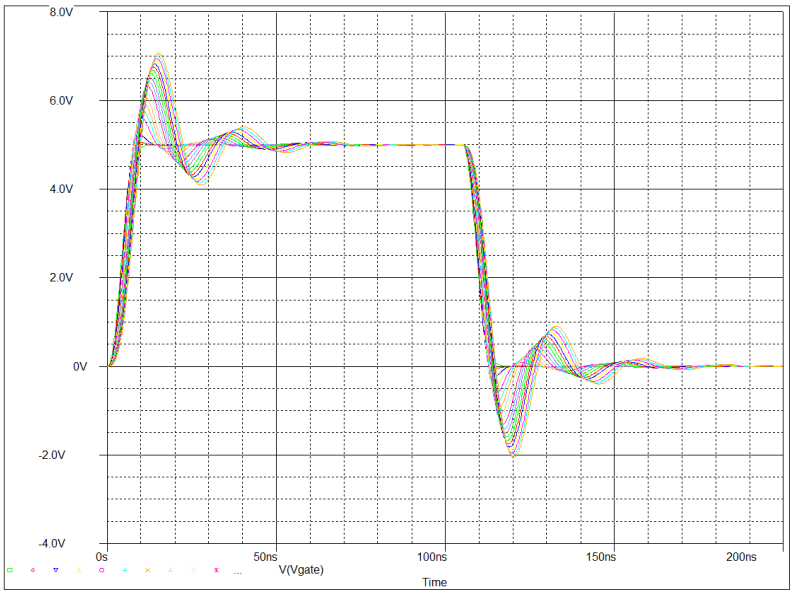


Fig. 5. Gate-source voltage simulation of a Freebird eGaN HEMT with series inductance varied from 1 nH to 20 nH.

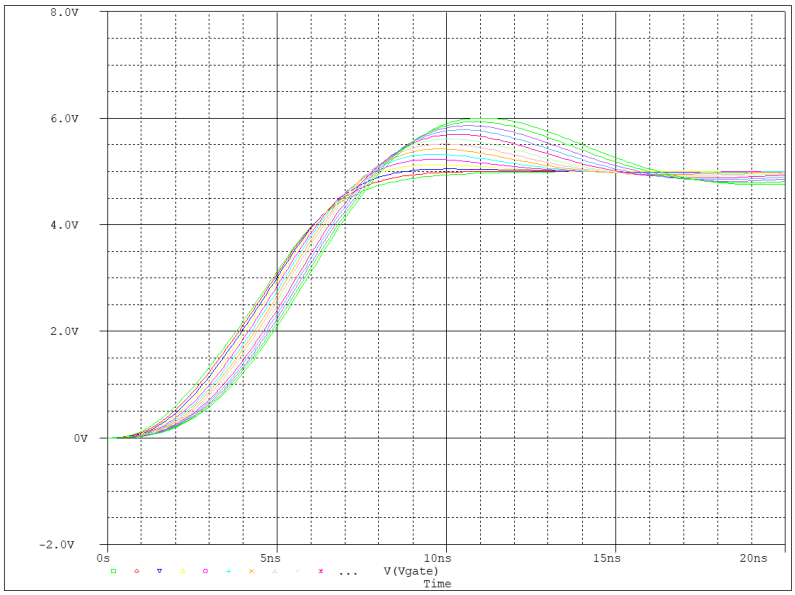


Fig. 6. Gate-source voltage simulation of a Freebird eGaN HEMT with series inductance varied from 1 nH to 7.5 nH. (Time scale is adjusted for a close-up view of device turn-on.).

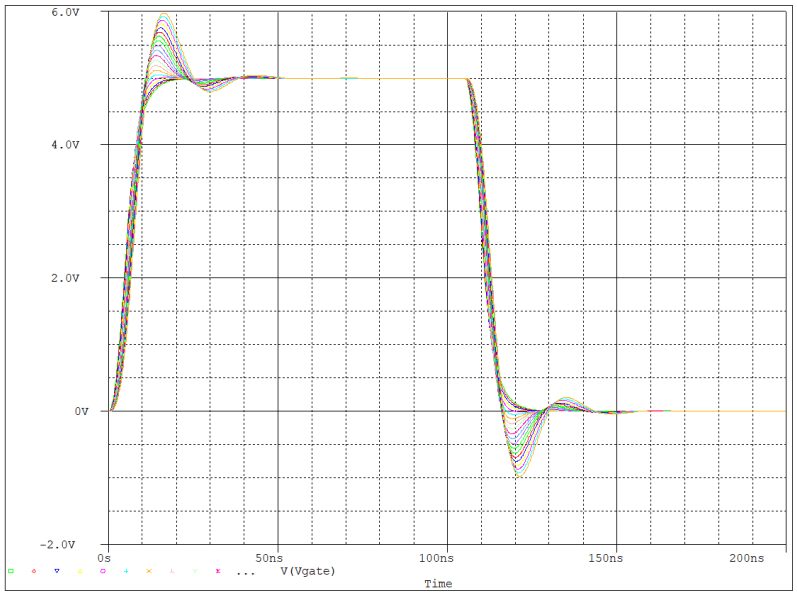


Fig. 7. Gate-source voltage simulation of a Freebird eGaN HEMT with series inductance varied from 1 nH to 20 nH, again, but with a 2-Ω damping resistance added.

Caution must be exercised in applying the damping resistance as when the value is increased, the peak available gate current is limited, and the rise and fall times of the gate voltage are increased. The net effect is to decrease the overall performance of the circuit. For example, the conversion efficiency in a power supply will be lower.

So, the designer must keep the damping resistance to the lowest reasonable value that balances the gate switching performance desired and the maximum peak gate voltage allowed or desired. If an integrated or

discrete driver is used that has separate gate pull-up and pull-down outputs, it is recommended that the damping resistance be utilized in the gate pull-up output only, as ratings-threatening overshoots in gate voltage will be encountered only during the turn-on event.

This implementation allows the switching performance of the eGaN HEMT to be maximized in that the performance of the turn-on loop is only, necessarily, affected by the required damping. Meanwhile, the turn-off loop remains optimized to pull the gate to the source with the lowest resistance possible, thus providing for the fastest gate turn-off time possible.

The turn-off circuit for the eGaN HEMT is shown in Fig. 8. It is similar to the turn-on circuit shown in Fig. 4 with the exception that the gate-driver output resistance is R_{Dpd}—the driver pull-down resistance.

For integrated gate drivers, the pull-up and pull-down resistances are often different, with the pull-down resistance lower than the pull-up resistance. This will not be a problem in terms of the peak transient undershoot of the gate-source voltage at turn-off because the voltage margin from 0 V (the final gate turn-off potential) to the absolute maximum value of -4 V is four times that of the margin between the optimum gate drive voltage (+5 V) and the absolute maximum rating of +6 V, or 1-V margin.

Also, the lower pull-down resistance value helps to ensure that the HEMT gate will remain below the gate-source threshold voltage ($V_{gs(th)}$) even with the effects of the Miller capacitance (C_{rss}) accounted for. Although the rate-of-change of drain voltage can be considerable (for example 100 V in 10 ns for the FBG10N30, or 10,000 V/µs), the value of C_{rss} for the eGaN HEMTs is small in comparison to conventional MOSFETs (for the FBG10N30, C_{iss} = 30 pF).

For example, Fig. 9 shows the PSPICE simulation for the equivalent circuit shown in Fig. 8b for an FBG10N30 with a pull-down resistance of 2 Ω, no damping resistance and the layout inductance L_{LAY} varied from 1 nH to 20 nH.

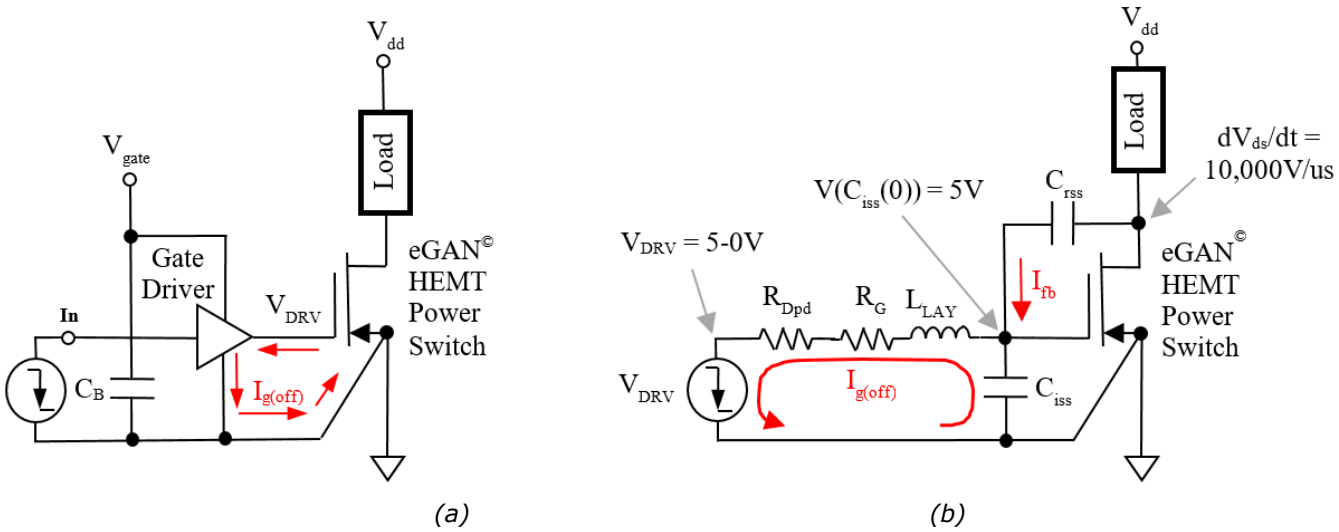


Fig. 8. An eGaN HEMT at turn-off. Current flow is shown for HEMT and gate driver (a) and the equivalent circuit including parasitic elements (b).

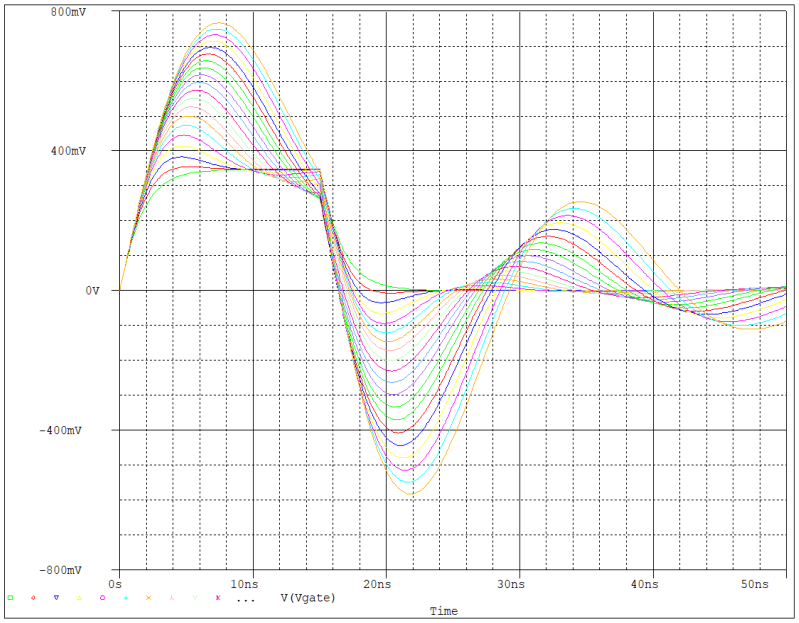


Fig. 9. Gate-source voltage simulation of a Freebird eGaN HEMT with series inductance varied from 1 nH to 20 nH, again, but with Miller feedback included.

It can be seen that for all values of inductance that gate-source voltage remains below the minimum gate-source voltage threshold for the FBG10N30 of 0.8 V. However, this is the 25ºC value, and at a 125ºC junction temperature the $V_{gs(th)}$ is 0.7 V, so gate-source voltage exceeds the minimum $V_{gs(th)}$ value for the three highest values of L_{LAY}, and there is a risk of transient dynamic turn-on at the HEMT turn-off event.

In practice, this would not be a significant issue because at HEMT turn-off, the bypass capacitor (C_B) is excluded from the circuit, and this component carries with it a not inconsiderable inductance due to its physical side/length. Thus L_{LAY} during turn-off will be less that at turn-on due to the exclusion of C_B from the circuit.

Conclusion

Freebird Semiconductor's eGaN rad hard HEMTs represent a leap forward in electrical performance over conventional silicon rad hard MOSFETs. Recognizing and accommodating the devices' ratings, particularly those relating to the gate-source input, will allow the designer to extract and enjoy all the benefits that these high-performance transistors offer.

Also, acknowledging that these transistors are not the same as silicon MOSFETs is key to realizing the performance increases that HEMTs can provide versus MOSFETs. This is not unlike the situation when silicon MOSFETs were first introduced, and it was necessary to recognize how they differed from silicon bipolar transistors. The guidelines provided in this discussion allow the circuit designer to implement Freebird eGaN HEMTs both efficiently and reliably, the most important criteria for space product design within a spaceborne radiation effects arena.

About The Authors

Jim Larrauri is chief strategy officer, executive director and co-founder of Freebird Semiconductor. Larrauri has 30 years' experience in the space-level high-reliability industry where he has worked in applications engineering, and strategic product and business development. He has expertise in a number of areas including open architecture VME, power semiconductors, power hybrids and radiation effects. He is currently advancing wide-bandgap high electron mobility gallium nitride (GaN) materials at Freebird Semiconductor as co-inventor and patent holder to a multi-function power control circuit using enhancement mode GaN high electron mobility

transistors (HEMTs) patent # 10,122,274.

For more information on designing with GaN power semiconductors, see How2Power's Design Guide, locate the Popular Topics category and select "Silicon Carbide and Gallium Nitride". Also, see How2Power's special section on SiC & GaN for more information. For more on rad hard power components, see How2Power's special section on Space Power.