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Matching Driver IC And FETs Bring GaN Benefits To Low-Voltage POL Converters

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There are two well known advantages of using higher switching frequencies (>1 MHz) in lower voltage (12 V to 1 V) point-of-load (POL) dc-dc converters. First, the inductors are smaller, both in physical size and inductance value for the same level of ripple current when compared to lower frequency operation. Secondly, less capacitance is needed in the output filter for the same output voltage ripple. A less discussed advantage is the potential for increased control loop bandwidth, which results in lower output capacitance to meet voltage excursion requirements during fast load transients. These benefits can't be obtained using silicon MOSFETs without sacrificing efficiency. However, due to the recent advent of low-voltage GaN FETs and matching drivers, giving up efficiency is no longer necessary.

This article will demonstrate the performance improvements that can be obtained when using GaN FETs in combination with suitable GaN FET drivers in 12-V input to 1-V output point-of-load converters. The example design described here uses the uP1966D, a dual-channel, synchronous driver IC from uPI Semiconductor in combination with an EPC2100 GaN asymmetrical half-bridge FET from Efficient Power Conversion.

In discussing the performance of this GaN-based point-of-load converter design, the focus will be on its efficiency in comparison with a conventional silicon-based solution. Although GaN-based point-of-load designs have been documented in the literature, most GaN applications to date have been at 48 V and above. The EPC2100 represents the first in a series of new GaN devices at low voltages with a matching driver that allows 12-V to 1-V (or 1.8-V) point-of-load conversion at high frequency with high efficiency. The article begins with a description of the driver.

Driver Features And Performance

The driver consists of a "floating" driver powered from a bootstrap circuit for a "high-side" GaN device and a ground-referenced driver for a "low-side" device. This driver has a maximum input voltage rating of 40 V. For higher-voltage applications, such as 48-V input dc-dc converters, the uP1966D has a sister device, the uP1966B, that has an 80-V rating. Fig. 1 below is a simplified block diagram of the uP1966D and uP1966B. In addition to their use in dc-dc converters the uP1966D and uP1966B also find use in switching audio amplifiers.

Another feature of the uPI1966D is its ability to adjust the time that both GaN devices are off (deadtime) by a selection of resistor values at the DTL (*d*eadtime *t*ransition *l*ow) and DTH (*d*eadtime *t*ransition *h*igh) pins. This driver also has the ability to control rise and fall times of both GaN FETs by selecting series resistor values between UGH, UGL, LGL, and LGH and GaN FET gates. The PWM input, which is tri-state capable, and can accept both 3.3-V and 5-V input levels, controls the switching action of the GaN FETs.

With the PWM input in the tri-state mode, both GaN FETs stop switching. The PWM input can accept narrow input pulses (<30 ns) and maintain proper high-side and low-side drive capability of the GaN FETs with no cross-conduction currents. Pulse widths below 5 ns will not result in any drive pulses to the GaN devices. The uP1966D also has an undervoltage lockout circuit on the Vcc input to prevent impaired switching of the GaN devices. A 5-V bias supply is the only drive rail required.

Typical Applications

In Fig. 2 we show the schematic of our application test board. It consists of a tri-state input buffer U2, which is used to test the tri-state function of the uP1966D driver. The buffer output drives the input of the uP1966D, which then drives an EPC2100 GaN asymmetrical half-bridge FET. The FET synchronously switches Vin to L1 or L2, depending on board stuffing options.

Diode D1 is a "catch" diode that freewheels the inductor current during deadtimes. This Schottky diode has a much lower forward voltage than the internal diode of the GaN device and can help improve efficiency. The diode is not always necessary.

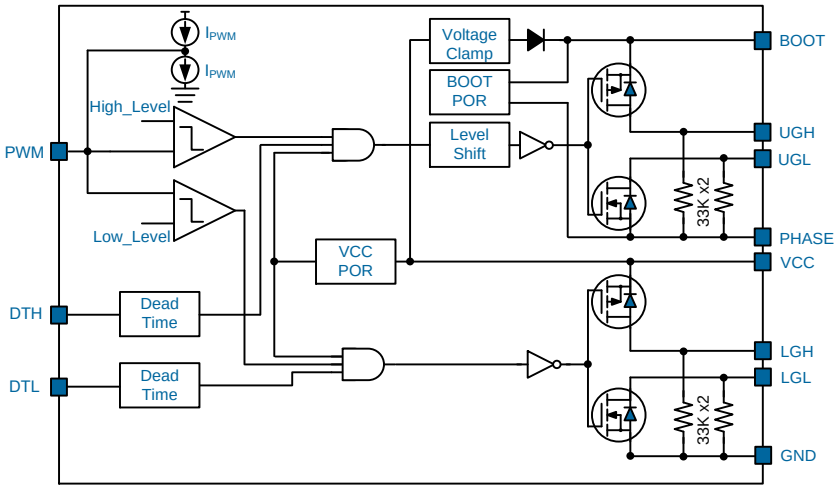


Fig. 1. Simplified block diagram of the uP1966D and uP1966B dual-channel, synchronous driver ICs. The uP1966D is housed in a 1.6-mm x 1.6-mm wafer-level chipscale package, making it likely the smallest of its kind on the market.

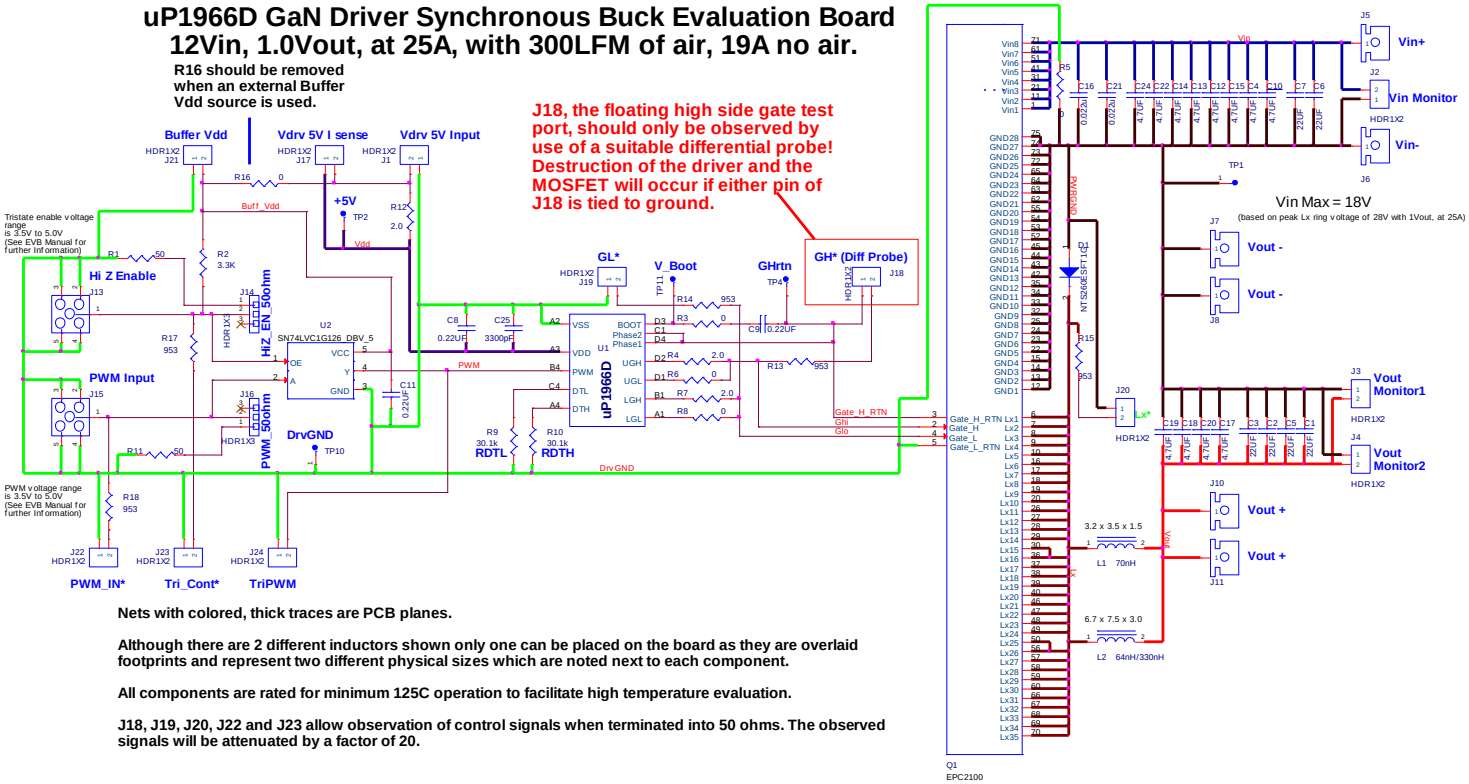


Fig. 2. The two-pin 0.1-in. headers, J18, J19, J20, J22, and J23, are used in conjunction with a two-pin header to BNC with a 50-Ω cable terminated into 50-Ω input on a 1-GHz or greater bandwidth oscilloscope to observe signals at these circuit nodes. A minimum bandwidth requirement of 700 MHz is required for accurate observation of these signals.

Circuit Description

The circuit above in Fig. 2 utilizes a tri-state buffer, U2, so that the user can observe the transitions in and out of tri-state from an external signal source. Allowances have been made for the use of an independent external power rail, through J21, for just the buffer to test the tri-state input levels.

The output of the tri-state buffer is fed to the PWM input of U1, the uP1966D, which in turn drives the gates of Q1, the GaN asymmetrical half-bridge FET EPC2100.

There are three sets of input capacitors on the main power input at J2 and J6. The first set of 22-µF capacitors is for bulk decoupling, the second set of 4.7-µF capacitors is to create a low-Z source for the GaN FET power loop, and the 0.022-µF capacitors are for high-frequency bypass to lower EMI at switching transients.

L1 and L2 are the output filter inductors. These are arranged as a dual footprint in the layout so that different size inductors can be evaluated. L1 and L2 combine with 4.7-µF and 22-µF output capacitors to make up the output filter.

Components related to the driver, including the GaN asymmetrical half-bridge FET, must be mounted on the same layer as the driver, if possible. RDTL and RDTH may be moved to the opposite side of the board when required but should return directly to the driver's ground pin through vias. The following components C_Vcc, HFCap, RBoot, and CBoot, should be placed with minimum inductance and on the same side of the board as the driver IC. Note that the DRVGND net is only tied to the GaN FET in one place (see Fig. 3).

When these layout guidelines are used, the GaN FET can switch at sub-nanosecond speeds as can be observed below in Fig. 4.

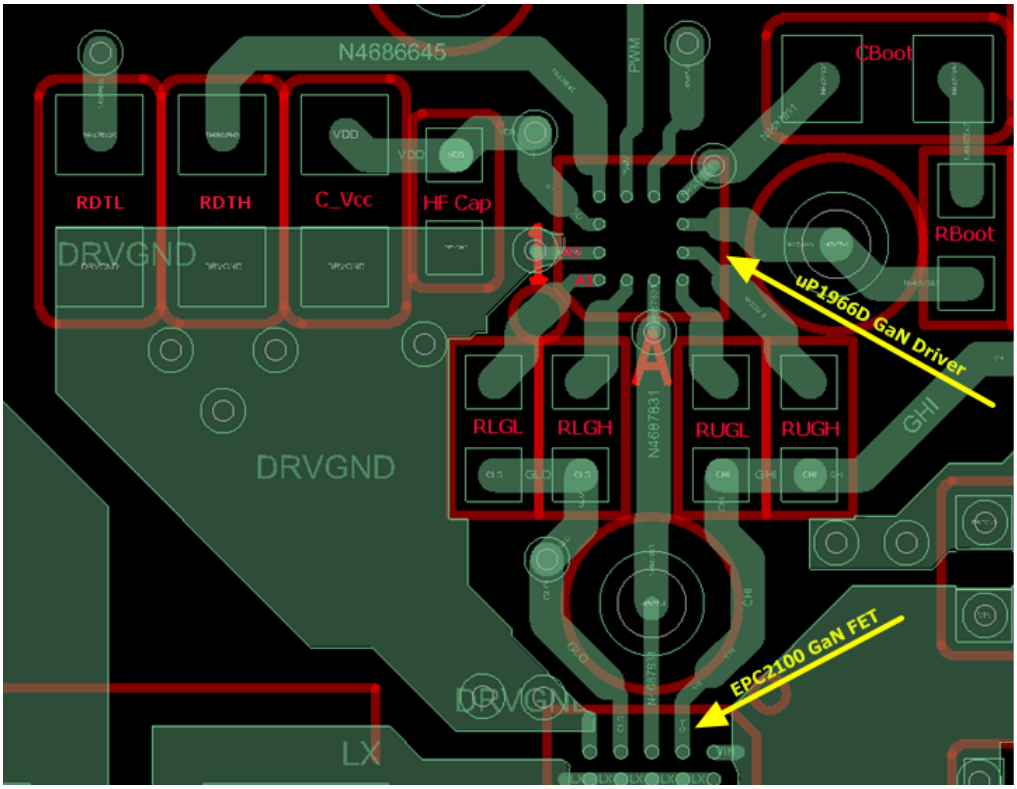


Fig. 3. PCB layout example of uP1966D GaN driver and EPC2100 GaN FET, designed according to optimal layout technique.(see the reference)

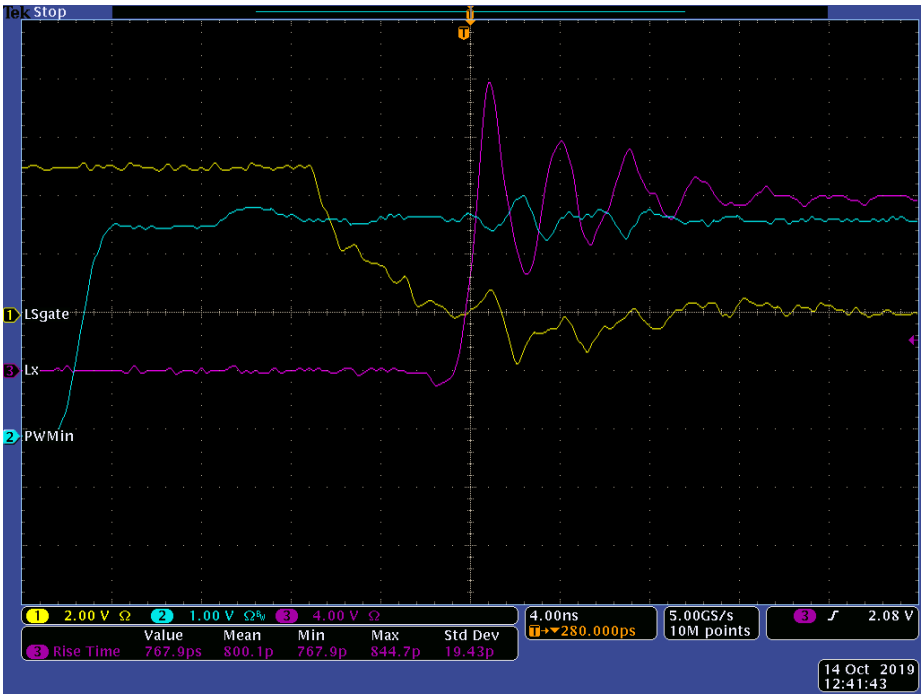


Fig. 4. Switching waveforms of the gate-driver input, output, and GaN FET drain-to-source voltage.

Performance

The driver will operate with GaN devices over a wide application range. Fig. 5 provides some examples at different switching frequencies over a 20-A load range.

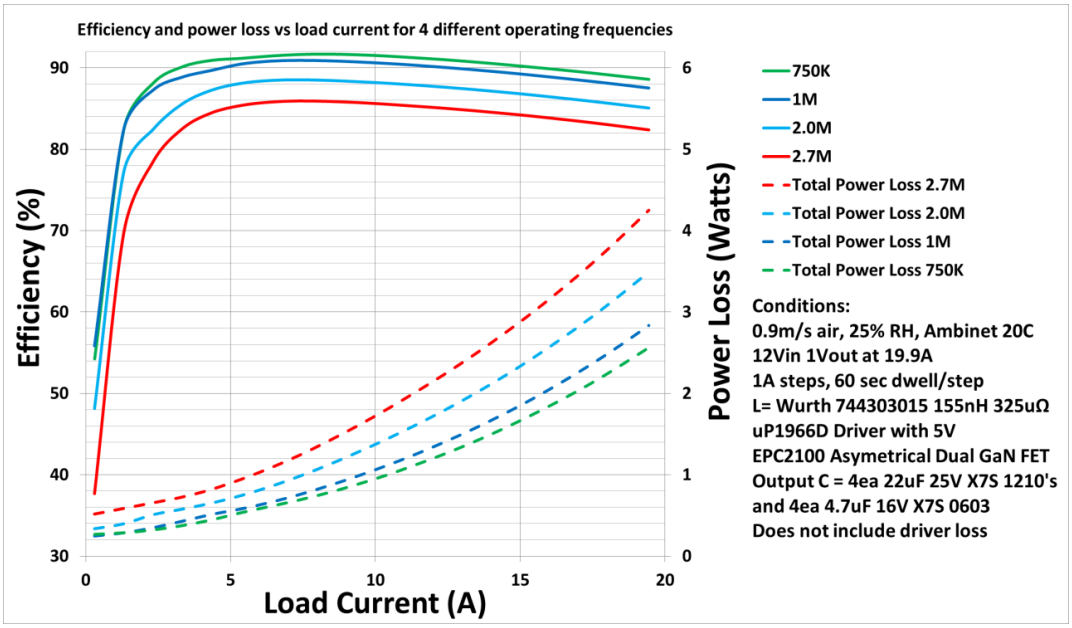


Fig. 5. Efficiency and power loss with load, over frequency of operation, at 12-V in, 1-V out.

Comparison With MOSFET Performance

A 4.5-mm x 3.5-mm DrMOS product is used for comparison with GaN performance in Fig. 6. The GaN solution is superior in both efficiency and power loss at twice the operating frequency of the DrMOS solution in this 12-V to 1-V application. The test set-up used to make these dc measurements is shown in Fig. 7. The test set-up used to make ac measurements and for thermal testing is shown in Fig. 8.

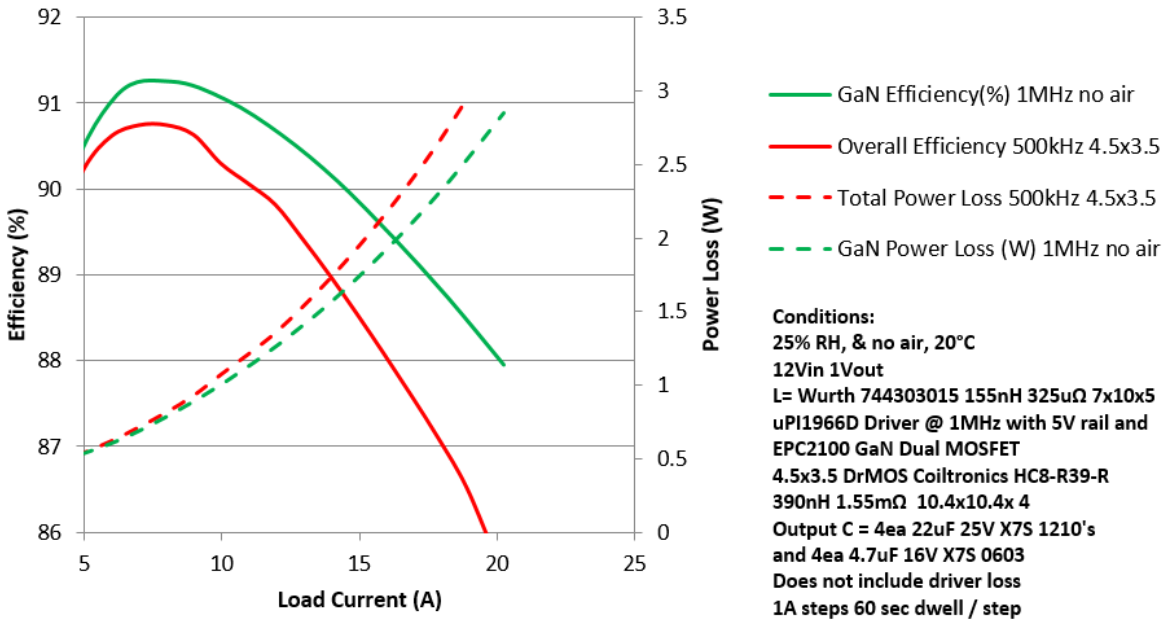


Fig. 6. Comparing 4.5-mm x 3.55-mm DrMOS efficiency at 500 kHz versus a uP1966D driving an EPC2100 GaN FET half-bridge at 1 MHz for 12-V input and 1-V output.

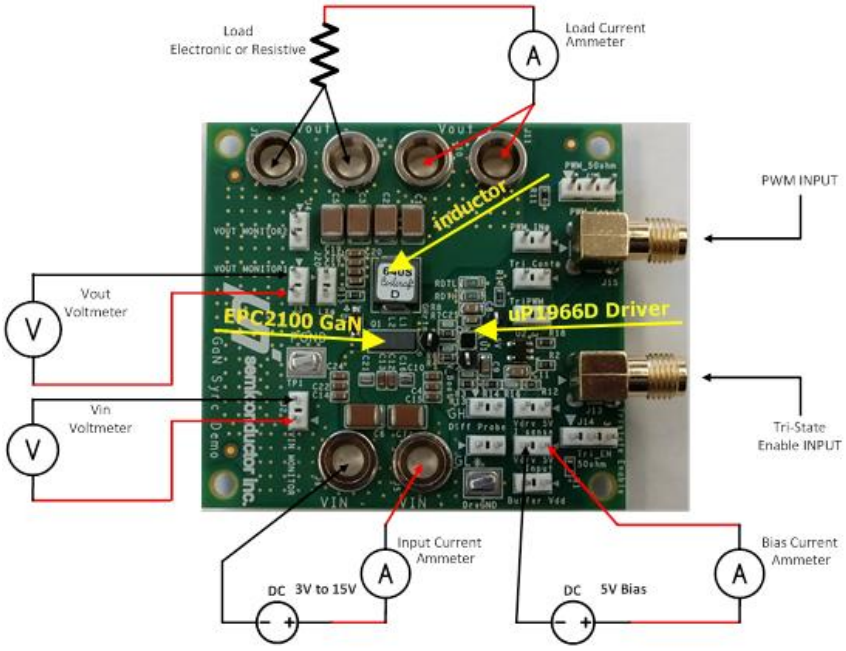


Fig. 7. Typical test set-up for dc tests. Note the small size of the components in the power stage.

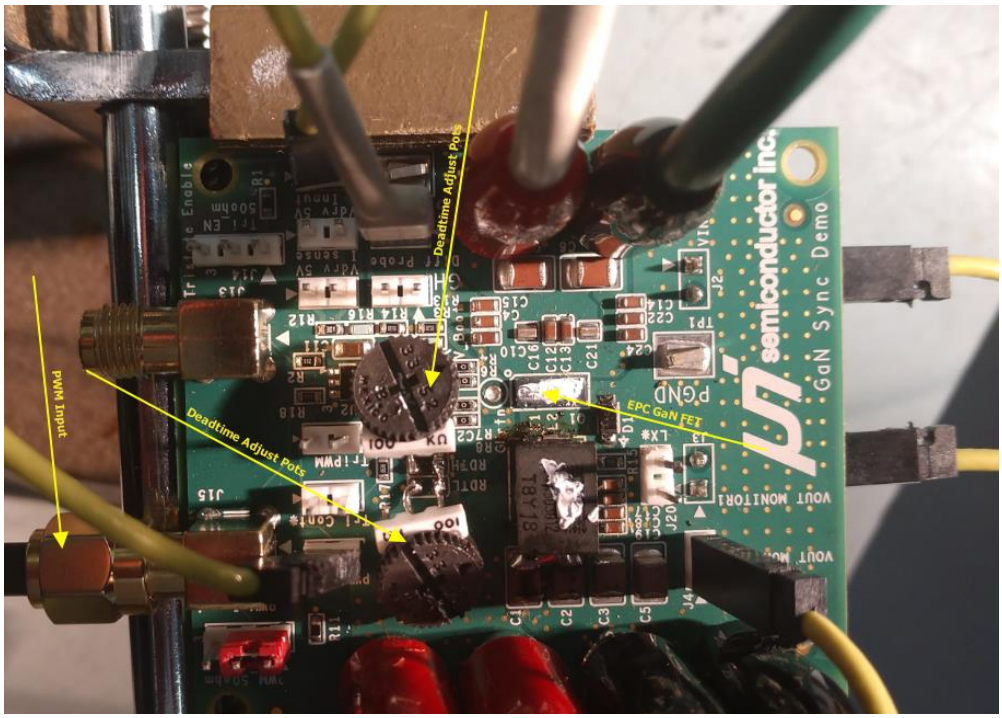
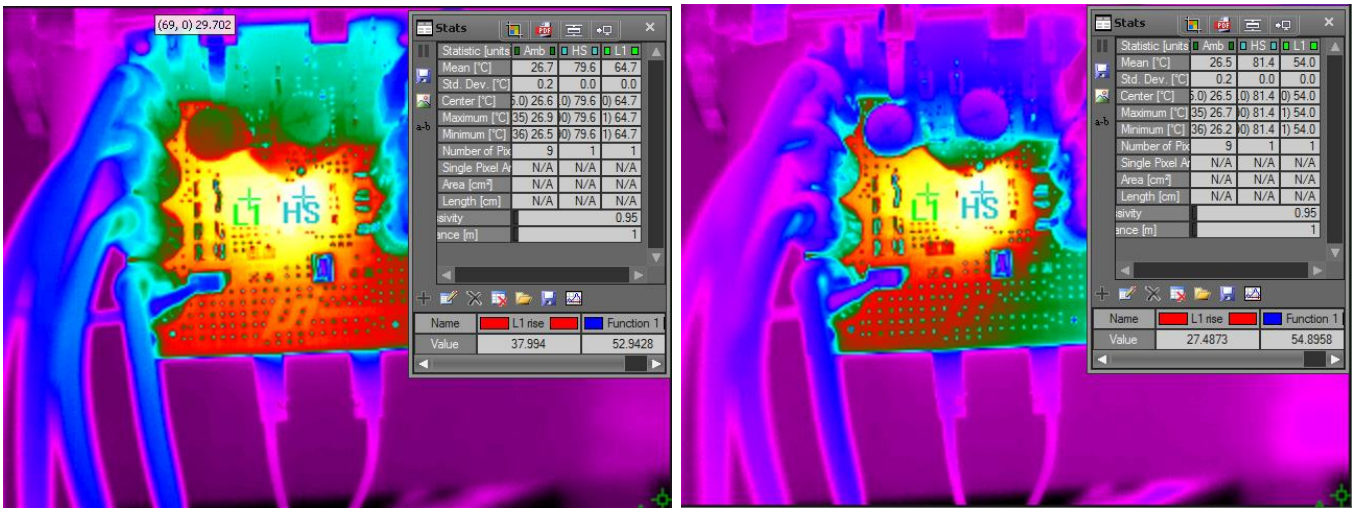


Fig. 8. Test board set-up for temperature and ac testing (note yellow, 50-Ω cables).

Thermal Performance

Fig. 9 shows examples of temperatures of the hottest spots on the two key components, the EPC GaN device and the inductor. In each instance in the thermography below, a Wurth 744403012 inductor is labeled L1 and the EPC2100 GaN device is labelled HS. Before taking the temperature readings, 15 min was allowed at the respective operating points for temperature stabilization.



(a) *(b)*

Fig. 9. Images captured at 12-V input, 1-V output and 19.5 A, and 1-MHz switching with convection airflow (a) and at 12-V input, 1-V output and 24.5 A, and 1-MHz switching with 300 LFM of forced airflow and 37% RH (b). In the table, Function 1 is the temperature rise of the GaN FET.

Conclusion

When low-voltage GaN devices are combined with suitable drivers such as the uP1966D, smaller POL solutions can be realized with little sacrifice in efficiency and operating temperatures. Now that conversion frequencies of 1 MHz and above can be easily realized, inductors can be smaller, output capacitance can be reduced and loop responses can be improved.

In the future, lower $R_{DS(ON)}$ GaN devices will be available that enable parity in efficiency with MOSFETs in higher current (>20-A) applications. These attributes, combined with driver improvements, will make GaN the solution of choice in POL applications.

Reference

"Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter" by D. Reusch and J. Strydom, Applied Power Electronics Conference, APEC 2013, pp. 649–655, March 16–21, 2013.

About The Author

Ron Vinsant is a senior member of Technical Staff at uPI Semiconductor. With more than 30 years of experience in analog and digital power systems design, he has demonstrated success in engineering and application engineering roles at technology companies both large and small, including Vishay Siliconix, Powervation, Fairchild, Zilker Labs, SOMA Networks, Linear Tech, and Teledyne. Prior to joining the power industry, he studied physics at U.C. Berkeley, Calif.

For more on designing power converters using SiC and GaN devices and related product news, see How2Power's Special Section on Silicon Carbide and Gallium Nitride Power Technology.