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Rad Hard Regulator Integrates Synchronous Buck And LDO For Satellites

Renesas Electronics, describes the ISL70005SEH as the industry's first single-chip synchronous buck and low dropout (LDO) regulator targeting low-power FPGAs, DDR memory and other digital loads for spaceflight payload applications. The company adds that this rad-hard dual output point-of-load regulator (POL) is the only point-of-load power solution that reduces size, weight, and power (SWaP) by integrating a synch buck and LDO in one monolithic IC. The device enables satellite manufacturers to reduce bill of materials (BOM) and power supply footprint for their medium Earth orbit (MEO) and geosynchronous Earth orbit (GEO) long duration mission profiles (Fig. 1).

The ISL70005SEH combines a 95% efficiency for the synch buck regulator with a low 75-mV dropout on the LDO regulator. The device enables easier thermal management for systems with 3.3-V or 5-V power buses and can support 3-A continuous output load current for the buck regulator and ±1 A for the LDO. The buck regulator uses voltage-mode control and switches at a resistor-adjustable frequency of 100 kHz to 1 MHz, enabling a smaller filter size.

"The ISL70005SEH gives satellite manufacturers the superior radiation performance, and SWaP and BOM savings they want," said Philip Chesley, vice president, Industrial and Communications Business Division at Renesas. "Our dual output POL regulator also provides the configurability to address multiple applications in commercial telecommunication satellites, military satcom satellites, and science and exploration missions."

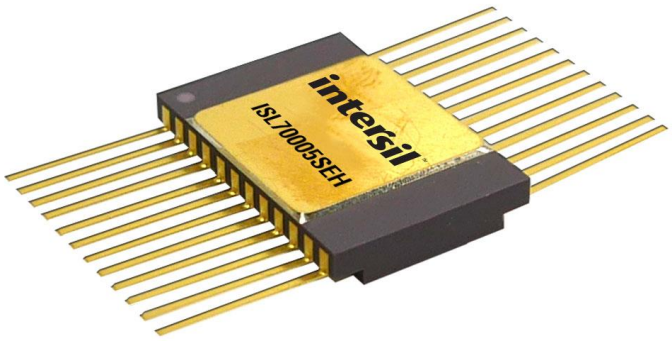
The space-grade ISL70005SEH simplifies design configuration allowing designers to use it as a dual-output regulator, DDR-memory power solution or high-efficiency low-noise regulator for RF applications (see Fig. 2). The flexible LDO can source and sink current and accept input voltages as low as 775 mV to reduce unnecessary power dissipation.

The externally adjustable loop compensation on the buck allows users to achieve an optimal balance of stability and output dynamic performance. The device is wafer acceptance tested to 100 krad(Si) over high dose rate (HDR) and tested for ELDRS up to 75 krad(Si) over low dose rate (LDR). Single event effects (SEE) testing shows no single event latch-up (SEL) and single event burnout (SEB) at a linear energy transfer (LET) up to 86 MeV∗cm^2/mg. Single-event transients (SETs) have been characterized at a LET range of 8.5 to 86 MeV∗cm^2/mg.

Other key features of the ISL70005SEH:

- Synchronous buck Vin range of 3 V to 5.5 V
- LDO Vin range of 600 mV + VDO to Vcc - 1.5 V
- 1% reference voltage accuracy
- Separate VIN, enable, soft start and power good indicator
- LDO stable with 150-µF; 3x less output capacitance than competitive solutions
- Full military temperature range of -55°C to +150°C.

The ISL70005SEH is a single-chip power solution for both FPGA core and I/O rails and can be combined with Renesas analog signal chain ICs to create a satellite telemetry solution. The ISL70005SEH is available now in a 28-lead ceramic dual flatpack package or in die form. An evaluation board is available to evaluate device features and performance. For more information, see the website.



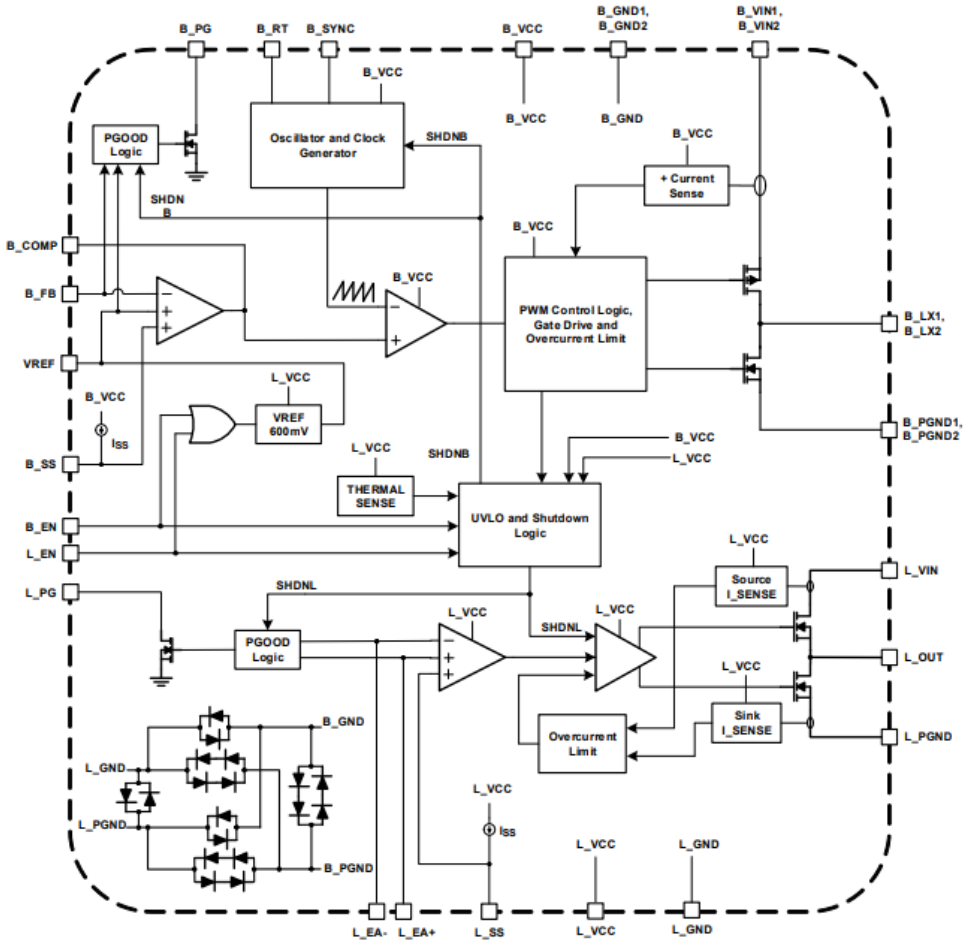


Fig. 1. Housed in a 28-lead ceramic dual flatpack package (top image) or in die form, the space-grade ISL70005SEH combines a synchronous buck regulator and an LDO in one monolithic IC. The device enables easier thermal management for systems with 3.3-V or 5-V power buses and can support 3-A continuous output load current for the buck regulator and ±1 A for the LDO.

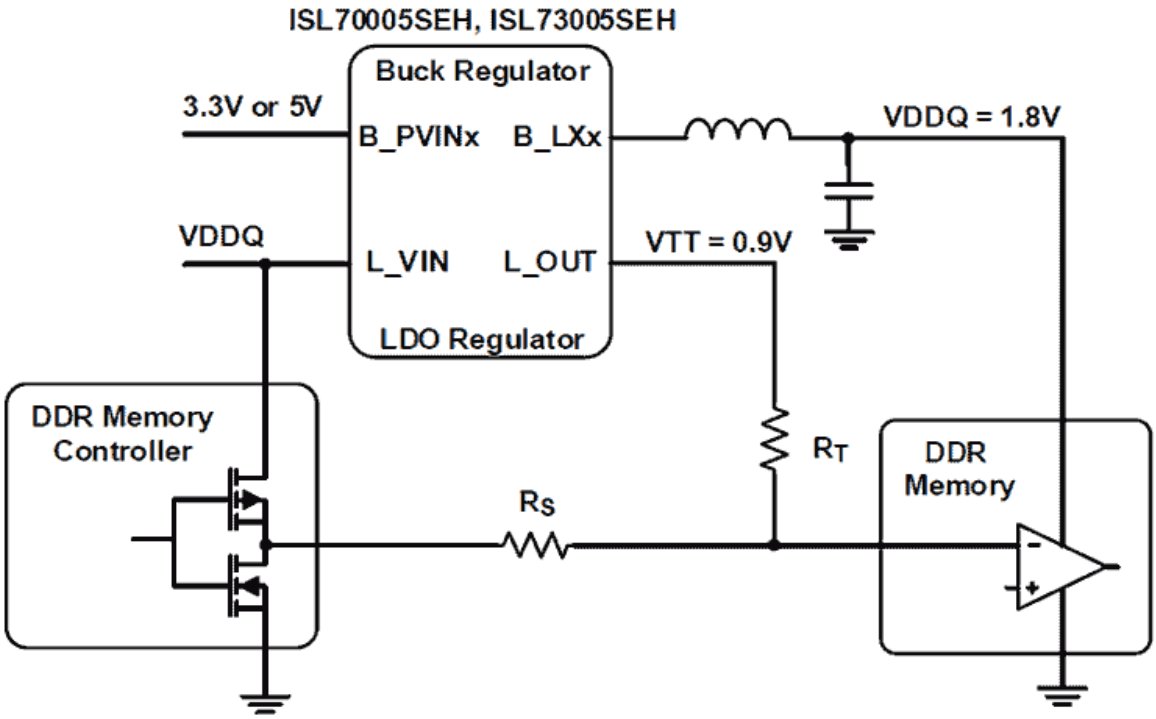


Fig. 2. The ISL70005SEH can be used as a dual-output regulator, DDR-memory power solution.