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The Power Supply Designer's Guide To Radiation Effects In Power Semiconductors

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Let's pretend that in a parallel universe, off in a wormhole somewhere, our predecessors who knew the ins and outs of radiation hardened semiconductors retired, but left no succession plan. They had no understudies or interns to transfer the knowledge to. No mentoring sessions, water cooler chats or lunchroom exchanges. The knowledge just disappeared with a distant generation. New engineers would have a lot of questions and no answers, as would tenured staffers. Most would have never dealt with radiation hardened devices before.

Not that any of this would be possible in *our* universe. But if it were, maybe the brief ramblings to follow would help fill that cosmic gap and offer a bit of utility.

So why is radiation hardened needed? What then of the fundamentals of radiation hardness? How do you design for this? How can a 2N2222A be $0.60 in single pieces at Digi-Key while a JANSR2N2222A[1] is $165.00? What do these things do and how do they work? How then are they tested and validated?

These are the types of questions this article will answer. In this discussion, we explain what happens when different types of charged subatomic particles bombard your power semiconductor devices in space.

We'll begin by explaining how the loss of atmospheric shielding makes electronics vulnerable as we move to higher altitudes. Then we'll introduce Bragg Depth—an idea that helps to explain particle behavior during radiation induced collisions and which is needed to understand the various types of radiation tests that are used to qualify radiation hardened components.

With these basics established, we'll forge ahead in defining the alphabet soup of rad hard testing used to gauge a semiconductor's ability to withstand different types of radiation effects such as SEE, TID, ELDRS, LET, SEB, and SEGR. We'll explain these terms in the context of the familiar power transistors and rectifiers by looking at the impact of particles as they travel through the strata of vertical and lateral devices.

As we'll see, certain device structures are more vulnerable to specific radiation effects than others, and the design of radiation hardened devices reflects these sensitivities. In some cases, device rating or the choice of power supply topology may be effected.

We'll round out the discussion with a few words about neutron bombardment and integrated circuits, and how to interpret the coding in a space-grade part number, which indicates the different levels of JAN screening.

Radiation Effects In Space

Our earthbound electronics are afforded a large degree of cosmic and atmospheric shielding. But shielding is often a misleading term. Having spent a lot of time in the EMC chamber, we always view shielding as something solid, usually something with very low resistivity and sometimes very low reluctance.

Atmospheric shielding operates on a different concept. When a charged particle comes in, perhaps from nuclear reactions on the sun or some other point in deep space, the particle hits stuff. It hits the various gas molecules in the various layers of our atmosphere. As the particle has more and more collisions, it loses more and more energy. By the time the particle reaches the earth's surface, there isn't much energy left or it has stopped altogether somewhere above us. To shift the vantage point of the observer a bit, if we design electronics that go increasingly higher in altitude, the electronics will see more charged particle interactions in their lifetime.

A good, simple reduction to practice may be an airline pilot's routine. The pilot has a lot of window area to observe his or her environment. Most pilots will wear that odd sunscreen on their nose and take other precautions that they wouldn't normally take at sea level. This is due to flying higher, in thinner atmosphere, with less shielding. Of course, there are particles with higher energies than the UVB or UVC photons. These particles concern the electronics more so than the pilot.

If we go out even further, perhaps beyond the earth's atmosphere into low earth orbit (LEO), the atmospheric protections fade, but the earth's magnetic poles still bear some shielding effects. The earth's magnetic poles attract charged particles. These particle concentrations are known as the Van Allen radiation belts. There are two of them.

The inside Van Allen belt is located about 4,000 miles above sea level on earth. It contains high energy electrons and protons. The outer belt is located about 20,000 miles above sea level. It contains mostly lower energy electrons. Geometrically, there is a null in these belts above the north and south pole, leaving the belts arranged as a toroidal shape centered around the earth's equator.

Bragg Depth

Bragg depth gets its name from the efforts of Sir William Henry Bragg and his son, William Lawrence Bragg (see reference 2). Their work won the 1915 Nobel Prize in Physics. While Bragg depth is a simple one-dimensional notion, this term is often shrouded with uncertainty and guarded with false expertise. It's not that bad.

Bragg depth and Bragg distance are synonymous. This measurement describes the depth of penetration of charged particles into a test specimen. In our world of semiconductor devices, the test specimen is usually the device under test (DUT), usually comprised of mostly silicon (Si) by mass. Bragg depth varies with particle size.

From a first-order glance the variation is backwards. Larger particles with more energy have a shorter Bragg distance. But if we consider the collisions, this makes a little more sense. The big heavy particle hits a lot more particles in the DUT than the smaller lighter particle. It imparts a lot more energy into the particles that it hits (consider basic momentum exchange).

The particles that the impinging beam particle collides with then scatter. They don't simply move aside as though they were "nudged." They were hit hard, by something big, fast and large. The particles in the DUT then scatter. This mechanism dissipates the energy from the large beam particle quickly. The large beam particle then runs out of momentum at a shorter distance into the DUT, a shallow Bragg depth, often finding itself painfully in the middle of a MOSFET channel or BJT drift region.

But the smaller beam test particles don't impart as much energy into the collisions. The particles in its collision path don't receive as much momentum, they don't scatter as much. This then allows the smaller beam particle to travel further into the DUT, sometimes passing through it completely. In general, Bragg depth ties to the ion species in the test beam. The larger the ion species, the less the Bragg depth (See Table 1).

A course model of this may be illustrated with a barrel of jellybeans and a stick. If an observer were to force a large stick, hard and fast into the barrel of jellybeans, the stick wouldn't go in very far and jellybeans would scatter all over the test area. However, if the stick were changed to a smaller one, the jellybeans wouldn't scatter as much and the stick would go in further. (If you attempt this experiment, please observe all prevalent social distancing protocols, wash your hands often and do share the jellybeans rather than wasting them.)

Radiation Effects

There are four main tests that a radiation hardened semiconductor must undergo to test the semiconductor's ability to withstand (survive) various types of radiation effects. Single event effect (SEE) testing captures fast, heavy particle collisions. Total ionizing dose (TID) is a slower test with a much slower dose rate. It uses gamma rays from a Co^{60} source. The device under test is exposed for a fairly long time and the effects are measured.

Extreme low dose rate sensitivity (ELDRS) testing represents a subset of TID. The dose rate or flux is much lower than TID as is the total exposure or fluence. Neutron bombardment testing then tests (almost) purely neutron events in the DUT. These different tests can excite different responses ranging from long term degradations to momentary upsets to catastrophic failures. There are only two interactions that stem from these tests, ionic interactions and lattice disturbances.

Table 1. The Bragg table.

Energy Level	Ion	Total Energy	Energy at Bragg Peak	Range in Si	Range at Bragg Peak	Range To Bragg Peak	Initial LET (air)
A (MeV)		MeV	MeV	um	um	um	MeV/mg/cm^2
15	^{4}He	60	0.4	1423	2	1421	0.11
15	^{14}N	210	7	428	7	421	1.3
15	^{20}Ne	300	14	316	8	308	2.6
15	^{40}Ar	599	29	229	9	220	8
15	^{63}Cu	944	90	172	16	156	18.7
15	^{84}Kr	1259	152	170	21	149	26.6
15	^{109}Ag	1634	248	156	26	130	40.3
15	^{129}Xe	1934	339	156	31	124	49.3
15	^{141}Pr	2114	441	154	37	117	56
15	^{165}Ho	2474	608	156	44	112	66.7
15	^{181}Ta	2714	702	155	46	109	74.8
15	^{197}Au	2954	902	155	53	102	82.8
25	^{4}He	99	0.4	3449	2	3447	0.07
25	^{14}N	347	7	1009	7	1002	0.9
25	^{22}Ne	545	14	799	8	791	1.8
25	^{40}Ar	991	29	493	9	484	5.5
25	^{84}Kr	2081	152	332	21	311	19.8
25	^{129}Xe	3197	335	286	31	255	38.9
40	^{14}N	560	7	2334	7	2327	0.6
40	^{20}Ne	800	14	1655	8	1647	1.2
40	^{40}Ar	1598	29	1079	9	1070	3.8
40	^{78}Kr	3117	140	622	20	602	14.4
40	Proton	40	0.1	8148	1.2	8147	0.012

SEE

Single event testing is carried out in a linear accelerator. The most popular linear accelerator used in these tests in the U.S. is located at Texas A&M University. The tests are run at a constant energy per AMU (atomic mass unit). For example at 15 MeV per AMU, a particle having an atomic mass of 4 would then have 60 MeV energy in the beam. But how does this beam energy transfer into the DUT?

For this we have to introduce the concept of linear energy transfer (LET). LET takes into account the particle energy and the media properties. LET is expressed in mega-electron volts per milligram per centimeter squared (MeV/mg/cm^2). SEE is a shorter test as outlined in JEDEC's JESD57A standard. The flux can be anywhere between 10^3 and 10^5 ions/cm^2/s. The total fluence is often 10^7 ions/cm^2. SEE interactions are predominantly ionic in nature.

Like most radiation tests, SEE testing affects different components in different ways. If we consider the discrete vertical MOSFET, as would be found in most any switching application requiring a power switch, we see two dominant effects. These are single event burnout (SEB) and single event gate rupture (SEGR).

SEB is less likely than SEGR in most modern power MOSFET designs. SEB is a compound reaction. In the first part of the reaction, the heavy ion from the test beam impinges at or near normal to the DUT surface into the N+ region under the source metallization (see Fig. 1).

In the second part of the SEB event, the ions from the initial nuclear reaction travel vertically through the die. As they pass through the die, a sheath of electron-hole pairs forms coaxially around the secondary ion path. Note that the MOSFET is in the off state during this event, blocking high voltage across V_{DS} This off state attracts the negative ions (electrons) to the backside of the die or the drain terminal. The positive ions (holes) are then attracted to the source terminal.

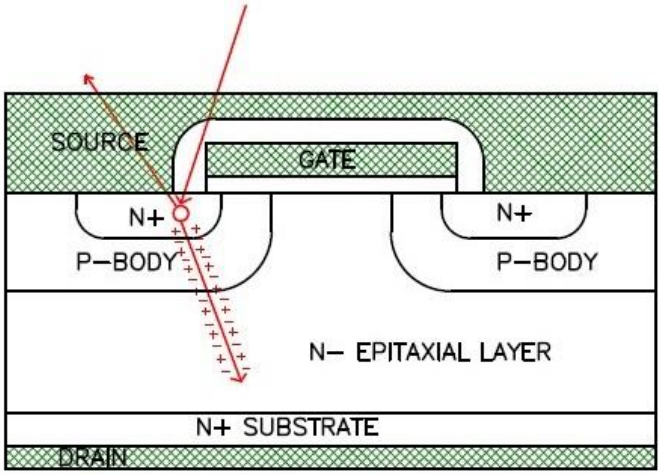

Fig. 1. The initial reaction in a SEB event.

It is important to note the location and design of the intrinsic NPN (depicted on the right of Fig. 2). This intrinsic NPN is a very important element of an n-channel enhancement-mode MOSFET. If the intrinsic NPN is ever turned on, the MOSFET is in the on state regardless of V_{GS} or gate command.

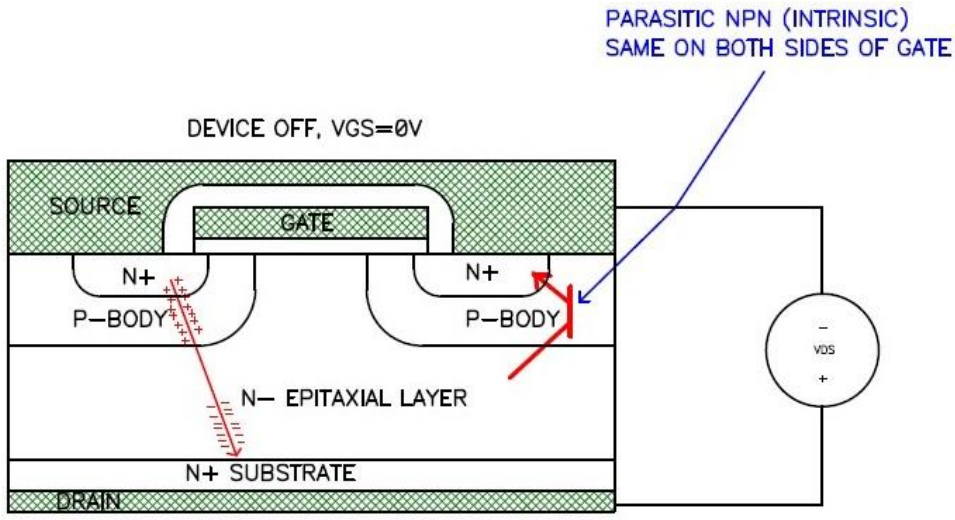

Fig. 2. In the second part of an SEB event, the sheath of electrons and holes formed around the ion path are attracted to respective opposite polarities of V_{DS}. This can lead to turn-on of the parasitic NPN transistor, which then causes the MOSFET to turn on.

By design, the source metallization is to keep a very low impedance (short) across the BE junction of this intrinsic NPN. If enough holes are attracted to the p-body region, the lower portion of the BE junction of the intrinsic NPN can be forward biased. With this, the intrinsic NPN turns on.

This happens some distance (resistance) away from the surface metallization shorting the intrinsic NPN BE junction. When this happens, the device turns on regardless of V_{GS} command. This is the SEB mechanism. In most applications it is catastrophic should it happen. However, note that modern rad hard device designs have minimized the likelihood of SEB.

SEGR is a different phenomenon than SEB. In view of SEB, SEGR is more likely to occur in a modern MOSFET design. SEGR also impacts a MOSFET in the off state. V_{DS} is at a high blocking voltage, usually tested at datasheet V_{DS}. V_{GS} is at a negative voltage. The device is assuredly off.

In terms of E field, it is important to note that there is a positive voltage on the drain and a negative voltage on the gate. In a vertical structure, this is a high E field. Extreme positive on the substrate, extreme negative on the gate, over a short distance. Maximum V/m! Under these conditions, a heavy ion travels through the gate, the gate oxide and the channel of the MOSFET. As per the Bragg relationships, the ion may stop in the channel, in the substrate or perhaps pass through. A sheath of electron-hole pairs is formed around the heavy ion path (see Fig. 3).

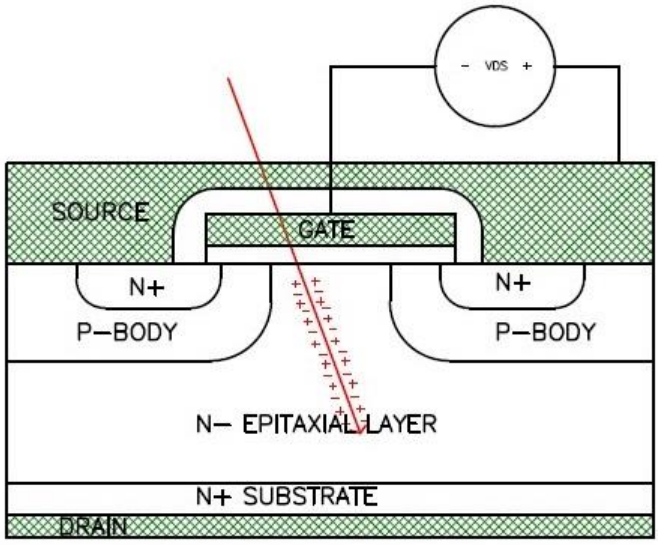

Fig. 3. An SEGR event in a MOSFET, initial heavy ion path.

This momentarily alters the E field distribution. The N-epi layer rises up sharply toward the gate (Fig. 4). This then reduces the distance between the drain and the gate, thereby increasing the E field even higher, with a fairly sharp gradient directly under the gate. When this field is high enough, the gate oxide will rupture and the device will fail. Radiation hardened MOSFETs are designed with this in mind.

As a side observation, we hear more and more about SiC MOSFETs. SiC MOSFETs have lower R_{DSON} per unit area and the material can handle much higher E fields. To consider this, a smaller device can then handle more current and higher voltage. The sine qua non of power switch improvement!

The very same attributes that make SiC a sought-after improvement over Si are detrimental at SEGR. The gate oxide sees much more stress in the SiC device at rated voltage and SEGR conditions, the E field is much higher. It is for this very reason that modern SiC MOSFET realizations are slow to be adopted into radiation hardened designs.

The present SiC geometries are very susceptible to SEGR, however once derated to Si type E-fields, the devices may perform well. At present state of the art, this means a 1200-V SiC MOSFET might pass SEE testing at a V_{DS} of 200 V to 250 V.

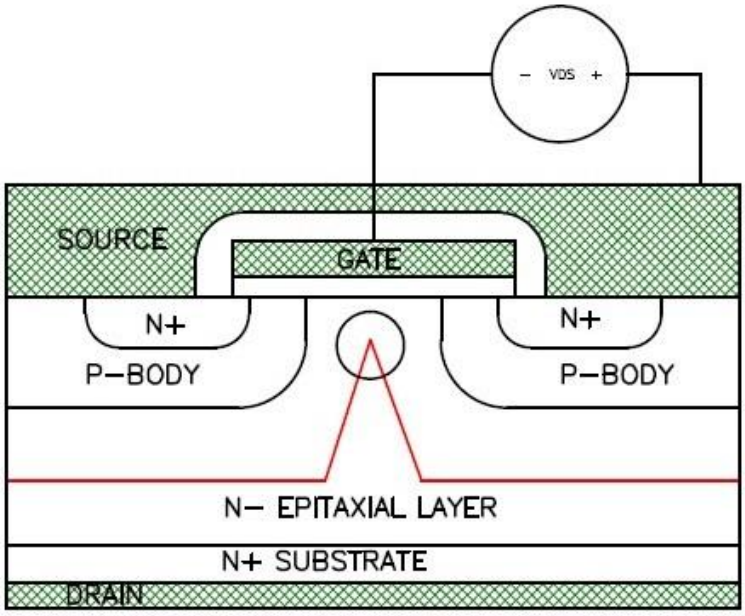

Fig. 4. SEGR resultant E-field gradient.

SEEs in BJTs are fairly minimal. There has been some testing that has shown single event transients (SETs) in BJTs biased in linear modes. This is believed to be simply a transient event and harmless. A coarse model of the transient event involves the heavy ion passing through or stopping in the drift region. This event momentarily disturbs the carrier distribution. A click type noise can then be seen looking at the collector.

Schottky diodes were initially thought to be immune to SEEs. However, many tests have shown single events in Schottky diodes at higher voltages. In a high-voltage Schottky, the incident heavy ion displaces some of the metal in the barrier junction into the semiconductor material. This small displacement gives rise to a high E-field around the displaced area. The high E-field then degrades the local material (electromigration) until ultimately the device fails short. Low-voltage Schottkys don't exhibit this problem.

Again, we can consider the higher E-fields supported by SiC Schottky diodes in view of Si. This is detrimental for SiC. To pass SEE tests, SiC Schottky diode voltages have to be derated by a large amount, again perhaps a 1200-V SiC Schottky derates to 200 V to 250 V to pass SEE testing.

PN junction diodes are relatively immune to SEE.

SEE Design Considerations

To design for SEEs, an engineer will carefully consider the SEE mechanisms when selecting power MOSFETs and Schottkys. In-house derating guidelines must be adhered to, for example, the design procedure may be to derate the MOSFET V_{DS} by a factor of two or more. For example, on a 120-V bus, a 250-V MOSFET may be specified.

Other good design procedures should be adhered to. For example, the gate-drive circuitry should be designed to hold the device off through worst-case commutation speeds. During fast commutation, the C_{OSS} of the MOSFET that was on at t0- turns off quickly. C_{OSS} of this MOSFET then charges up from 0 V to the rail voltage.

If this happens quickly, charge is coupled into C_{ISS} through C_{RSS}. This is often dubbed Cdv/dt turn-on. The driver off-state impedance must be low enough to hold the MOSFET off through this fast commutation (Figs. 5 and 6).

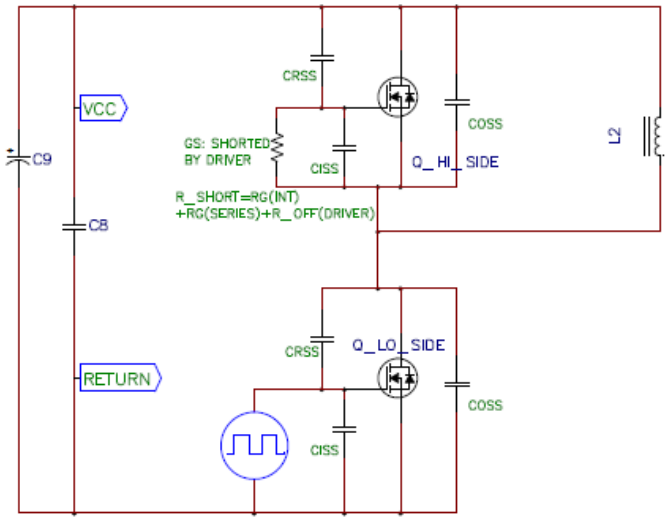

Fig. 5. Double pulse test setup used to examine Cdv/dt turn-on events.

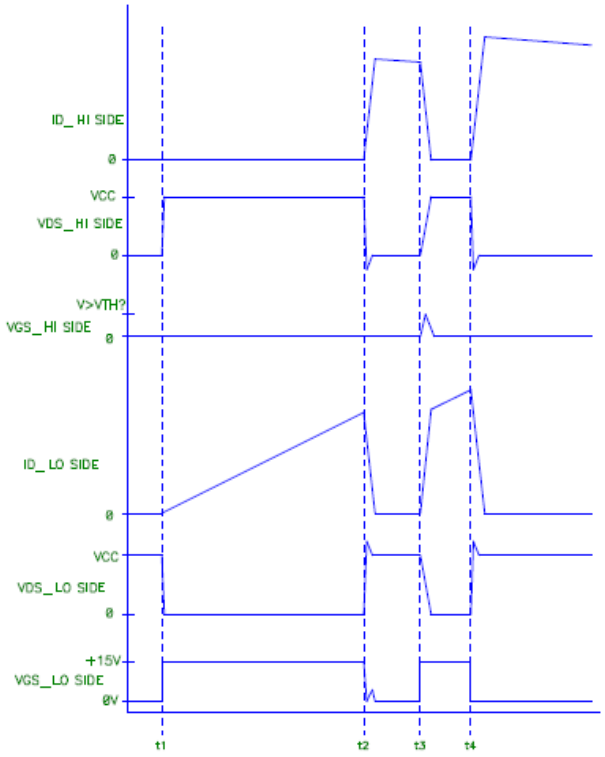

Fig. 6. Waveforms from double pulse. Note fast commutation at t3. V_{GS} Hi Side sees a positive V_{GS} at this point due to fast charging of C and coupling through C_{RSS}.

TID

TID is a much slower test than SEE. TID relies on a higher fluence of CO60 gamma ray source over a lower flux. It is designed to mimic long-term exposure to radiation. The tests are carried out as per MIL 750, TM1019. TID interactions are ionic in nature.

TID effects in MOSFETs are fairly minimal. The most notable interaction is that of hole trapping and the resultant V_{TH} shift. As the gamma rays impinge on the gate oxide, holes and electrons are created on the semiconductor surface. The electrons recombine faster than the holes, creating a surplus of holes. These holes cause a shift in the threshold voltage over increasing fluence.

An n-channel MOSFET will exhibit a negative threshold voltage shift whereas a p-channel MOSFET will exhibit a positive shift in V_{TH}. For a good radiation hardened process, the shift may be on the order of 1 V at perhaps 100 krad fluence. The other impacts are fairly small, but the leakage currents will increase slightly over increasing fluence (I_{DSS}, for example).

TID effects in BJTs are much more substantial. The basic mechanism is the same as in a MOSFET. Electrons and holes accumulate on the surface of the device. In the case of the BJT there is no oxide to trap the holes. The holes accumulate as a resistive sheet across the BE junction shunting base-drive current. This then requires more base current for the same collector current. The mechanism reduces the gain (Fig. 7).

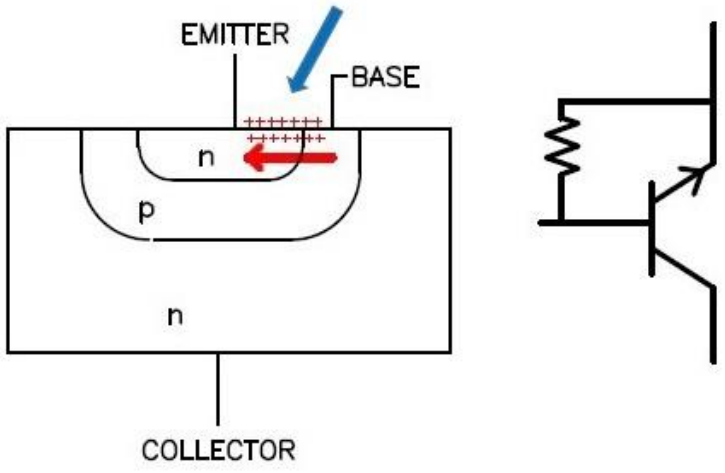

Fig. 7. TID mechanism in BJT. The blue arrow is an impinging gamma ray, and the red arrow shows the base current shunt path.

But there are subtleties to this gain reduction. V_{CBO} and V_{CEO} are related by gain. Anyone remembering perhaps the old days of using BJTs for HV power switches will remember this relationship. The lower the H_{FE}, the higher V_{CEO} with respect to V_{CBO}. These voltages were related by BE storage time. A higher H_{FE} BJT has a higher BE storage time. This is to say that higher H_{FE} means more carriers in the BE junction, thereby it takes these carriers longer to recombine than a lower H_{FE} device (all processes the same).

If we can drop the gain and drop the BE storage time, BE recombines quicker and enables a higher V_{CEO}. After TID testing, it can usually be observed that V_{CBO} has stayed constant while V_{CEO} has increased slightly. Higher voltage processes tend to show a sharper increase in V_{CEO} vs fluence. Clearly V_{CEO} can never surpass V_{CBO}, but it can approach that value. Other effects from TID and increasing fluence are increasing leakage currents in the BJT.

TID effects in Schottky diodes are negligible. TID effects in PN diodes are often disregarded, but there are some subtle performance differences in the dynamic performance parameters of the irradiated diode.

In a different diode application, there was a need for soft reverse recovery. The (then) state-of-the-art ultrafast PN junction diodes were very fast, but very snappy. These devices had long t_A and very fast t_B. Worse yet, they had very large I_{RR} (often 5x I_F). Q_{RR} was then substantial. To use these diodes was difficult. Lossless snubbers had to be set up around the diode to tank the I_{RR} pulse, store it and then switch it into the output (Fig. 8).

The first sign of relief in this application came as an irradiated PN junction diode. The concept was that the backside of the diode wafer was irradiated in processing. This irradiation created recombination regions and some small steps in the bandgap of the diode. These recombination regions increased V_F slightly and dramatically decreased I_{RR} and Q_{RR} while raising t_B slightly and making the structure much less snappy (Fig. 9).

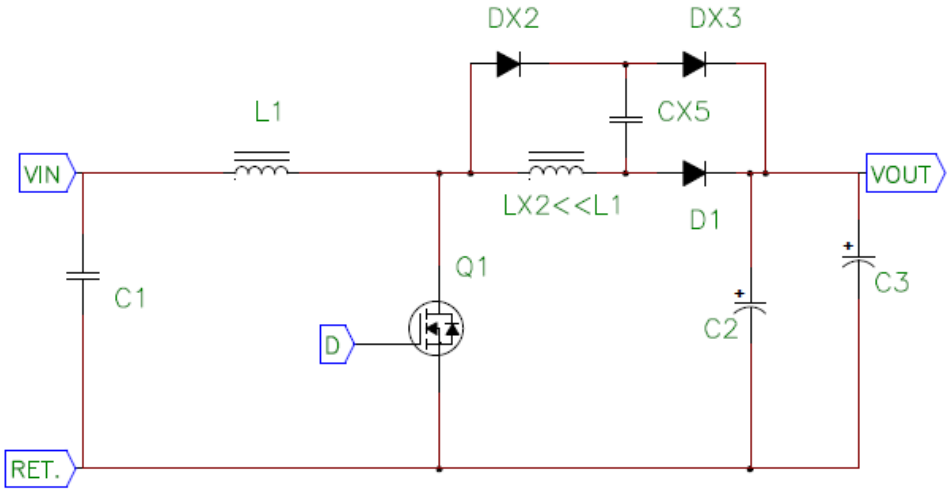

Fig. 8. Boost converter schematic with snubber (Note: inductor current is in continuous conduction mode).

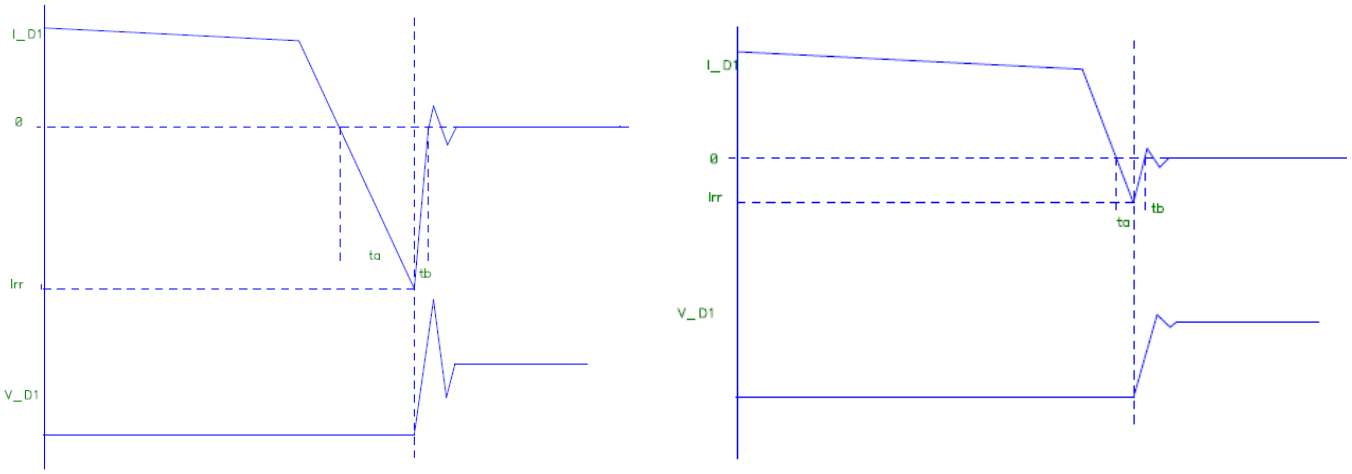

Fig. 9. Diode reverse-recovery waveform without (a) and with (b) backside irradiation. In the latter case, t_B is softened, and I_{RR}, Q_{RR} and E_{RR} are much lower. Waveforms for the irradiated diode are less snappy and contain less energy. (As a result, the CCM boost snubber is likely no longer needed)!

Our takeaway from this is that irradiation of a PN junction diode does in fact change the operation a bit. V_F can rise slightly while the ad hoc recombination regions that the irradiation creates soften the reverse recovery event of the structure. This is not a major attribute in most designs, but it is worthy of mention.

Designing For TID

For MOSFETs, this is much like designing for SEE. Gate drive becomes very important. If an n-channel MOSFET is being driven at end of life (EOL), perhaps at a hot temperature, the threshold may be in the 1 V or less range. Recall, threshold shifts downward with temperature and then even further with the added hole-trapping mechanism from TID. The gate driver must then hold that device off through Cdv/dt events during commutation.

For BJTs, the design tricks are very application dependent. The best example is likely a flyback converter using a BJT for a power switch (Fig 10.)

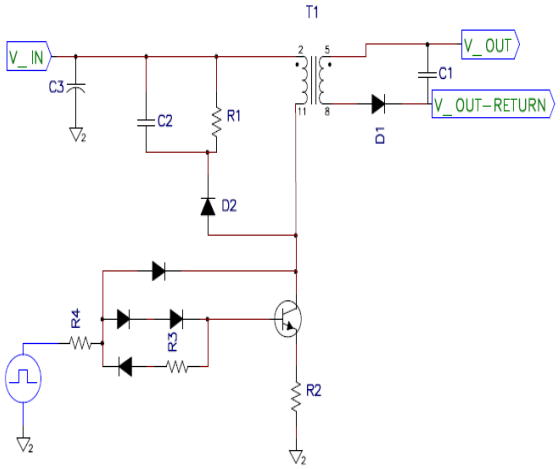

Fig. 10. BJT flyback.

This circuit drives the BJT such that it is either saturated or off. Initially, perhaps at beginning of life (BOL), the gain of the BJT is high. To drive the BJT too far into saturation will surely help the conduction losses of the device, but at a serious detriment to the switching losses. Remember it will take a long time to sweep the minority carriers out of the BE junction at turn off. This is excessive switching loss.

The circuit in Fig. 10 allows the V_{CESAT} of the device to be fairly constant over the lifetime and gain degradation of the device. This is called a Baker clamp. If the base is driven hard enough to pull V_{CESAT} too low, the excess drive current is simply steered through the collector. At EOL, the design will steer less current through the collector and the device will still operate at a fairly constant V_{CESAT}.

PN junction diodes and Schottky barrier diodes require no special design considerations for TID, other than perhaps the minor PN dynamic change noted above.

ELDRS

Enhanced low dose radiation sensitivity (ELDRS) testing is a subset of TID testing. It is carried out with the same ion species in the same fashion. The flux and fluence are lower. Flux is in the range of 0.5 mRad/cm^2/s to 10 mRad/cm^2/s. Total fluence is in the range of 5 krad to 50 krad.

It is accepted that at higher flux the holes on the surface of the device have more charge than at lower flux. Higher flux holes then repel each other more uniformly and spread out more so over the small area. At lower flux, the repulsion isn't as strong, and the holes can cluster up. This means that some devices will be more susceptible to low dose rates. This is the basis of ELDRS.

MOSFETS, PN junction diodes and Schottky barrier diodes are relatively unscathed by ELDRS. BJTs can be sensitive to this depending on process and voltage. Smaller features tend to have more sensitivity.

The procedures in designing for ELDRS are the same as designing for TID.

Neutron Bombardment

In the neutron bombardment test, the devices are unbiased. The parts are often placed in a bag and hung in the beam. Neutron effects are displacement effects. The test is carried out as per MIL STD 750 TM1017.

The substance of this test is unique in that neutrons don't have a charge. Protons, ions, gamma rays all have some charge, they are attracted to other particles. Neutrons are not. The stopping distance of a neutron is much larger than that of a Co^{60} gamma ray source or a heavy ion. The neutron passes through the DUT.

The neutron fluence ranges from 10^9 n/cm^2 to 10^{13} n/cm^2. In that neutrons have no charge and substantial mass, they are less attenuated by the Van Allen belts and the earth's atmosphere. This leads other industries to look at neutron bombardment including aviation.

The procedure for designing a circuit for a neutron event is similar to designing a circuit for TID.

What About Higher Levels Of Integration In ICs?

Thus far, the discussion was on a two- or three-layer device such as as a diode, BJT or MOSFET. What then happens when we add the fourth layer? If a PNPN stack, it is very likely that there can be a latchup mode, where the device enters a latched condition (Fig. 11).

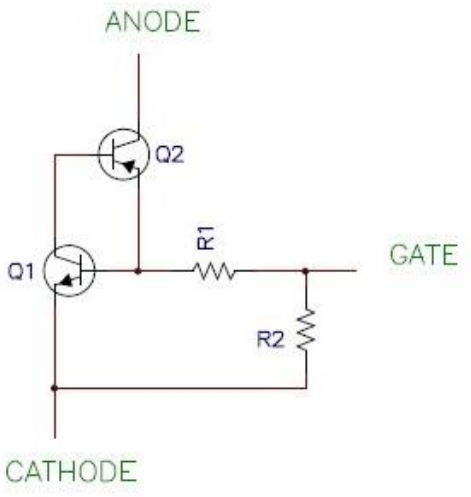

Fig. 11. A simple PNPN stack, also known as SCR, can experience latchup when exposed to radiation.

Worse yet, what if we were on a bipolar or BiCMOS IC process with perhaps 12 to 16 layers? Gates? State machines? Differential amplifiers? Thresholds? Bandgaps? Clearly the possibility of latchup, SEE, ELDRS, neutron, or TID issues increase exponentially. These matters are not trivial. They often define the difference between radiation hardened and radiation tolerant.

Radiation hardened devices were designed in processes that were completely vetted and understood. Every cell, every connection, every junction. Radiation tolerant devices came from commercial, industrial or automotive processes. They were tested exhaustively and found to be tolerant, but they were not explicitly designed for a radiation environment.

What Then Is JANS?

With these brief descriptions, the next logical question should be one of specification and screening. All of this Joint Army Navy or JAN stuff can get a bit confusing. In general, when we consider space applications, JANTX is often the lowest quality level considered, JANTXV adds a visual inspection to the screening process, while JANS adds several additional screening steps.

The designator that comes after the JAN prefix is one of Radiation Hardness Assurance (RHA) level. For this designator, TID fluence is used. L is used to denote 50 krad, R is used to denote 100 krad, F is used to denote 300 krad, G for 600 krad, and H for 1000 krad. With this we can decode the prefix to a part's model number. For example, JANSR2N2222A[1] is a space-grade device, with RHA to 100 krad.

For the specific screening we refer to MIL PRF19500. Table 4 in Appendix E is very insightful in terms of what is screened at the device level. This table is reproduced below as Table 2.

Table 2. Screening for JAN parts (re-written version of PRF19500, Appendix E, Table 4).

Screen	MIL STD 750 Method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
1. Internal Visual Inspection	2073, 2074, 2069, 2070, 2072		100%	100%	NA
2. High Temperature Life	1032	Tstg≤175C, t as specified	optional	optional	optional
3a. Temperature Cycling	1051	No dwell is required at 25 deg C. Test Condition C, or maximum storage temperature, whichever is less, 20 cycles, t(extremes)≥10 minutes	100%	100%	100%
3b. Surge (as specified)	4066	Condition B as specified	100%	100%	100%
3c. Thermal Response	3161, 3131, 3101, 3103, 3104	As Specified	100%	100%	100%
4. Constant Acceleration	2006	Y1 direction at 20,000 G min except at 10,000 G minimum for devices with power rating ≥10W at Tc=25 degC. The 1 minute hold time requirement shall not apply.	100%	optional	optional
5. PIND	2052	Condition A	100%		
6. Instability Shock Test, Axial lead diodes only	2081, 2082		100%		
7. Hermetic Seal	1071	omit for double plug diodes. Test condition G or H, maximum leak rate =5E-8 atm cc/s except 5E-7 atm cc/s for devices with internal cavity > 0.3 cc. Maximum Leak Rate =5E-6 atm cc/s for cavities of 3-40cc	optional	100%	100%
8. Serialization		see 3.10.9	100%		
9. Interim electrical parameters		as specified	100%	for case mounted rectifiers as specified	for case mounted rectifiers as specified
10. High Temp Reverse Bias (HTRB)	1039, 1039, 1042	Test Condition A. 80% minimum of rated Vcb (BJT), Vds (MOSFET)	100%	100%	100%
11. Interim electrical and delta parameters		As specified, but including all delta parameters as a minimum. When HTRB is performed leakage current shall be measured on each device before any other specified parametric test is made	100%	100%	100%
12. Burn In	1039, 1042, 1038, 1040	As specified	100% (240 hours)	100% (96 hours)	100% (96 hours)
13. Final Electrical Test		as specified	100%	100%	100%
14. Hermetic Seal	1071	(same as 7. above)	100%	optional	optional

Clearly the JANS quality-level parts undergo a lot of electrical, mechanical and visual screening as well as burn-in. This takes hundreds of hours. We might compare this to a more commercial or industrial semiconductor process where a full automated test might take a few seconds. This high level of screening and quality is also completely documented and traceable. This is the reason for the cost difference between the 2N2222A and the JANSR2N2222A.

Conclusions

While this is surely no replacement for the endless information offered on NASA's RADOCs website, it might offer a little explanation of some common terms and tests, as well as some considerations for circuit designs in gamma, heavy ion and neutron environments. Take this information for use in the design of circuits, the specification of the components and understanding the intensive screening and how these parts are applied.

References

1. JANSR2N2222A product page.
2. William Henry Bragg, Wikipedia entry.

About The Author

Paul Schimel is a principal power electronics engineer in the Aerospace and Defense group at Microchip Technology. He has over 24 years of theoretical and hands-on experience in power electronics, spanning military, aerospace, automotive and industrial markets. Paul's work regularly includes module design, dc-dc converter design, device-level analysis, root cause analysis, failure analysis, EMI mitigation, PCB layout, control loop compensation, inverter design, transformer design, rotating machine design, bench-level measurement and validation techniques and system-level analysis/comprehension.

He has designed dc-dc converters from milliwatts to megavolt-amps, inverters to 5,000 HP. He is a licensed professional engineer (PE) and holds two FCC licenses (First Class Radiotelephone and extra class amateur). In addition, Schimel holds three patents on power electronics matters.

For more information on designing rad hard power converters, see the How2Power Design Guide, locate the Extreme Environments category and select "Radiation". For information on rad hard power converters and power semiconductors, see How2Power's Space Power section.