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Analysis, Simulation And Experimentation Enable Successful Design Of Power Supply Compensation

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Loop control represents an important aspect of the design of a switching power supply. However, for various reasons, its study is often relegated to the end of the project when the main components have already been selected. Through simple trial and error, it is sometimes possible to get the impression that a design delivering an acceptable transient response on the oscilloscope is ready for production but this is a very unwise and potentially costly attitude.

That's because most of the components used in the converter are affected by stray elements whose wide-spread effects are hidden during the prototype stage. Without a thorough analysis backed up by simulations and loop measurements, you have no idea what phase and gain margins look like and how solid they are. It is very likely that such a loosely designed converter will fail in production or shortly after being powered in the field. To keep you away from such situations, this article reviews some of the tools currently available to let you calculate, simulate and measure your prototype's control loop before safely pressing the production start button.

The Importance Of Power Stage Response

A switching converter is composed of a power stage whose output is controlled by a voltage variable. Labeled V_{err} or V_c in this article, it is delivered by a compensation block which maintains the converter output within regulation. For converters operating at a fixed switching frequency F_{sw}, the control variable is the duty ratio D. But that is not always the case and some converters are controlled by a variable frequency (resonant converters like the *LLC* for instance) or a variable on- or off-time. In this article, we will mainly concentrate on fixed switching frequency types.

The error voltage V_{err} can directly control the duty ratio in which case we're talking about voltage-mode control (VM) or direct duty ratio control. On the other hand, there's also current-mode control (CM), where the control voltage V_c fixes the inductor peak current on a cycle-by-cycle basis via a sense resistor and *indirectly* sets the operating duty ratio.

However, when the oscilloscope displays waveforms from a converter, you cannot tell whether it's operating under CM control or VM control. This is because the power stage is similar between the structures and only the way the duty ratio is calculated changes: a buck converter delivering 5 V from a 10-V source to a load will exhibit a theoretical 50% duty ratio whether the system is operated in voltage- or current-mode control.

Our goal, as power supply designers, is to build a reliable converter capable of delivering a precisely regulated voltage (or current) while being insensitive to operating conditions: input source variations, changes in the ambient temperature, different loading conditions etc. Beside these practical requirements, the designer must ensure that his converter remains stable and operational during its entire lifetime.

There are natural manufacturing variations and component performance degradations due to aging you must cope with. What about my nice design margins five years from now? How confident am I in my choices if my buyer friend shows me the new cheaper capacitor the factory has selected? "Hey Joe, can you confirm the new one-million piece batch of your adapters will be ok if we choose brand B for the output capacitor over the currently stored brand A?" Could you fearlessly answer the question?

You could, indeed, if you have done your homework and carefully studied the impact of the capacitor parasitics on crossover and phase margin for instance. But if you did not and just looked at the step response in the lab while tweaking the *R* and *C* knobs of the compensator, then yes, wipe the sweat drop off your forehead, nights are going to be short to keep disaster away.

One way to avoid the trap is to do things by the book and start with the power stage response. This is the only starting point: you need to characterize the system you want to control before ever thinking of a possible control strategy. What you want is to determine how the output variable responds to a change in the control input. This means that you need the *control-to-output* transfer function of the buck or the boost converter you plan to build: what is the dynamic *response* of V_{out} to a given *stimulus* in V_{err} (Fig. 1). In other words, what is the *plant* response?

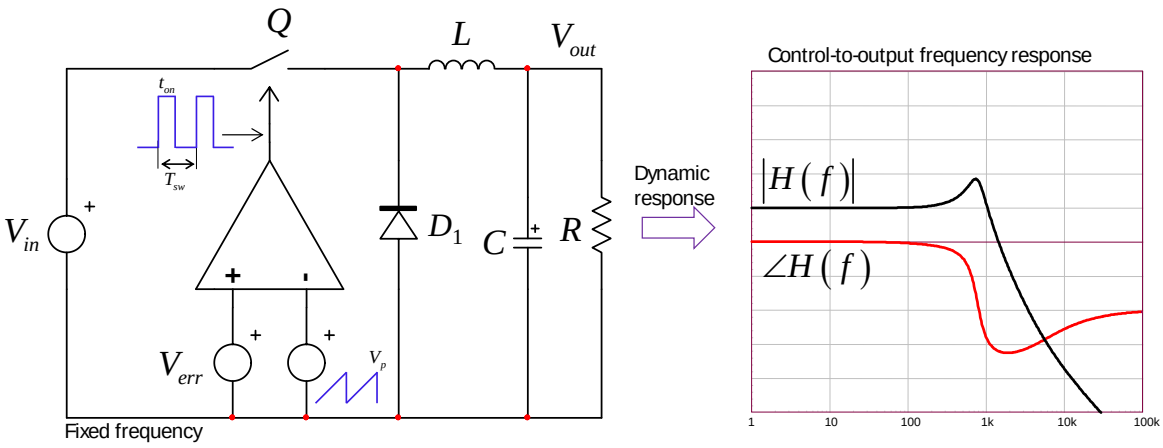

Fig. 1. We want dynamic response of the power stage.

Once you have the transfer function magnitude/phase plot in hand, then you can think of a compensation strategy consisting of placing poles, zeroes and gain (or attenuation) at various frequency locations to meet your design goals which will include appropriate gain and phase margins. The role of the compensator in the power supply feedback path is illustrated in Fig. 2 along with an example compensator response.

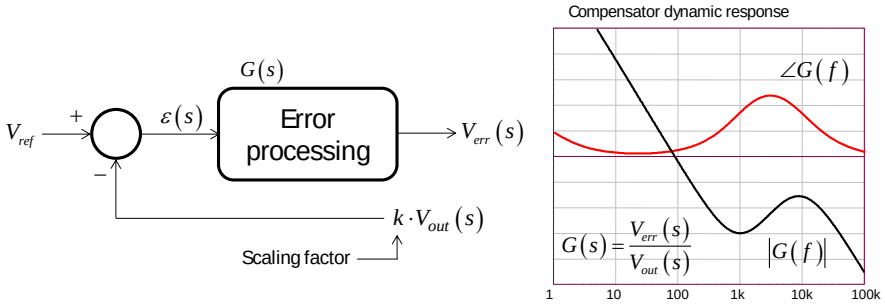

Fig. 2. The compensator (i.e. the error processing block and the scaling factor) is the place to insert poles and zeroes and shape the frequency response you want.

There are several paths to follow when you build compensators as illustrated in Fig. 3. The classical option is widely described in the literature and resorts to an operational amplifier (op amp) for building a filter because a compensator is nothing other than an active filter.

However, in the industry, the TL431 shunt regulator rules and you can find it in the vast majority of adapters sold on the market these days. I confess that it is difficult to beat in terms of simplicity or cost: for a few cents, you have a moderately high open-loop gain (55 dB) op amp packed with a precise 2.5-V voltage reference V_{ref} down to 1.24 V for the TLV version. The part is available in different packages and some versions can accept up to 36 V. Selecting the device however, brings other issues linked to fast and slow paths as described in reference [1].

An operational transconductance amplifier or OTA can also be selected for compensation purposes. Integrated circuits designers like OTAs because they tend to occupy less silicon area than their op amp counterparts. I am personally not a big fan of OTAs because you do not have the virtual ground provided by an op amp-based compensator. Furthermore, the resistive divider ratio affects the pole-zero placement.

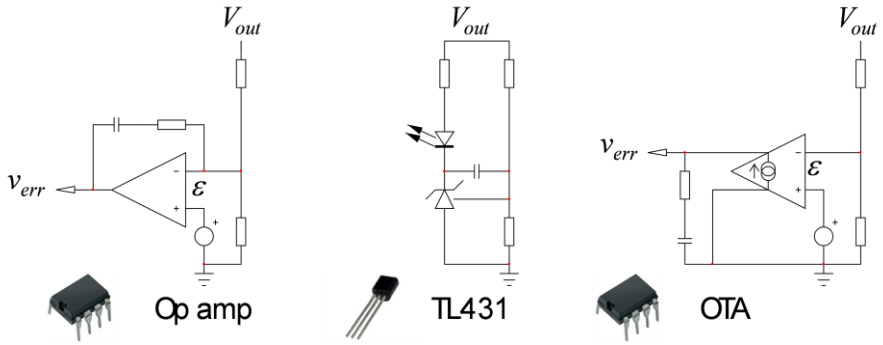

Fig. 3. There are several active elements to choose from when designing the compensator.

OTAs are popular in power factor correction (PFC) applications and lend themselves well to realizing compensators with a moderate *phase boost*. But if you plan to use them for applications where a high phase boost is necessary, you may hit an upper limit imposed by the ratio V_{out}/V_{ref} as described in reference [2].

The phase boost is the amount of extra phase you need from the compensator to meet your phase margin goals, usually a number greater than 45°. If you look at Fig. 4, you see a power stage having phase lags of 90° or 145° at some selected frequencies f_1 and f_2. Should you close the loop with a standard integrator exhibiting a permanent 270° lag, then the sum of the two contributors at f_1 will be -360° or 0°: the signal returns in phase at the injection point and conditions for sustained oscillations are met. Not something you want unless building an oscillator is your goal.

Now, should you force crossover at f_2, the phase margin is negative, meaning the closed-loop poles are located in the right half-plane: the system is unstable. You counteract this problem by creating *phase boost* at f_1 or f_2. By inserting poles and zeroes in the compensator, you tailor its phase response to no longer be permanently -270° but less than that. When combined with the plant response, the total argument or phase will now be less than -360° creating the *phase margin* you want for stability purposes.

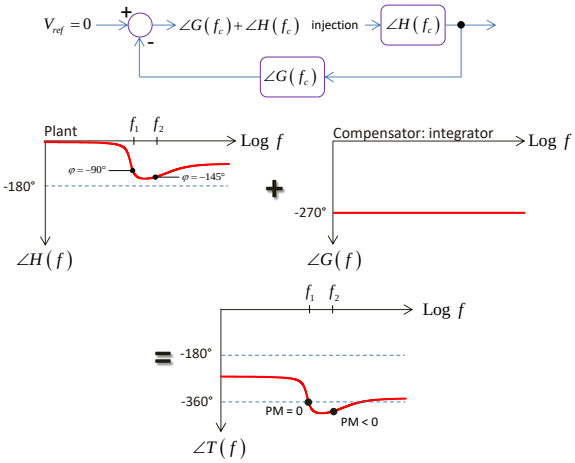

Fig. 4. Summing the phase of the plant with that of the compensator should bring the total lag below -360°.

We can identify three compensator types known as type 1, 2 and 3.[3] They are represented in Fig. 5.

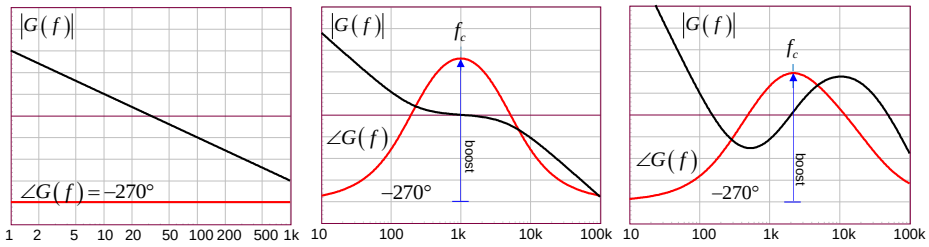

Fig. 5. The three configurations let you implement your compensation strategy.

The first type includes a pole at the origin: it is an integrator described by the following transfer function:

$$G_1(s) = -\frac{1}{\frac{s}{\omega_{po}}} \qquad (1)$$

There is no phase boost and the phase is that of the inverting op-amp structure (-180°) plus that of the pole of the origin (-90°) leading to a final argument of -270° or 90°.

The type 2 is commonly encountered in current-mode control designs where a phase boost below 90° is needed. It includes a pole at the origin plus a pole and a zero. The pole at the origin (s = 0) theoretically cancels the static error (the dc deviation between the target and what you have once the loop is closed). This pole is present in the vast majority of compensators but there are techniques such as the so-called *output resistive shaping* which purposely omits this pole and accepts a small deviation.[4]

In the type 2, the zero is located before the pole and brings the phase high as frequency increases. The pole kicks in later on and the phase boost returns to zero. By spreading the zero and the pole, you adjust the phase boost you want up to 90°. Please note that having pole and zero coincident turns the compensator into a type 1 with a 0° phase boost.

The transfer function describing this structure is as follows:

$$G_2(s) = -G_0 \frac{1+\frac{\omega_z}{s}}{1+\frac{s}{\omega_p}} \qquad (2)$$

You can see the presence of the *inverted zero* in the numerator which allows the factorization by G_0 having the dimension of a gain.[4]

Finally, the type 3 compensator adds another pole-zero pair to the type 2 and can boost the phase up to 180°. It is described by the expression below:

$$G_3(s) = -G_0 \frac{\left(1+\frac{\omega_{z_1}}{s}\right)\left(1+\frac{s}{\omega_{z_2}}\right)}{\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)} \qquad (3)$$

If we now use a type 3 circuit for $G(s)$ instead of a pure integrator in the Fig. 4 example and boost the phase by 125°, the total loop phase is now away from the 0° or -360° limit and we have a 70° margin as shown in Fig. 6.

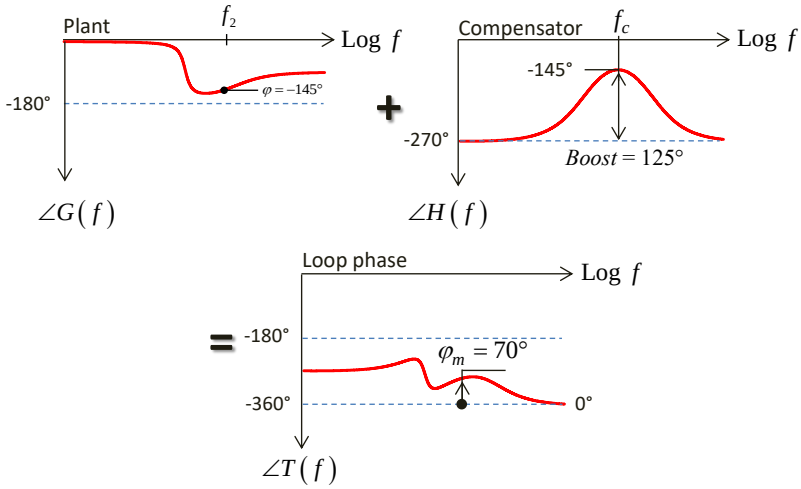

Fig. 6. The phase margin is now 70° using a type 3 compensator.

It is possible to derive a formula linking the amount of needed phase boost based on the power stage lag and the phase margin φ_m we want. We know that the inverting op amp and the pole at the origin bring a 270° lag to which we add the power stage phase characterized at the selected crossover frequency f_c. When adding these numbers, the result should be away from the -360° limit by the phase margin amount. Therefore, we can write:

$$\angle H(f_c) - 270° + boost = -360° + \varphi_m \qquad (4)$$

Solving for the boost value, we find:

$$boost = \varphi_m - \angle H(f_c) - 90° \qquad (5)$$

From this number, we will infer which compensator type to use:

- No boost needed: type 1. Suitable for discontinuous conduction mode converters and, to some extent, PFC stages.
- Up to 90°: type 2. Popular with current-mode-controlled converters (flyback and PFC stages for instance).
- Beyond 90° and up to 180°: type 3. Usually implemented in voltage-mode-controlled converters operating in continuous conduction mode (CCM).

Obtaining The Power Stage's Dynamic Response

As already pointed out, the key to starting the compensation study for a given switching converter is the power stage Bode plot. There are several ways to obtain it and the first one uses an average model in a SPICE simulation.

Average models are available in many versions but the most popular one is the three-terminal PWM switch introduced by Vatché Vorpérian in 1986 and published in 1990.[5] The original work covered voltage-mode control and current mode was addressed later on but covered CCM only. I have derived auto-toggling versions of these models in reference [1] for both VM and CM operation.

A typical buck converter operated in current mode would be modeled as suggested by Fig. 7. The PWM switch is connected in a so-called common-passive configuration in which terminal *p* is grounded. The XPWM block models the pulse-width modulator which converts the error voltage set by source V_2 into a duty ratio. The gain of this *naturally-sampled* modulation block is simply the inverse of the sawtooth peak value V_p biasing the comparator:

$$G_{PWM} = \frac{1}{V_p} \qquad (6)$$

As we assume a 2-V peak amplitude for the sawtooth, the attenuation is 0.5 corresponding to a –6-dB gain.

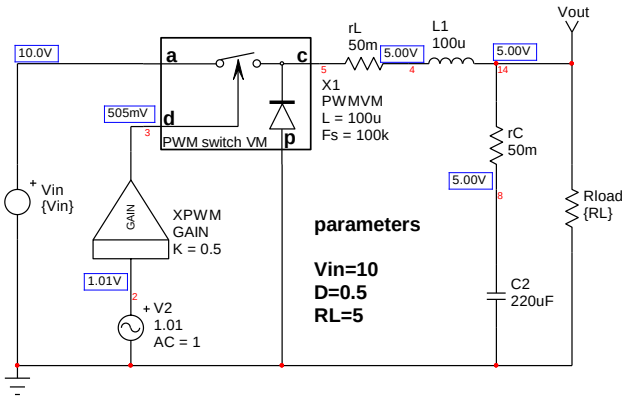

Fig. 7. The PWM switch lends itself very well to average-simulating switching converters such as a buck in this example.

Once the simulation is run, you can display the operating points and verify they are correct. This is an important step to check that the converter operates properly and the delivered results can be trusted. Here, the model delivers 5 V across the 5-Ω load and that is what we wanted. We can plot the results as shown in Fig. 8.

The peaking in the magnitude response indicates a strong quality factor *Q*. This variable is representative of the circuit losses and depends on the overall efficiency. If you build the buck converter and plot its response, it is likely to be more damped than the one in Fig. 8. This is because the MOSFET $R_{DS(ON)}$, the various ohmic losses on the capacitor and the inductor plus the freewheel diode recovery losses, all contribute to the circuit losses and affect *Q*.

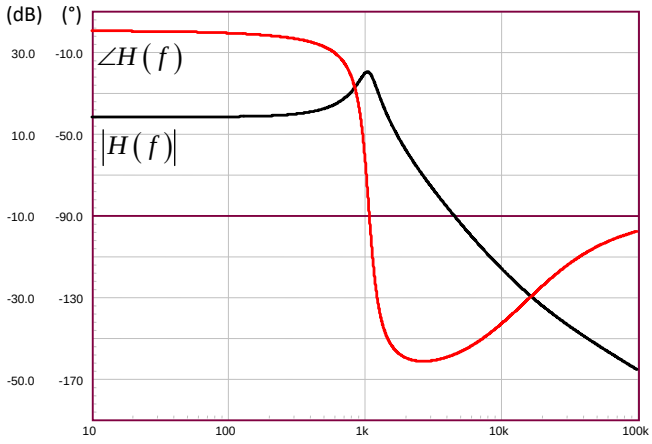

Fig. 8. The second-order response peaks at 1 kHz.

If the load now increases to 100 Ω, the model automatically transitions to DCM and delivers a new plot obtained with a duty ratio set to 31% for the same 5-V output. The updated response appears in Fig. 9 and confirms the disappearance of the peaking gain.

Unlike the results obtained with other approaches such as *state-space averaging* (SSA), the buck converter operated in DCM remains a second-order system but is affected by a low quality factor *Q*. This is obvious when looking at the phase which in a first-order model would reduce to zero at high frequency but keeps going down until it touches -180°. The response is thus made of low- and high-frequency poles while the output capacitor together with its equivalent series resistance (ESR) contributes a zero in the transfer function.

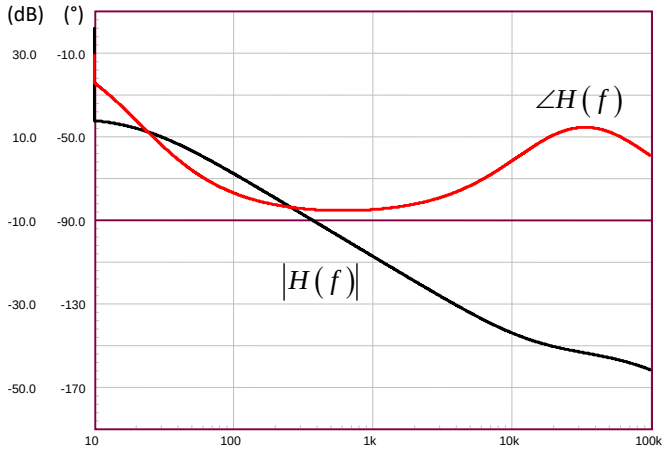

Fig. 9. When operated in DCM, the VM buck converter is still a second-order system.

SPICE simulations represent another viable option to plot the control-to-output transfer function of the converter you want to stabilize. However, while it faithfully models the effect of the parasitics (inductor and capacitor ESRs for example), it does not tell you what term in the transfer function these stray elements affect. It is extremely important to understand the impact of a given component on the dynamic response as you need to neutralize its deleterious effects through an adequate compensation strategy.

Besides Monte Carlo or sensitivity analysis, which can take a lot of computation time, the best way to understand the impact of a component on the response is to determine the control-to-output transfer function from a small-signal model. Such a model appears in Fig. 10. This time, we have selected a buck converter operating under current-mode control (CM). Its study can be carried out with the CM PWM switch, which lends itself very well to this type of analysis.[6,7] The model predicts subharmonic oscillations due to an unstable current loop gain. By adding some slope compensation, it is possible to reduce the current loop gain and stabilize the converter efficiently.

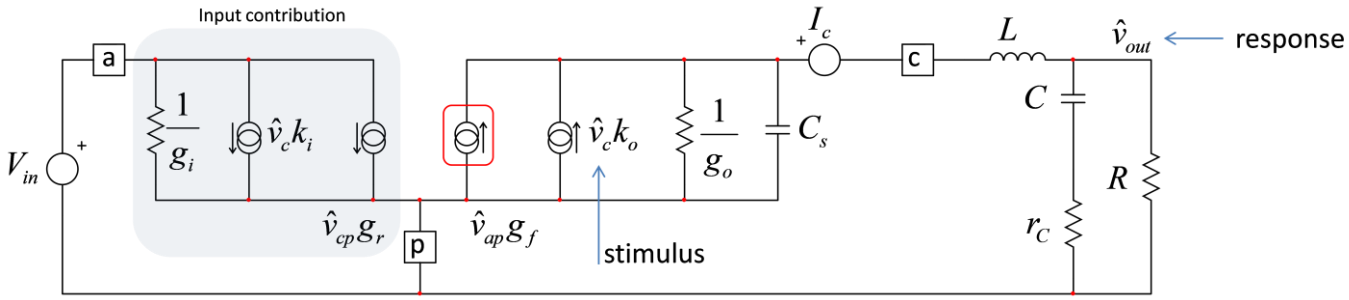

Fig. 10. The CM buck converter in small signal is described by a third-order model.

Counting the number of energy-storing components having an independent state variable gives us the order of this converter: it is a third-order circuit and we want the control-to-output transfer function with V_c the stimulus and V_{out} the response.

Numerous ways exist to determine the expression linking V_c to V_{out} but, in my opinion, none can beat the fast analytical circuits techniques or FACTs.[4] They not only represent the fastest way to go compared to classical node/mesh analysis they also yield the so-called *low-entropy* result. The numerator and the denominator naturally appear in a formalized form once the analysis is done. The obtained results thus provide immediate insight on the transfer function: where the poles and zeroes are and what parameters affect them.

Again, knowing the parameter at play in the definition of a zero or pole will let you efficiently fight its natural variability in production. Ray Ridley has derived the control-to-output transfer function of the CM buck including subharmonic poles located at $F_{sw}/2$ in his doctoral dissertation.[8] It is given below:

$$H(s) \approx H_0 \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \frac{1}{1+\frac{s}{\omega_n Q}+\left(\frac{s}{\omega_n}\right)^2} \tag{7}$$

where

$$H_0 = \frac{R}{R_i} \frac{1}{1+\frac{RT_{sw}}{L_2}\left[m_c(1-D)-0.5\right]} \tag{8}$$

$$\omega_p = \frac{1}{RC_3}+\frac{T_{sw}}{L_2C_3}\left[m_c(1-D)-0.5\right] \tag{9}$$

$$\omega_z = \frac{1}{r_C C_3} \tag{10}$$

$$\omega_n = \frac{\pi}{T_{sw}} \quad Q = \frac{1}{\pi\left[m_c(1-D)-0.5\right]} \tag{11}$$

In these expressions, the term m_c relates to the amount of external slope purposely injected in the modulator to reduce the current loop gain. Here m_c is defined as follows:

$$m_c = \frac{S_e}{S_n}+1 \tag{12}$$

S_e represents the external slope expressed in [V]/[s] while S_n denotes the inductor on-time slope also expressed in [V]/[s] via a scaling brought by R_i, the sense resistor. For a buck converter the inductor upslope is determined by:

$$S_n = \frac{V_{in} - V_{out}}{L_1} R_i \qquad (13)$$

For m_c = 50%, it can be shown that the audio susceptibility of the CM buck converter is nulled in theory.

With equation (7) on hand, it becomes possible to plot the power stage's dynamic response and see where to place the crossover frequency. Fig. 11 represents the response in which you can clearly see the peaking at half the switching frequency.

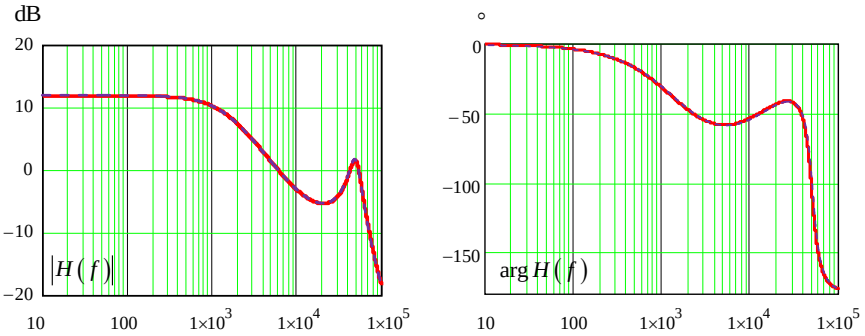

Fig. 11. The gain is flat at dc and drops with a –1-slope until it peaks at $F_{sw}/2$.

We have seen how average simulations and equations-based results can deliver the power stage response we need. A third option consists of using a simulator capable of delivering a small-signal response from a switching circuit. Such program is called a piece-wise linear (PWL) simulator.

SPICE is a linear solver in essence and any nonlinear behavior must be linearized around a suitable operating point. That particular point is found by reducing the simulation step until convergence is achieved. A nonlinear element such as a diode for instance, must be replaced by a linear approximation point by point during the simulation. This process not only heavily loads the computer but it often engenders convergence errors when the timestep reduction algorithm hits a lower limit.

On the other hand, a simulator like SIMPLIS employs a PWL engine and can extract the ac response from a switching circuit. Fig. 12 shows how a diode is typically modeled.

Fig. 12. SIMPLIS uses perfect elements described by linear segments.

You can see how the segments describe the forward drop increase in relationship with the diode current. They advantageously replace the exponential Shockley equation describing the current in a diode. Regardless of the diode operating point, the behavior is always linear and only the slope changes. That way, there is no need to apply an extra linearization algorithm because the circuit is always linear. An ac modulation can thus be applied as a stimulus to a switching circuit from which a small-signal response is obtained.

A typical LLC converter is represented in Fig. 13. The high- and low-side MOSFETs are operated exactly at a 50% duty ratio in this new current-mode control approach implemented by the NCP13992 current-mode resonant controller. The high-side transistor turns on and remains in this state until the peak inductor current meets the target imposed by the feedback loop.

When the high-side transistor turns off, the low-side transistor activates for an off-time duration precisely duplicating the former t_{on} duration to ensure a perfect 50% duty ratio. The proposed circuit in Fig. 13 is a simplified version of this complex control section but it allows the complete simulation of the circuit using Elements, the demonstration version of SIMPLIS.

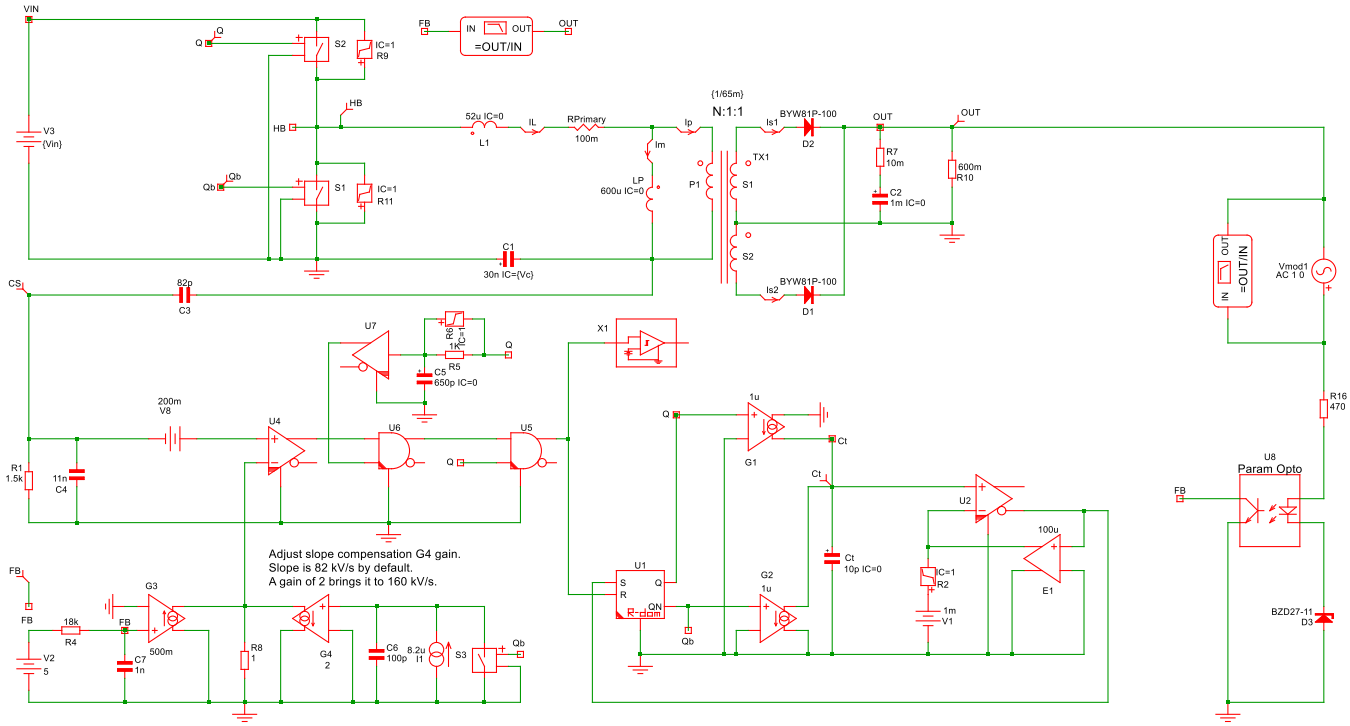

Fig. 13. SIMPLIS uses perfect elements described by linear segments.

After a few tens of seconds, the simulator not only delivers the cycle-by-cycle waveforms—you can then check RMS, average or peak values for instance—but also the control-to-output transfer function. These two results appear in Figs. 14 and 15.

This is interesting because you do not need to resort to an average model and you can explore second- or third-order effects like changes in $R_{DS(ON)}$ and immediately see the effects on the transfer function. Equation-based models exist for the LLC converter but they are, in my opinion, difficult to use considering their complexity and the heavy math they involve. Having access to simulation data mixing transient and small-signal results in a small amount of time is really a useful approach.

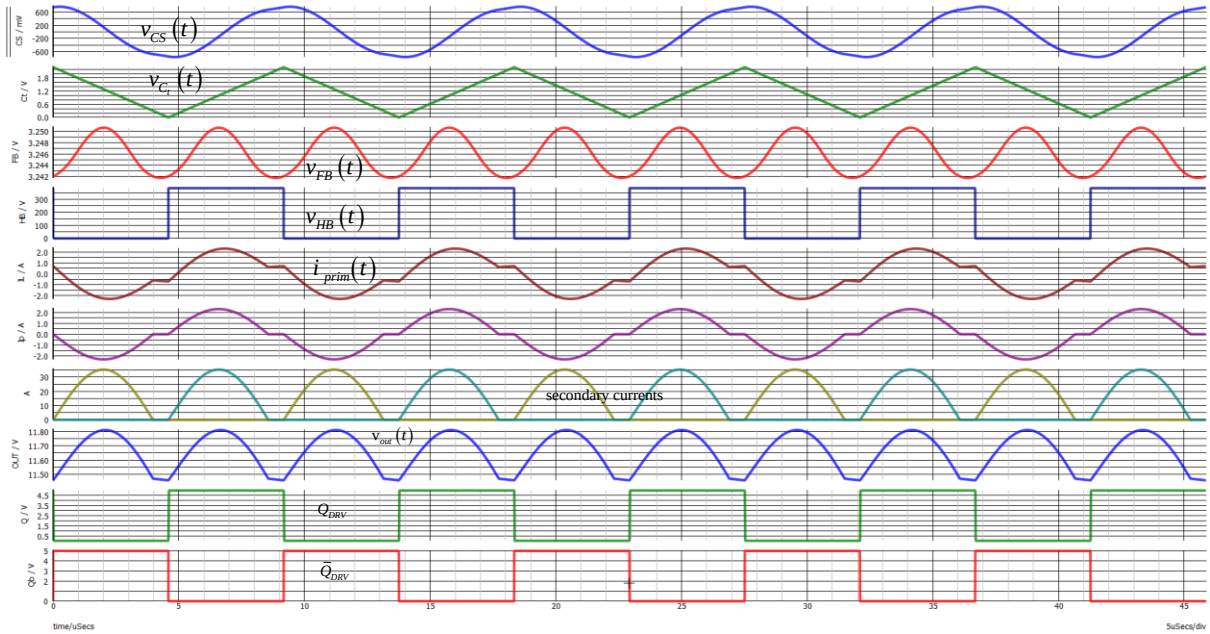

Fig. 14. The cycle-by-cycle simulation confirms the correct operating point, a 24-V output.

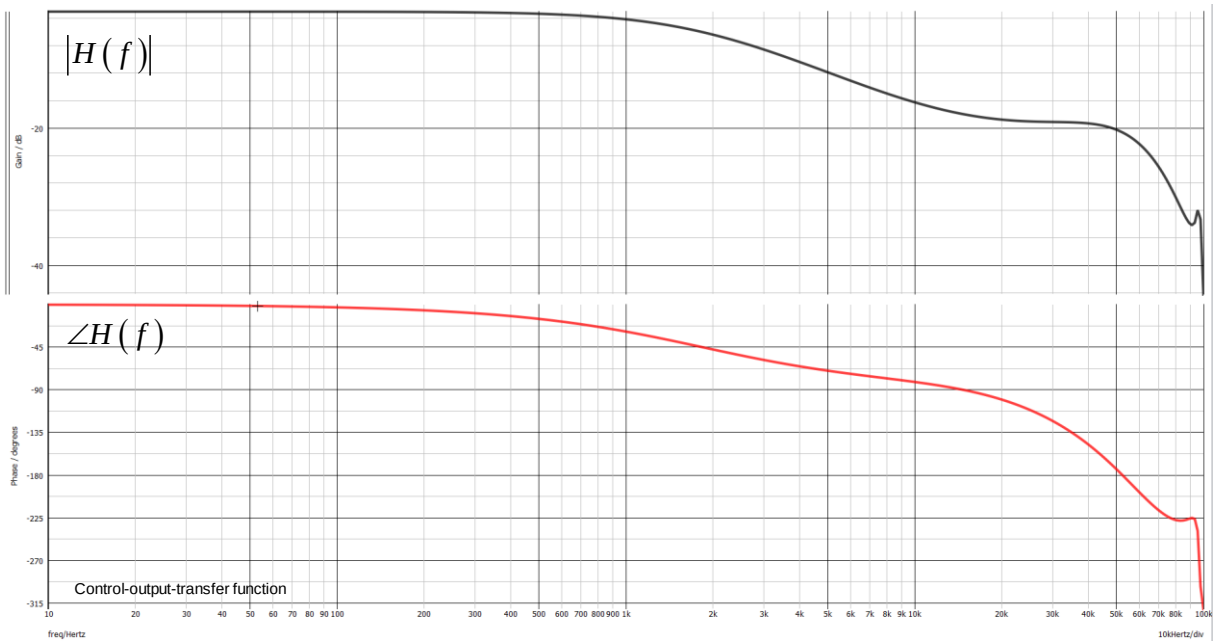

Fig. 15. The control-to-output transfer function is obtained immediately after the periodic operating point (POP) calculation.

Selecting Crossover Frequency And Phase Margin

Now that we have the transfer function of the power stage, it is important to select and apply the compensation strategy. The first question is how to select the crossover frequency f_c and the phase margin? Literature abounds with recommendations ranging from one-fifth to one-tenth of the switching frequency F_{sw}. If the upper

crossover limit is obviously $F_{sw}/2$ for any converter, there are other boundaries imposed by the adopted topology.

Buck-Derived Topologies

There is a resonant frequency f_0 imposed by the *LC* network. If you look at the power stage control-to-output transfer function in voltage-mode control, the gain peaks at f_0. Consequently, the loop must exhibit some gain at this frequency so that correction of any oscillation can occur. It is therefore a good practice to select f_c at least 3x to 5x the resonant frequency.

In current-mode control, the situation simplifies as the response is of the first-order type at lower frequencies. It can however peak at $F_{sw}/2$ because of undamped subharmonic poles. Slope compensation is then necessary to tame these poles and the converter gains in stability.

Buck-Boost Derived Topologies

In these structures, the energy is transferred in a two-step process. You first store energy in the inductor during the on-time then you release it to the load during the off-time. In case of a sudden output power demand, the converter cannot instantaneously react as the inductor needs more cycles to increase energy storage. This inherent delay in the response materializes as a right-half-plane zero (RHPZ) in the control-to-output transfer function.

A RHPZ provides an increase in magnitude (as any zero would) but the phase lags. It is the opposite of a left-half-plane zero whose phase leads. When you have a RHPZ in your transfer function, the power stage phase further degrades as you approach its position. It is therefore recommended to crossover well before the RHPZ occurrence.

A good rule is to set the upper f_c limit at 20% to 30% of the lowest RHPZ position (obtained for the maximum current and the minimum input voltage). This statement is true for both VM and CM control methods as the RHPZ occupies the same location. In VM you have to follow the buck rule which is to select an f_c greater than 3x to 5x f_0 but, this time, f_0 varies with the duty ratio which complicates the final choice.

Boost Topology

The behavior of this topology is almost the same as with the buck-boost described above. There is a RHPZ and a resonance in voltage-mode control. In current-mode control, there is a little more flexibility than in VM because you do not have the peaking at f_0 but the RHPZ bounds the upper limit of f_c anyway. If you want bandwidth with the boost or buck-boost converter, it is better to reduce the inductance value so that the converter can respond faster to a sudden output power demand.

All of these recommendations are summarized in the table. Please note that pushing the crossover frequency too high when the topology permits is not a wise decision either. This is because having a wide bandwidth is like opening a funnel: the converter is indeed faster but becomes more sensitive to external perturbation and noise: tailor f_c to meet certain transient specifications but do not push it beyond this value.

Selection of the open-loop phase margin depends on the type of transient response you need. If you want a fast response and can accept a bit of overshoot, a phase margin in the vicinity of 50° is adequate. If you want to play it more conservative and have a slower response (or recovery) without overshoot, then 70° to 80° represents a good number to start with. You can link the *open-loop* phase margin φ_m to the *closed-loop* quality factor Q_c by the graph shown in Fig. 16. This is a theoretical approach which describes how a second-order system featuring a pole at the origin and a high-frequency pole (no zeroes) behaves once it operates under closed-loop conditions.

Table. You cannot arbitrarily select the crossover frequency as it depends on the adopted topology. (Continuous conduction mode is assumed.)

Topology	Voltage mode	Current mode
Buck	$3 \cdot f_0 < f_c < F_{SW}/2$*	$f_c < F_{SW}/2$*
Boost	$3 \cdot f_0 < f_c < 0.3 \cdot f_{RHPZ}$	$f_c < 0.3 \cdot f_{RHPZ}$
Buck-boost	$3 \cdot f_0 < f_c < 0.3 \cdot f_{RHPZ}$	$f_c < 0.3 \cdot f_{RHPZ}$

*Theoretical upper limit

It is important to understand that phase margin selection depends on your application but also on the limits you can accept. For instance, if your converter will experience large temperature values (-40°C to 80°C of ambient for instance), then it is better to select a high margin (80° to 90° or even more) for instance and see how low it goes in a worst-case situation. Too low of a phase margin and the response may ring unacceptably and possibly trip the protection features. A value of 40° is an adequate absolute lowest value in my opinion.

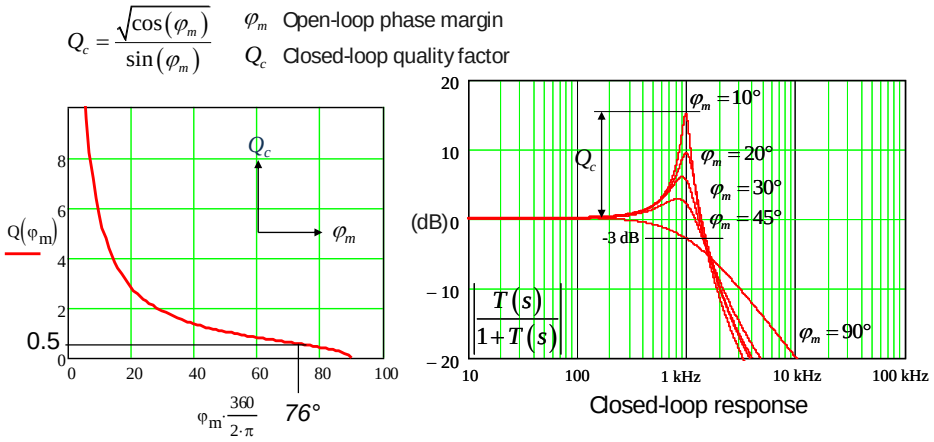

Fig. 16. The open-loop phase margin dictates how the converter will react once the loop is closed.

If your power supply operates in a room in which the ambient temperature never exceeds 35°C and never drops below 0°C (most consumer products), then perhaps less aggressive targets will be easier to meet. Once the design is frozen, you must go through extensive experiments (e.g. Monte Carlo or worst-case analysis) and make sure the phase margin never drops below the 40° level in corner simulations.

As highlighted in the literature, having a large phase margin will slow down the recovery but will also reduce the gain at low frequency, hampering the converter to reject low-frequency perturbations (the 120-Hz ripple for an ac-dc switcher). The graph below shows a typical transient response with two different phase margins at a constant crossover frequency (Fig. 17).

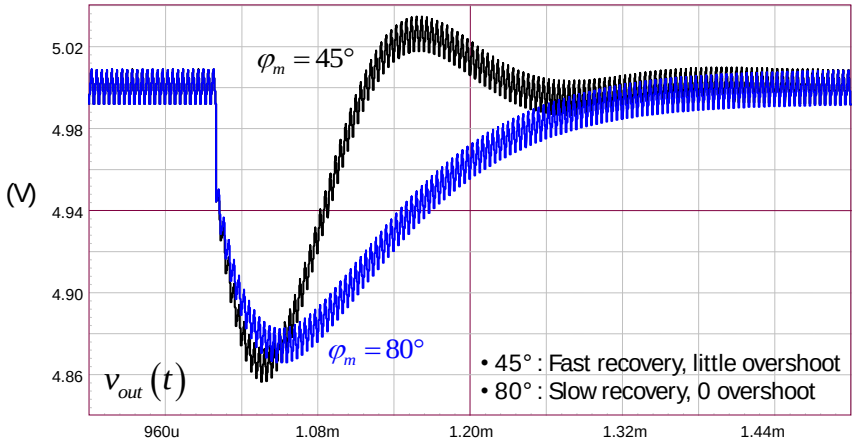

Fig. 17. Too large a phase margin affects the recovery time (f_c is constant).

The gain margin depends on the variations in open-loop gain your system will experience during operation. Depending on the error amplifier's open-loop gain variations (due to manufacturing processes, temperature and so on), whether there is input feedforward or not, etc., the loop-gain magnitude can shift up and down affecting the crossover frequency. Typically, a gain margin of 15 to 20 dB is considered a conservative value leading to rugged designs.[9]

A Design Example: Stabilizing An AC-DC Flyback

I have selected an ac-dc adapter project to illustrate how the above guidelines could be applied. The converter we want to stabilize delivers 2.8 A from a 19.5-V output and its schematic diagram appears in Fig. 18.

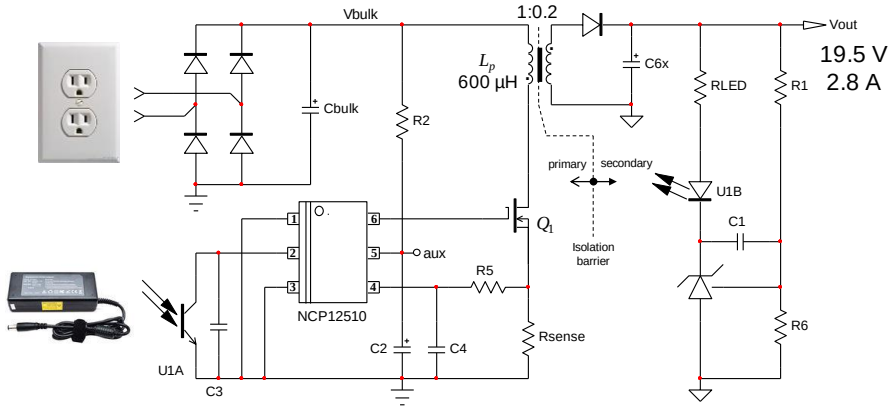

Fig. 18. This ac-dc converter delivers 2.8 A and uses a TL431 for the feedback loop.

This flyback converter is supplied from the rectified mains via a diode bridge and a bulk capacitor. Considering the sinusoidal input, the rectified dc voltage feeding the flyback is expected to be that of Fig. 19. You can see that the voltage at the lowest line input (90 V) peaks to around 120 V but drops to 52 V in the valley. The converter must deliver the full power at this lowest input otherwise the overload protection might trip or an unacceptable ripple can appear at the output.

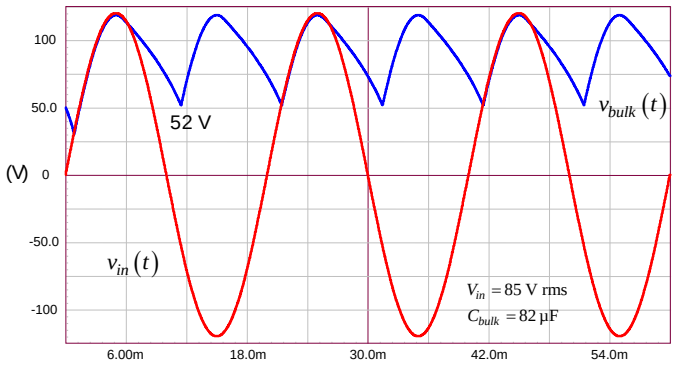

Fig. 19. This ac-dc converter is supplied from a dc input affected by a large voltage ripple.

The first thing we need is the control-to-output transfer function at the lowest input level. It can be obtained using the SIMPLIS circuit shown in Fig. 20. Without any slope compensation, we expect a response peaking at half the switching frequency resulting from the heavy CCM operation at a 52-V input. Because SIMPLIS needs to find a periodic operating point (POP) before launching the ac analysis, I had to add some compensation ramp to let it properly converge (in addition to that needed to prevent subharmonic oscillations).

The extra ramp can be generated from the low-impedance drive pin with an *RC* network. If the time constant of this network is larger than the switching period, the obtained ramp is quite linear and well adapted for compensation purposes. The cycle-by-cycle and ac results appear in Fig. 21.

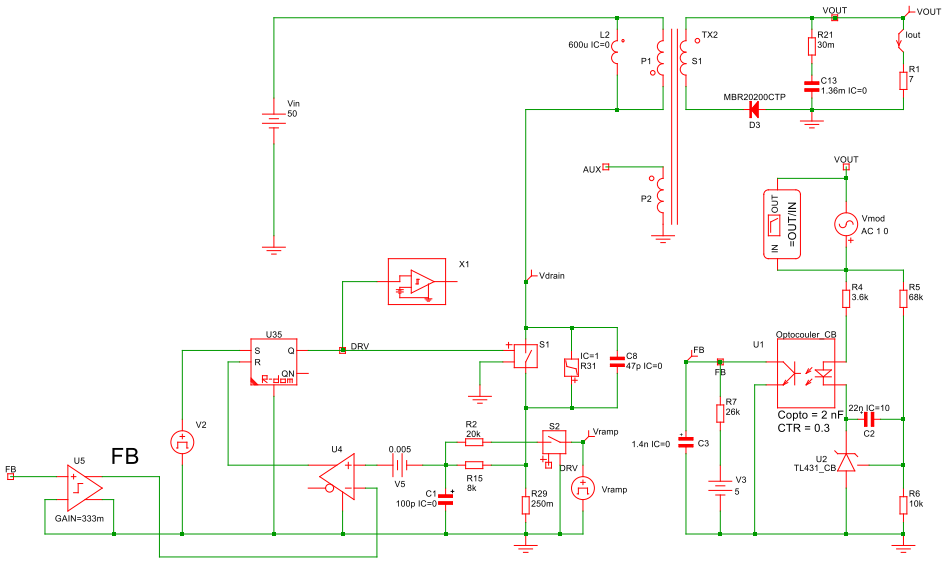

Fig. 20. SIMPLIS will confirm the operating point and delivers the power stage small-signal response we need.

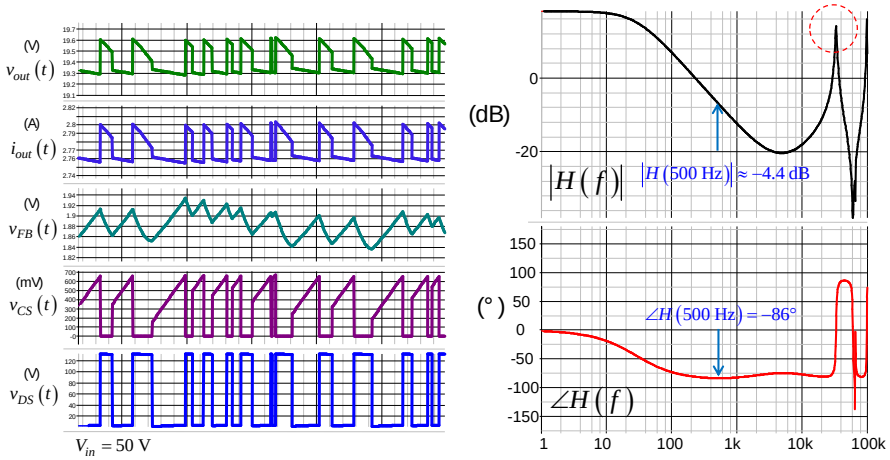

Fig. 21. The simulation confirms the instability linked to the heavy CCM operation.

Calculations reveal a negative *Q* factor for the double poles indicating a location in the right half-plane: no wonder the switching pattern is highly unstable. To select the crossover frequency, we need to know where the right-half-plane zero is located. With such a low input voltage, it won't give us a lot of bandwidth:

$$f_{z_2} = \frac{(1-D)^2 R_{load}}{2\pi D L_p N^2} \approx 1.6\text{ kHz} \qquad (14)$$

where *N* is the transformer turns ratio 1:*N*, *D* is the operating duty ratio, L_p is the transformer primary inductance and R_{load} is the load resistance.

If we limit ourselves to 30% of this f_{z2} value then 500 Hz for f_c seems reasonable. To obtain a better value, you have the choice to either increase the bulk capacitor and increase the valley voltage to 70 V for instance or reduce the primary inductance Lp. You will push the RHPZ to a higher location but will pay for it by increasing the conduction losses resulting from the larger ripple.

Extracting data at 500 Hz from the power stage Bode plot shows an attenuation of 4.4 dB and a phase lag of 86°. We can determine the phase boost we need (to correct the lag and bring some phase margin) for a 70° margin goal:

$$boost = \varphi_m - \angle H(f_c) - 90° = 66° \qquad (15)$$

The *k*-factor lends itself well to stabilizing current-mode power supplies and we can determine where to place the pole and the zero for a type 2 compensator. First, we determine the value of *k*:

$$k = \tan\left(\frac{boost}{2} + \frac{\pi}{4}\right) = 4.7 \qquad (16)$$

The zero will thus be placed at:

$$f_z = \frac{f_c}{k} = \frac{500}{4.7} \approx 106\text{ Hz} \qquad (17)$$

while the pole will land at:

$$f_p = k \cdot f_c = 500 \times 4.7 \approx 2.3\text{ kHz} \qquad (18)$$

The gain we want to compensate for the 4.4-dB deficit at 500 Hz depends on the LED series resistance[2] and the optocoupler current transfer ratio or CTR:

$$G_0 = \text{CTR}\frac{R_{pullup}}{R_{LED}} = 10^{\frac{-G_{fc}}{20}} = 10^{\frac{4.4}{20}} = 1.66 \qquad (19)$$

Using the values we have on hand from the design example, we find a R_{pullup} resistance of 3.6 kΩ. You must verify that this resistance is compatible with the biasing conditions necessary to bring the controller feedback pin low in worst-case operation.

Finally, the high-frequency pole f_p is placed by adjusting the capacitance across the optocoupler. Please note that this optocoupler must be properly characterized to know where its low-frequency pole is located.[2] Once all components are selected, we can independently test the TL431-based compensator as shown in Fig. 22 .

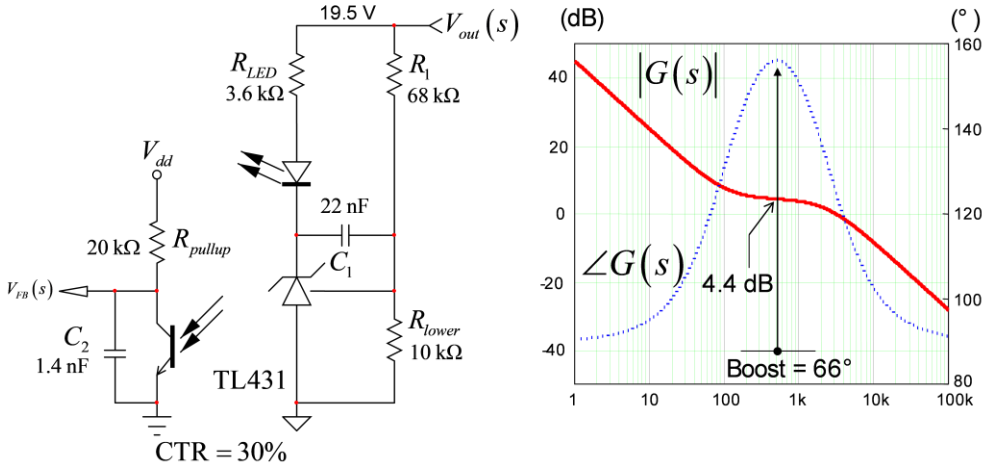

Fig. 22 . The type 2 compensation shows the expected phase bump at 500 Hz.

Once this step is done, the SIMPLIS template of Fig. 20 lets you check the crossover frequency at various input voltages. As confirmed by Fig. 23, the phase margin obtained at input voltage extremes is very comfortable. As soon as the input voltage increases to 120 V, the crossover extends to almost 1 kHz which should benefit the reaction speed.

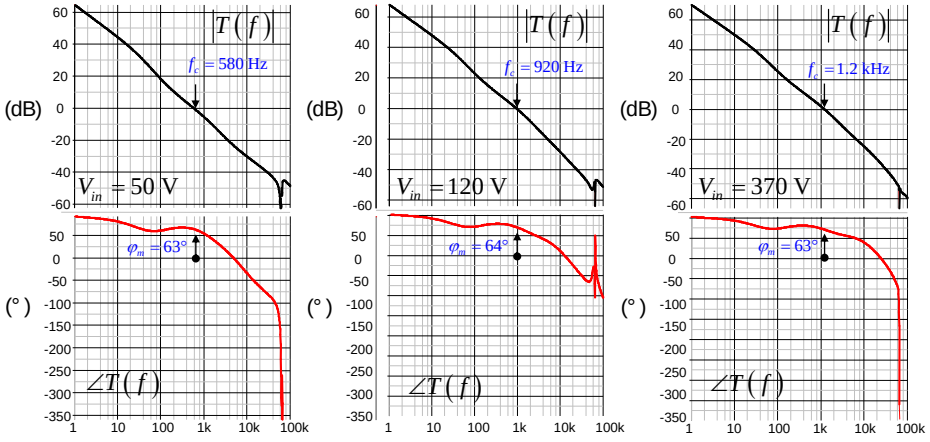

Fig. 23. The compensation strategy leads to excellent phase margins at input voltage extremes.

Once the compensation is implemented, output transient load steps are performed and you can check the response. This is what is shown in Fig. 24. The undershoot is well under control and there is no overshoot upon recovery. The next step is to build the prototype and verify the loop response on the bench with a network analyzer.

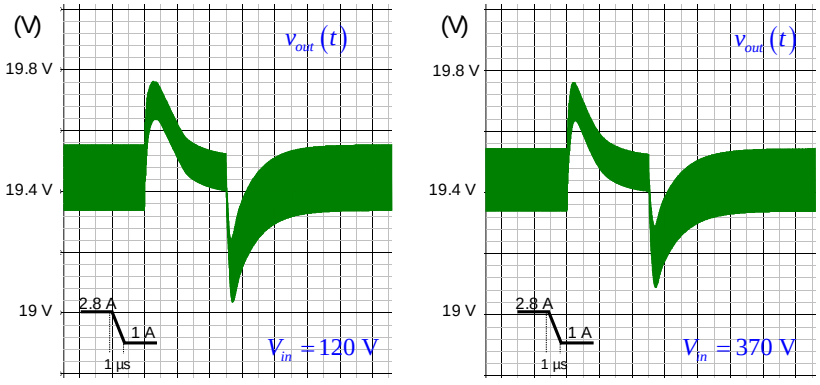

Fig. 24. The transient response shows a stable output waveform under low- and high-line conditions.

This practical test is essential and cannot be skipped. It will tell you if the hypothesis you made when modeling the converter and its compensation circuitry are confirmed by a real board measurement. Feeding the model back with these experimental results will let you conduct worst-case analyses on the computer and be confident it corresponds to reality.

Conclusion

This article has detailed the various ways to design the compensation section of a switching converter. It starts with the control-to-output transfer function of the power stage, which can be obtained by following different paths: simulation with an average model, deriving small-signal equations or using a piece-wise linear simulation engine like SIMPLIS.

Once a working simulation template complies with the phase and gain margins you have set, it is important to compare your results with those obtained from a prototype on the bench. Parameter sweeps, Monte Carlo and worst-case analysis will then be conducted on a validated model to ensure that you release a sound and rugged product to market.

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About The Author

Christophe Basso is a technical fellow at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "Linear Circuit Transfer Functions: An Introduction to Fast Analytical Techniques."

Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 25 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on power supply compensation, see the How2Power Design Guide, and do a keyword search on "compensation."