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The Engineer's Guide To EMI In DC-DC Converters (Part 15): Differential-Mode Input Filter Design

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Due to their high efficiency, small solution size and low component count, you'll find modern dc-dc converters in almost all electronic systems in the automotive, communications infrastructure, enterprise/data center and industrial sectors. Yet these converters generate substantial conducted electromagnetic interference (EMI), both differential mode (DM) and common mode (CM), as a side effect of high-frequency and high-edge-rate switching.

The challenges related to EMI issues have become distinctly more evident in recent years, especially with the continuous increase in switching frequencies driven by the availability of conventional and wide-bandgap power devices with short commutation times. EMI filter solutions can help ensure both the reliability and electromagnetic compatibility (EMC) of the system.

As discussed in parts 12 and 13 of this article series,[1-14] DM noise relates to the switched input current of the converter, whereas CM noise arises from capacitive coupling of the high transient voltage switching node(s) to the measurement ground plane, which along with the line impedance stabilization network (LISN) is part of the conducted EMI measurement setup. Part 3 presented an analysis showing that a decrease in switching time, while beneficial for converter power losses, leads directly to an increase in the EMI spectrum.

Moreover, faster switching triggers critical oscillations within the switched voltage and current waveforms—from parasitic elements related to the circuit layout, passive components and the power devices themselves—and further influences the EMI spectral content. Such oscillations typically occur at frequencies above 50 MHz, where filtering is more difficult. Collectively, these trends exacerbate the burden on EMI management components.

This article reviews theoretical concepts related to input filter design to minimize DM noise specifically, including selecting the filter topology, estimating the required filter attenuation and calculating the filter component values. A simulation provides the expected attenuation based on an input filter for conducted emissions (CEs) from an automotive synchronous buck converter.

Passive EMI Filtering

Occupying 25% to 50% of the total converter solution size, a compact and efficient EMI filter implementation is one of the most critical challenges in high-density dc-dc converter designs. The input filter plays three important roles:

- It ensures an almost dc input current by filtering the input current waveform to remove the ac harmonic content.
- It prevents both DM and CM EMI generated by the switching source from reaching input power lines and affecting adjacent equipment (for example, onboard radio receivers in automotive applications).
- It protects the converter and its load from incoming disturbances including line voltage transients (especially those applicable to automotive and industrial type inputs), surges, dips and bursts. Within this context, see ISO 7637-2[15] and ISO 21780,[16] which describe voltage transients in automotive systems for 12 V and 48 V, respectively.

As an introduction, Fig. 1a presents a conventional π-stage EMI filter for a dc-dc converter with DM and CM sections. Parts b and c of Fig. 1 show the corresponding DM and CM equivalent filter circuits[2] in order to simplify the analysis, assuming a symmetric design without mixed-mode noise contribution. These figures can help you understand the requisite attenuation as a first step toward EMI filter design.

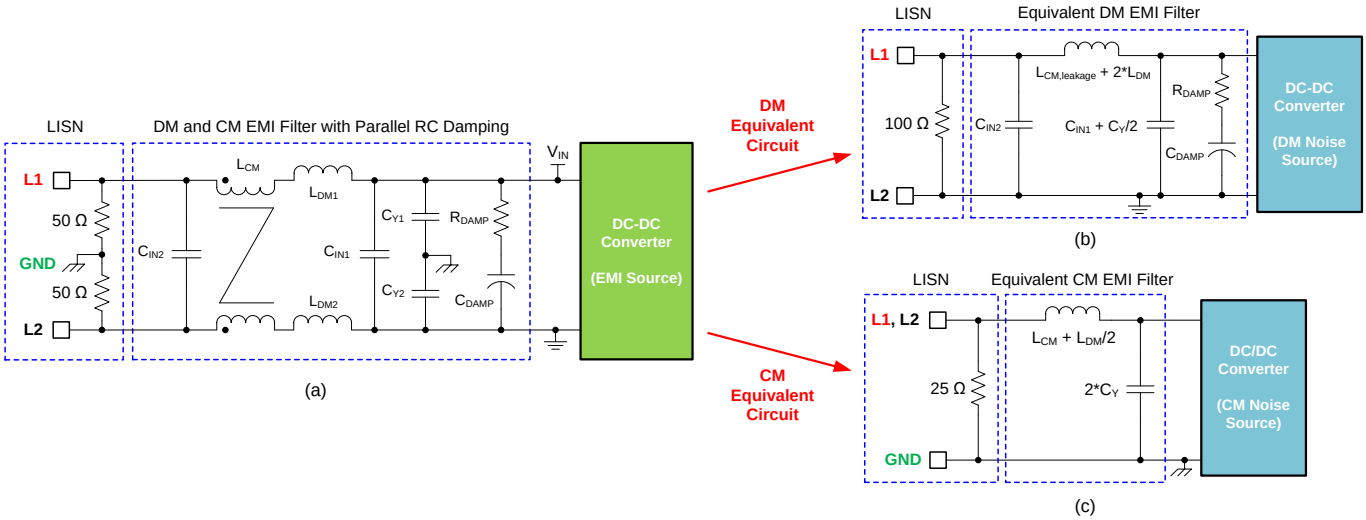


Fig. 1. An integrated DM and CM passive EMI filter with discrete components (a) and its equivalent circuits for DM (b) and CM (c) noise currents.

The design of such filters for use in power electronics applications is challenging, as the filters terminate with varying impedances, both noise source (switching converter) and load (LISN and EMI receiver). The effective load impedances of the filters shown in Fig. 1b and 1c correspond to the 100 Ω (DM) and 25 Ω (CM) presented by the measuring LISNs.[12, 13]

The DM inductances L_{DM1} and L_{DM2} in Fig. 1a are the leakage inductances of the two coupled CM windings or discrete DM inductances. C_{IN1} and C_{IN2} are DM filter capacitors, while C_{Y1} and C_{Y2} designate CM filter capacitors assuming a three-wire system (where a chassis ground connection is available).

The primary design targets and objectives for input filter design should be to:

- fulfill international EMC standards related to conducted emissions in terms of DM and CM noise attenuation,
- provide sufficient passive filter damping to reduce the peak output impedance, thus ensuring system stability and minimizing control design restrictions,
- limit the physical size and stored energy of the filter components,
- minimize the total filter cost.

Sufficient passive damping—without a major increase in the filter volume and a decrease in the high-frequency attenuation—is important for practical operation. Damping is not the primary task in the DM filter design presented here, however, given its earlier treatment in parts 10 and 11.

Terminal Impedances And Impedance Mismatching

Because EMI filters are basically impedance mismatching networks and thus require an estimation of the expected impedances connected at their input and output terminals, the actual variation of noise source[17] and load impedances versus frequency (for both DM and CM) affects EMI filter performance.

The output impedance of the filter and the noise source impedance of the converter, as well as the input impedance and load impedance of the filter, need proper mismatching. As shown in Fig. 2, the LISN and supply lines define the filter load impedance Z_{load} during a practical EMI measurement, while the source impedance Z_{source} corresponds to the DM or CM noise-source impedance of the converter system.

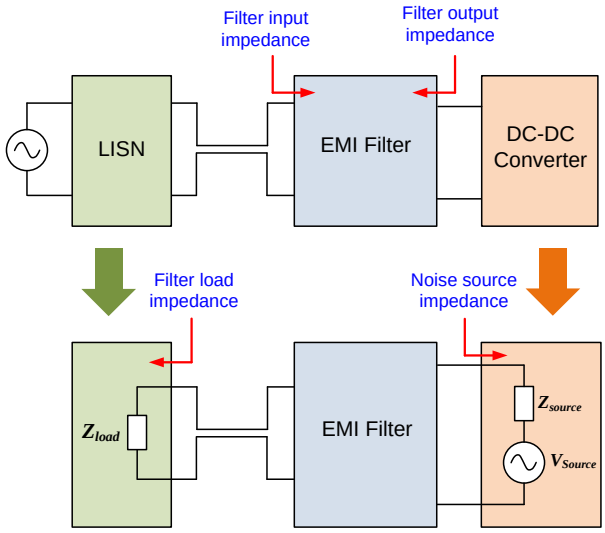
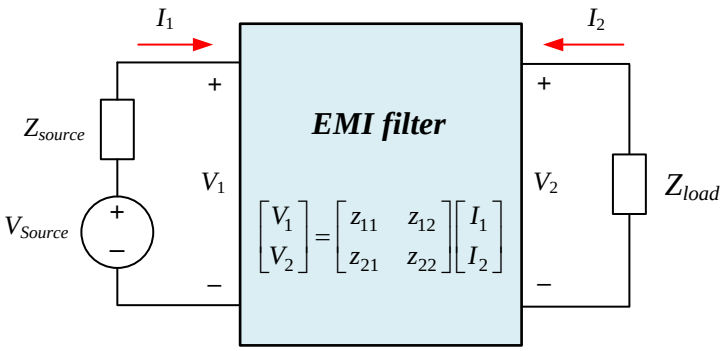


Fig. 2. An EMI filter two-port equivalent network with the load impedance Z_{load} defined by the LISN, and a model of the converter containing an equivalent noise-source voltage V_{source} and noise-source impedance Z_{source}.

Representing the EMI filter as a two-port equivalent network[18] with its z-parameter impedance matrix, as shown in Fig. 3, equation 1 shows the dependence of the actual filter attenuation corresponding to the in-circuit insertion loss (IL) on the terminal impedances denoted as Z_{source} and Z_{load}.

$$\mathrm{IL} = 20\log\left[\frac{(Z_{source}+z_{11})(Z_{load}+z_{22})-z_{12}z_{21}}{(Z_{source}+Z_{load})z_{21}}\right] \qquad (1)$$



$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

Fig. 3. EMI filter represented by an impedance network of z-parameters.

Designing input filters without considering the actual source impedance of the dc-dc converter results in a deviation between the actual filter insertion loss value and the expected value (based on the intrinsic filter attenuation capability derived from its voltage transfer function). Circuit simulation of the dc-dc converter and EMI filter is thus an important tool to predict and confirm attenuation performance before in-circuit validation.

Filter Topology Selection

A general sense of impedance mismatching[19] facilitates filter component design and topology selection to meet the requisite attenuation. Knowing at least the magnitude of the effective noise source and filter load impedances before proceeding with the filter parameter calculations is important for a preliminary selection of the most appropriate filter topology, according to the criteria shown in Fig. 4.

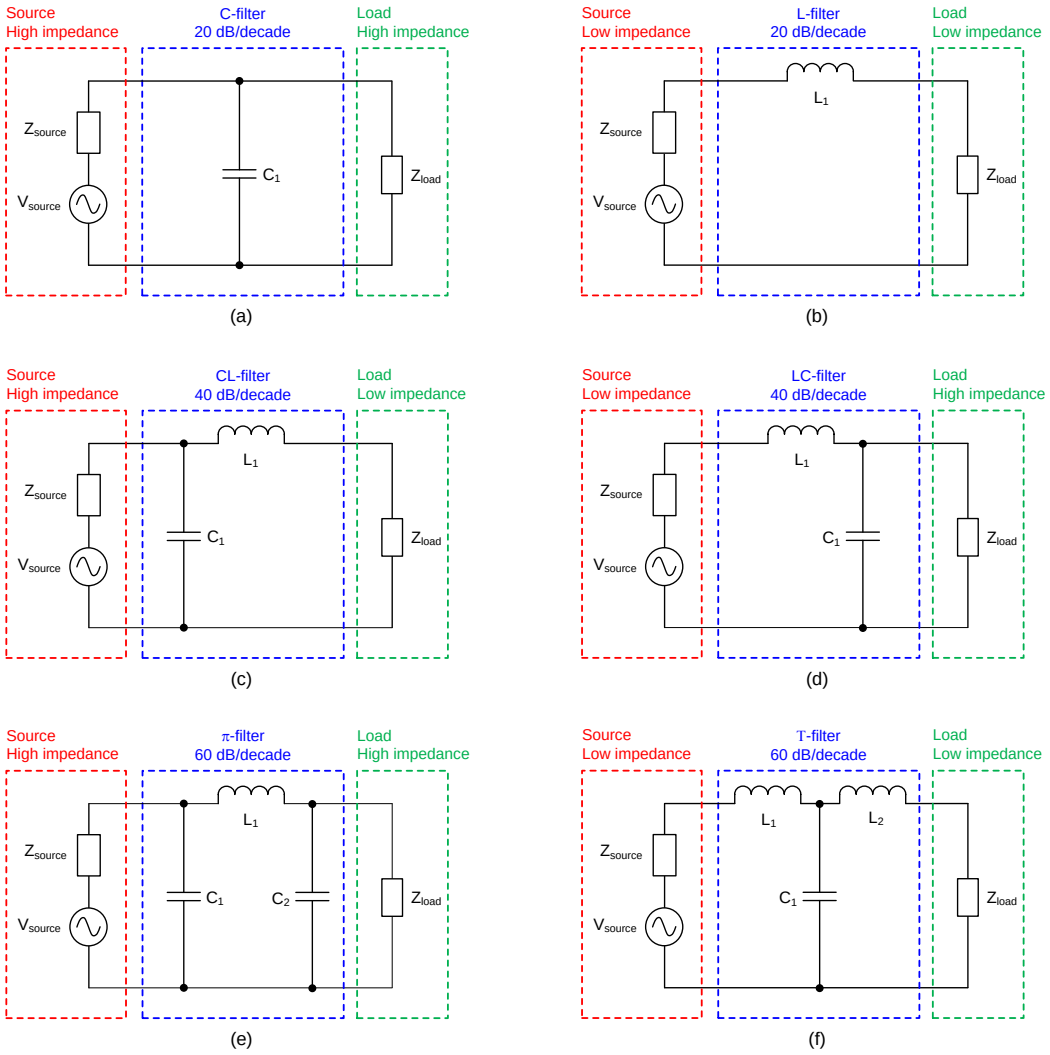


Fig. 4. Choice of filter topology based on impedance mismatch conditions: C filter (a), L filter (b), CL (or Γ) filter (c), LC filter (d), CLC π- filter (e) and LCL T-filter (f).

While a large number of DM filter topology options are theoretically available for EMI filtering, only a few are actually common, for reasons related to cost and complexity. For example, high (inductive) noise-source impedance typically characterizes a voltage-fed dc-dc converter. Meanwhile, the DM LISN load impedance of 100 Ω is also high on a relative basis. Thus, according to the criterion of maximum impedance mismatching, a Γ-filter or π-filter topology with low input and output impedances (see Fig. 4c and Fig. 4e) is a common choice for a DM filter.

DM Filter Design Workflow

The conventional way to design an EMI filter is to build a hardware prototype of the system with an initial filter implementation derived by approximate calculations and practical experience. Iterative EMI measurements and modification of the filter circuit will yield a final design (depending on the problematic frequencies) until the designs meets EMC standards with minimal filter component costs. Fig. 5 shows a simplified flowchart for a DM filter design to determine the values of its major components, with more detail described in the steps that follow.[20-22] Part 16 of this series will consider CM filter design.

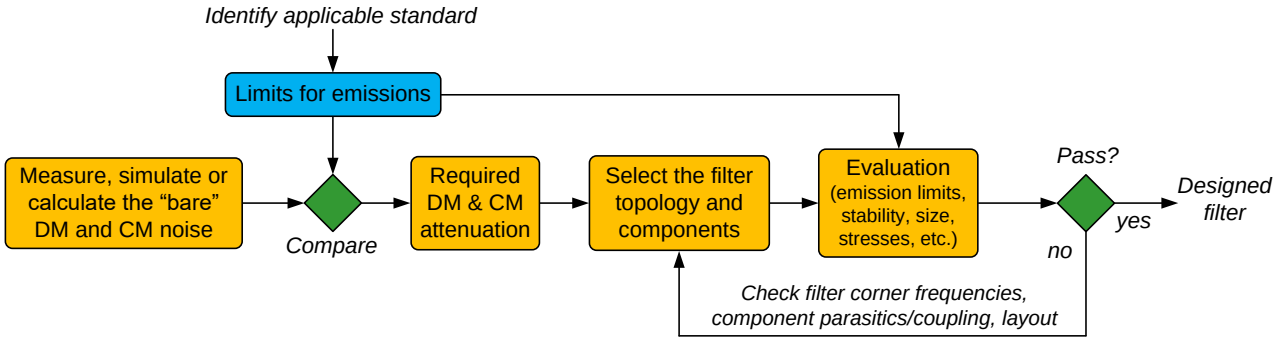


Fig. 5. EMI filter design procedure flowchart overview.

Converter Topology And Input Current Spectrum

Using an example of a synchronous buck converter with LISN and input filter as shown in Fig. 6a, let's analyze the current flowing into the input filter from the switching cell using the simplified circuit shown in Fig. 6b. I replaced all of the components placed downstream of the input filter with a periodically switching current source (given by equation 2) that has a quasi-rectangular waveform,[20] and whose amplitude is determined by the average load current and buck inductor ripple current:

$$i_{DM,buck}(t)=\begin{cases} I_{out}-\dfrac{\Delta i_{L\text{-}pp}}{2}+\dfrac{\Delta i_{L\text{-}pp}}{dT_s}t & 0\le t<dT_s \\ 0 & dT_s\le t<T_s \end{cases} \qquad (2)$$

where I_{out} is the output current of the buck converter, d is the duty cycle, $\Delta i_{L\text{-}pp}$ is the amplitude of the peak-to-peak inductor ripple current and $T_S = 1/f_S$ is the switching period.

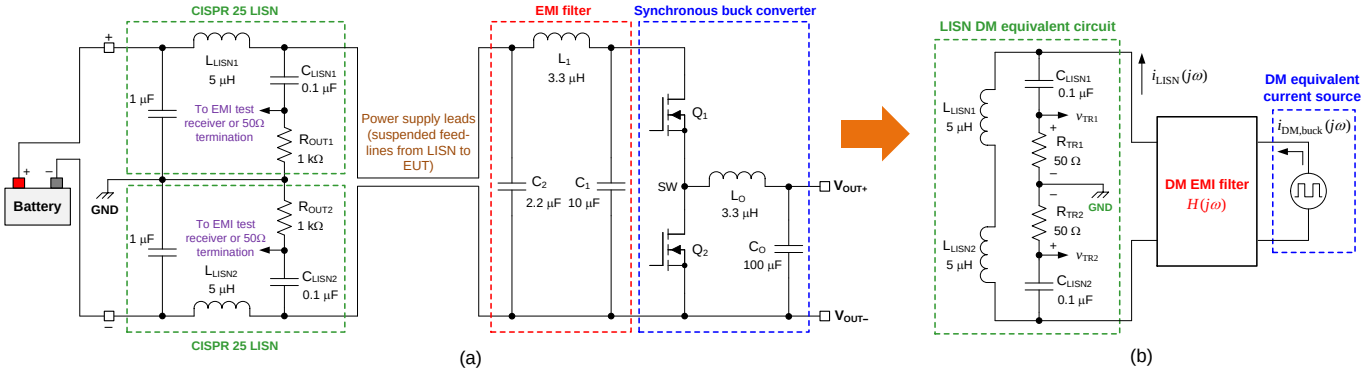


Fig. 6. Typical CISPR 25 CE measurement setup for a buck converter with input π-filter and LISN circuit connected on each supply line (a) and equivalent current source and LISN circuit for DM noise measurement (b).

Neglecting the rise and fall times of the current waveform, equations 3 and 4 represent the Fourier series for the DM input current and its filtered version for a buck converter, respectively:

$$i_{in,buck}(t)=I_{out}d+\sum_{n=1}^{\infty}\frac{2I_{out}}{n\pi}\sin(n\pi d)\cos(n\omega t) \qquad (3)$$

$$i_{LISN}(t) = H(0)I_{out}d + \sum_{n=1}^{\infty}\left|H(nj\omega)\right|\frac{2I_{out}}{n\pi}\sin(n\pi d)\cos\left(n\omega t + \angle H(nj\omega)\right) \qquad (4)$$

where $H(j\omega)$ is the DM filter transfer function[12] and n is the harmonic order. Equation 3 specifies the rolloff of input current harmonic amplitude with frequency as $1/n$, suggesting that the DM spectrum envelope of the rectangular current waveform has a decay rate of 20 dB per decade of frequency.

Determine The Required Filter Attenuation

When designing an input filter for fixed-switching-frequency converters, you'll want to determine the required attenuation using the lowest switching frequency harmonic that is within the frequency limits of the applicable EMI standard. As most standards for conducted emissions begin at 150 kHz, the filter components present very little parasitic effects at this frequency. And because you can initially neglect the computation of parasitic effects, you can employ simple models for the components and use analytical expressions with varying degrees of accuracy.

The amplitude of the first harmonic peak greater than 150 kHz leads to the required attenuation at the design frequency (i.e., the lowest frequency to be attenuated). This suggests that the fundamental is usually the most important frequency for DM filter design (or the second or third harmonic if the switching frequency is less than 150 kHz).

One option is to determine the *bare* noise measurement, which obtains the converter noise signature without a filter. You can calculate the required attenuation based on the measured result and applicable standard. Equation 5 gives the required filter attenuation, designated A_{dm}, as:

$$A_{dm}[\text{dB}] = A_{dm\text{-nofilter}}[\text{dB}\mu\text{V}] - A_{std}[\text{dB}\mu\text{V}] + m[\text{dB}\mu\text{V}] \qquad (5)$$

where $A_{dm\text{-}nofilter}$ is the magnitude of the maximum unfiltered (bare) conducted noise voltage at the EMI receiver, determined by simulation, calculation or practical measurement; A_{std} is the applicable standard limit (for example, CISPR 25 class 5); and m is the safety margin (3 to 6 dBμV is typical). As detailed in part 2, a measurement specifically of DM noise requires suitable DM and CM noise splitters at the LISN measurement ports.

By calculating the first harmonic amplitude from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance defined by the converter input capacitance C_1), equation 6 gives the required attenuation at the switching frequency as:

$$A_{dm} = 20\log\left(\frac{I_{out}}{2\pi f_s C_1}\cdot\frac{\sin(\pi d)}{\pi}\cdot\frac{1}{\mu\text{V}}\right) - A_{std} + m \qquad (6)$$

Component Value Calculations

I'll now provide some rudimentary expressions to derive component values for a π-filter.

Power Stage Input Capacitor

Neglecting equivalent series resistance (ESR)-related ripple (since the input capacitor is usually one or multiple low-ESR ceramic components), equation 7 gives the required ceramic input capacitance as:

$$C_1 > \frac{I_{out}d(1-d)}{\Delta V_{in,pp} f_s} \qquad (7)$$

where $\Delta V_{in,pp}$ is the peak-to-peak input ripple voltage specification measured at the power stage (5% to 10% ripple is a common specification) and effectively the DM excitation voltage source. For a buck converter, the ripple amplitude varies with duty cycle and reaches a maximum at 50%.

In general, correct operation of a voltage-fed dc-dc converter dictates a minimum amount of input capacitance. Such capacitance limits the steady-state voltage ripple at the converter input and constrains the input voltage swings during step-load transients.[20] Other factors related to converter operation may also limit the voltage ripple amplitude, including scenarios where:

- The linear regulator for a VCC bias supply that operates from the input voltage has a finite power-supply rejection.
- Undervoltage lockout requires accurate input-voltage sensing without excessive ripple.
- A voltage-mode control architecture requires input-voltage sensing for line feedforward, particularly for applications with a wide input-voltage range.

π-Stage Filter Components

Equation 8 specifies the required DM filter corner frequency, $f_{c\text{-}dm}$, assuming that the LC filter attenuation starts at the corner frequency and increases at 40 dB per decade:

$$A_{dm}(f) = \left(\frac{f}{f_{c\text{-}dm}}\right)^2 \Rightarrow A_{dm}(f)[\text{dB}] = 40\log\left(\frac{f}{f_{c\text{-}dm}}\right)$$
$$\Rightarrow \quad f_{c\text{-}dm} = \frac{f_s}{10^{A_{dm}[\text{dB}]/40}} = \frac{1}{2\pi\sqrt{L_1 C_2}} \qquad (8)$$

where A_{dm} is measured in dB and designates the required attenuation in decibels at the switching frequency.

Select the filter inductance (typically in the range of 0.47 μH to 4.7 μH) such that the characteristic (peak output) impedance of the filter is below the converter input impedance,[10] as expressed by equation 9:

$$Z_o = \sqrt{\frac{L_1}{C_1}} < \left|Z_{in(converter)}\right| = \frac{V_{in-\min}}{I_{in}} \quad \Rightarrow \quad L_1 < C_1\left(V_{in-\min}/I_{in}\right)^2 \qquad (9)$$

where I_{in} is the input current at the minimum input voltage, $V_{in\text{-}min}$.

Choose an inductor with low equivalent parallel capacitance (EPC), resulting in a high self-resonant frequency (SRF). Rearranging equation 8, equation 10 gives the filter capacitance as:

$$C_2 = \frac{10^{A_{dm}[\text{dB}]/20}}{4\pi^2 f_s^{\,2} L_1} \qquad (10)$$

Choose a ceramic capacitance for C_2 to provide low ESR and equivalent series inductance (ESL).

High-Frequency Attenuation And Component Parasitics

While DM currents at frequencies as high as 30 MHz are typically well attenuated by conventional π-stage filter designs, noise reduction at higher frequencies depends on component parasitic parameters and nonideal characteristics. More specifically, the self and mutual parasitics[22] of the filter elements degrade performance at high frequencies.

Ferrite beads[23] and small (0402 or 0603) package capacitors at the LISN side of the filter will increase attenuation, particularly in the three high-frequency bands limited by CISPR 25: the VHF band (30 to 54 MHz and 68 to 87 MHz), the TV band I (41 to 88 MHz), and the FM band (76 to 108 MHz). Three-terminal feedthrough capacitors[24] with low ESL (and thus high SRF) also enable improved high-frequency filter performance.

Case Study

Fig. 7 shows an example of a synchronous buck converter with an output voltage of 5 V, load current of 10 A and a switching frequency of 400 kHz. Setting the loop crossover frequency at 60 kHz aligns with a corner frequency of approximately 30 kHz for the input filter. Recall from part 12 that placing the filter corner frequency from a DM standpoint one decade to one octave below the loop crossover frequency (depending on the rate of rolloff of the filter gain) can avoid any break in the power-supply rejection performance (from the control loop to the input filter). Fig. 7 includes the parasitics of the filter components, but neglects those of the LISN for simplicity.

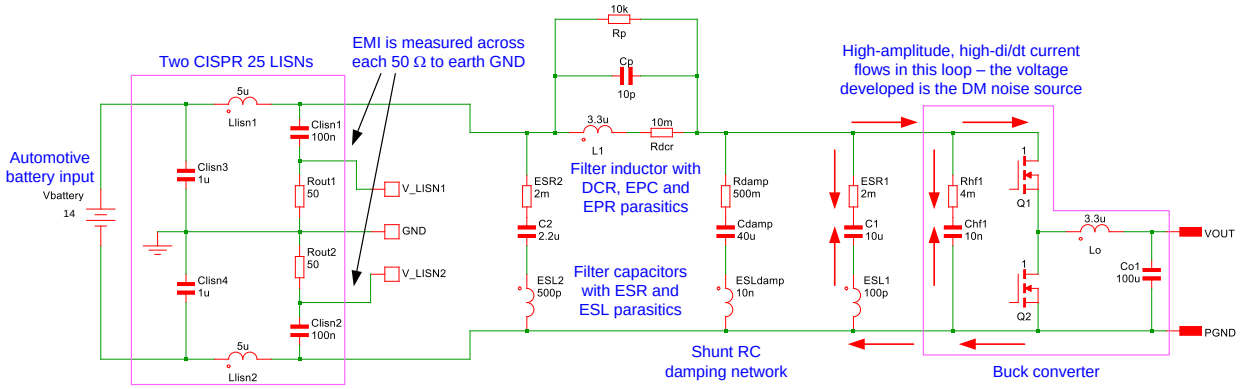


Fig. 7. SIMPLIS simulation schematic for a CISPR 25 CE setup with a synchronous buck converter and input π-filter.

Fig. 8 shows the simulated waveforms at the converter input and LISN output. Fig. 9 gives the frequency responses of the EMI filter and LISN circuit. The plot indicates a current attenuation of 89 dB at 400 kHz. Fig. 10 shows the filter output and converter input impedance plots confirming stability.[10]

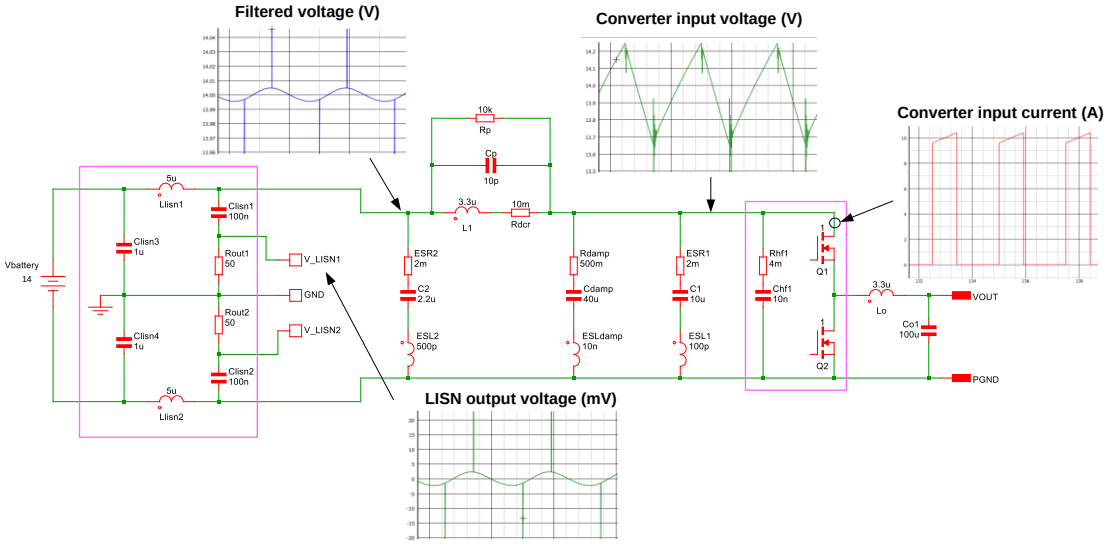


Fig. 8. Simulated time-domain waveforms at the converter input and LISN.

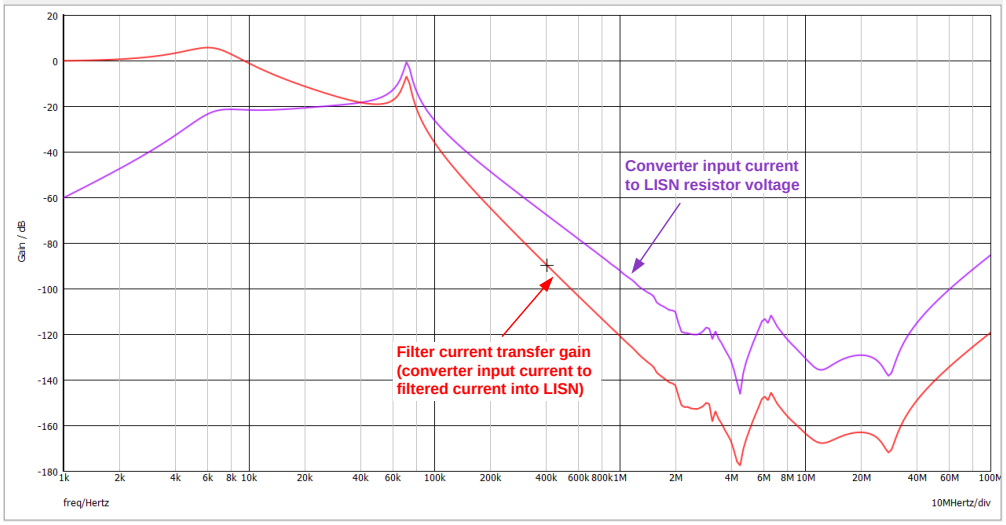


Fig. 9. Simulated DM filter frequency response over an extended frequency range.

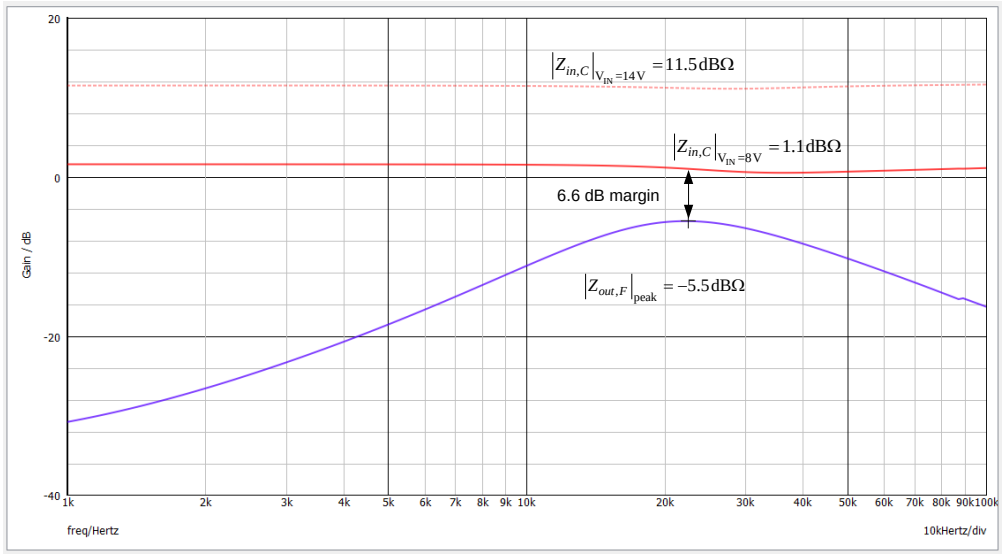


Fig. 10. Stability check of filter output impedance and converter input impedance.

In practice, you must consider the parasitic paths around the filter loops in the final simulation. Use an ideal filter schematic to generate a first-pass result, and then modify it as the filter layout progresses to account for the actual board layout.

Summary

With ongoing miniaturization, modularization and integration in power electronic systems, the requirements for EMI filters are quite demanding. Implement input filters that give you the best chance of pursuing the optimal noise attenuation, while also providing mismatched impedance conditions.

A consolidated treatment of input filter design mitigates the DM conducted noise signature of printed circuit board-mounted dc-dc converters. Confirming filter attenuation performance through simulation data has the potential to avoid expensive and time-consuming redesigns of hardware prototypes.

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Tim's current focus is on enabling technologies for high-frequency, low-EMI, isolated and nonisolated regulators with wide input voltage range, targeting industrial, communications and automotive applications in particular. He is a senior member of the IEEE and a member of the IEEE Power Electronics, Industrial Applications and EMC Societies.

For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".