ISSUE: December 2020

The Engineer's Guide To EMI In DC-DC Converters (Part 16): Common-Mode Input Filter Design

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The development and commercialization of dc-dc converters for use in various fields of power electronics—such as transportation, communications infrastructure and data-center applications—impose demanding specifications for power density, conversion efficiency and high-temperature operation. To meet these specifications, sustained progress in the design of new power electronics components unfortunately creates a fresh set of electromagnetic compatibility (EMC) problems.

Indeed, the spectrally rich emissions produced by high-frequency and high-edge-rate switching represent an undeniable impediment to the ongoing proliferation of dc-dc converters. Reducing such emissions requires a detailed understanding of electromagnetic interference (EMI) noise sources and propagation paths. Conductive common-mode (CM) currents are a significant subset of these emissions, especially at frequencies above 30 MHz where the parasitic coupling paths are lower impedance, and filtering becomes more challenging due to parasitic effects.

As discussed in part 13 of this article series,[1-15] CM noise current flows through the earth or system chassis ground (GND) connection and current magnitudes are dictated by the voltage slew rates at the power semiconductor terminals. The CM noise propagation path of a nonisolated converter[2] comprises mainly stray capacitances to GND from the output bus connections and—more importantly—the parasitic capacitance brought by the switching device(s) and related heatsink structure to GND.

An additional path for CM currents in isolated converters[7] is across the parasitic interwinding capacitance of the transformer, from the primary to the secondary side (where the CM current subsequently flows to chassis GND) and then returns to the primary side (where it is measured as noise). Mainly transmitted through coupling of a capacitive nature, CM current generally becomes evident at higher frequencies than differential-mode (DM) current. CM current also contributes significantly to radiated emissions,[13] leading to more severe noise issues.

This article reviews theoretical concepts related to dc-dc converter input filter design to minimize CM noise specifically, including selecting the EMI filter topology, estimating the required filter attenuation, calculating the filter component values, and integrating the CM filter stage synergistically to reduce the volume and weight of the overall EMI filter design. A simulation using a SIMPLIS model estimates the expected CM noise based on an input filter for conducted emissions from an automotive synchronous buck converter design.

Passive EMI Filtering With Integrated DM And CM Stages

Fig. 1a presents a conventional π-stage EMI filter for a dc-dc converter with DM and CM sections and a line impedance stabilization network (LISN)-equivalent circuit for EMI measurement. Fig. 1b shows the corresponding CM-equivalent filter circuit projected separately in order to simplify the analysis, assuming that the DM and CM noise components are not coupled to each other (for example, due to an asymmetric filter impedance, leading to mixed-mode noise). Separating the noise propagation modes helps the designer to understand the required attenuation as a first step toward EMI filter design.

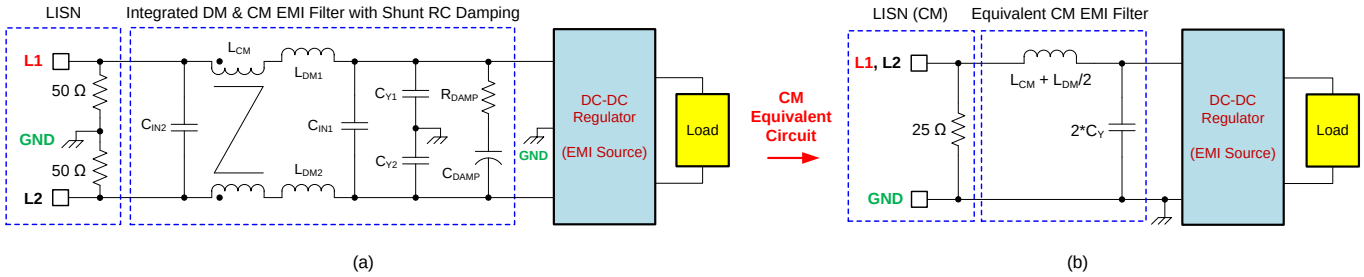

Fig. 1. An integrated DM and CM passive EMI filter (a) and its equivalent filter circuit for CM noise-current attenuation (b).

Because filters terminate with varying noise-source (switching converter) and load (measurement LISN and EMI receiver) impedances,[15] it is quite challenging to design such filters for use in power electronics applications. The effective load impedance of the filter shown in Fig. 1a for CM corresponds to that presented by the measuring LISN: two 50-Ω resistors in parallel.[2]

Inductors L_{DM1} and L_{DM2} in Fig. 1a represent discrete, uncoupled DM inductances and/or the leakage inductances of the common-mode choke (CMC), designated L_{CM1} in Fig. 1a. Note that such discrete inductances on each input supply line—implemented using conventional inductors or ferrite beads—appear in parallel from a CM standpoint, giving an effective CM inductance of $L_{DM}/2$, as indicated in Fig. 1b.

Meanwhile, C_{Y1} and C_{Y2} are the Y-capacitors connected from the supply lines to GND, assuming a three-wire dc-dc system—that is, where a system-level chassis ground, baseplate or protective earth terminal is available for connection. However, more common two-wire dc-dc systems preclude the installation of such capacitors. The CM inductance in such implementations acts by itself to increase the series impedance of the CM current loop,[13] resulting in an attenuation characteristic of -20 dB per decade.

CM Low-Pass Filtering: CMC Features And Characteristics

Connecting the CMC in series with the input lines increases the loop impedance of the CM noise propagation circuit. The winding polarity is such that the fluxes contributed by each coupled winding are cumulative for CM currents, yet cancel for DM. For a winding pair, the mutual inductances are equal and dependent on the self-inductances of the windings. Equation 1 gives the applicable expressions[16] as:

$$M = k\sqrt{L_1 L_2},\quad L_{CM} = \frac{L+M}{2},\quad L_{DM} = 2(L-M)$$
$$L_{M1} = k\,L_1,\quad L_{LK1} = (1-k)\,L_1 \qquad (1)$$

where k is the magnetic coupling coefficient, M is the mutual inductance, L_1 and L_2 are the individual winding inductances, L_{CM} and L_{DM} are the effective CM and DM inductances, and L_{M1} and L_{LK1} are the magnetizing and leakage inductances of winding 1, respectively.

Assuming perfect winding symmetry and ideal coupling, the winding inductances are equal and identical to the mutual inductance, as indicated by equation 2:

$$k = 1 \;\Rightarrow\; L = L_1 = L_2 = M,\quad L_{CM} = L,\quad L_{DM} = 0 \qquad (2)$$

CMCs for EMI filtering applications are typically wound with spatially separated windings. Such separation increases the leakage inductance and makes the CMC a more effective DM attenuation element. In many cases, interfacing that relatively small amount of inductance with a large DM capacitance often provides ample attenuation such that no actual DM inductor is required, thus enabling a unified DM-CM filter design. This is in contrast to CMCs targeted for data-transfer applications (such as USB or HDMI) where high leakage inductance results in signal distortion.

Understanding The Dominant CM Noise Source

Using an example of a buck converter, equation 3 gives the switch-node voltage in the time domain, assuming an ideal trapezoidal waveform without ringing at the switching transitions:

$$v_{sw,buck}(t)=\begin{cases}V_{in} & 0\le t<dT_s\\ 0 & dT_s\le t<T_s\end{cases} \qquad (3)$$

where V_{in} is the input voltage, d is the duty cycle and T_s is the switching period of the converter.

Equation 4 represents the corresponding Fourier series expression, which specifies that the rolloff of switch-voltage harmonic amplitude with frequency is $1/n$:

$$v_{sw}(t)=V_{in}d+\sum_{n=1}^{\infty}\frac{2V_{in}}{n\pi}\sin(n\pi d)\cos(n\omega_s t) \qquad (4)$$

where n is the harmonic order and $\omega_s=2\pi f_s$ is the switching frequency.

Equation 4 suggests that the CM spectrum envelope of the voltage waveform has a decay rate of 20 dB per decade of frequency. The CM coupling impedance to GND, being capacitive in nature, also decreases at 20 dB per decade, implying that the CM current spectrum is approximately flat over the frequency range of interest.

In practice, the parasitic coupling capacitance varies with frequency such that the CM current profile is less predictable. The output voltage ripple appearing on the load lines and at the load itself also causes CM noise, although this path is typically not as significant as that through the switch node.

Topology Selection

Because EMI filters are effectively impedance mismatching networks, the variation of noise source (dc-dc converter) and load (LISN) impedances versus frequency (for both DM and CM) has an effect on EMI filter performance. The output impedance of the filter and the noise source impedance of the converter, need proper mismatch, as do the input impedance of the filter and its load impedance. As a minimum, knowing at least the magnitude of the effective noise source and filter load impedances is important for a preliminary selection of the most appropriate filter topology (according to the criteria shown in Fig. 2) before proceeding with filter parameter calculations.

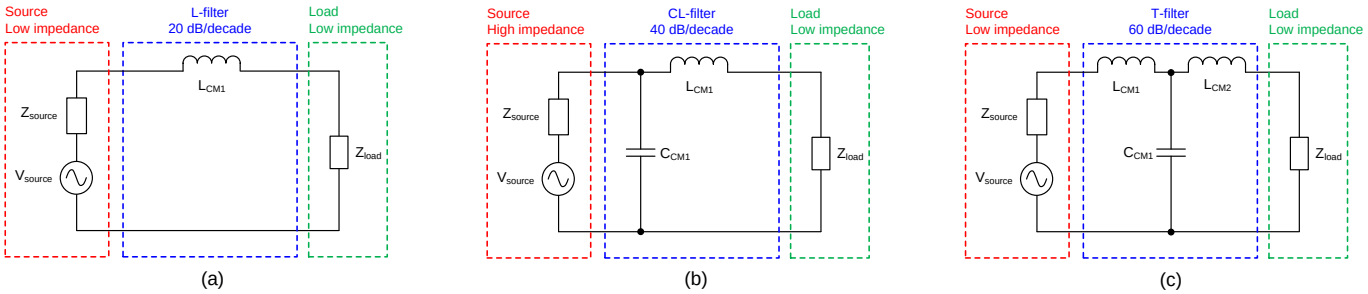

Fig. 2. Choice of CM filter topology based on impedance mismatch conditions: first-order inductive filter (a), second-order Γ-filter (b) and third-order T-filter (c). In the context of this discussion, the source represents the dc-dc converter noise source while the load represents the LISN.

For the purpose of CM filter design, the dc-dc converter can typically be characterized as a CM noise source with a capacitive impedance characteristic that decreases with frequency. Meanwhile, the LISN has an effective CM load impedance of 25 Ω, which classifies as a low impedance (above 100 Ω is generally recognized as high

impedance). According to the criterion of maximum impedance mismatching, a topology with high (inductive) output impedance is a common choice for the CM filter since this must effect a mismatch with the dc-dc converter. Similarly, the filter should present a high impedance to the LISN.

EMI Analysis And Filter Design

Fig. 3 is a flowchart of a systematic approach[17] to EMI analysis and filter design for switch-mode dc-dc converters, including steps for parasitic parameter extraction, component modeling, performance simulation, EMI input filter design and experimental verification by measurement. Using the iterative design loops in this approach helps determine an optimized EMC solution.

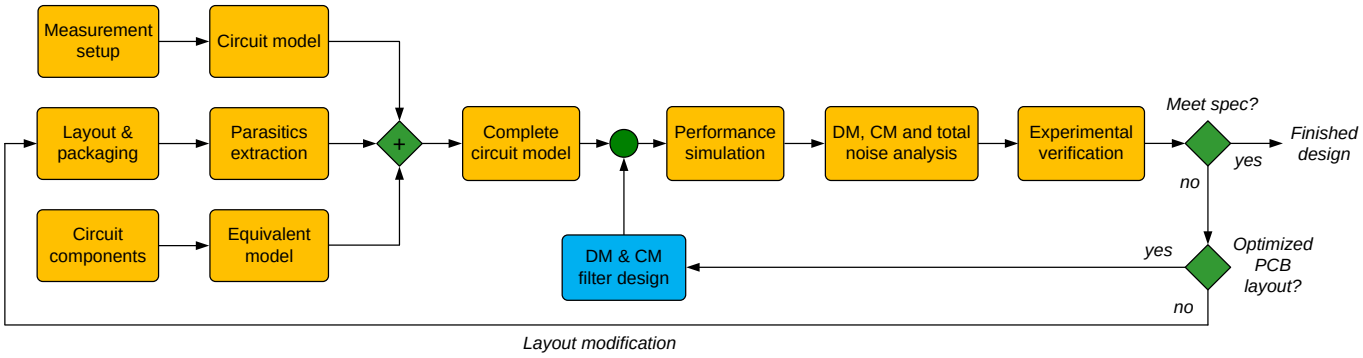

Fig. 3. Flowchart for EMI analysis and design in dc-dc converters.

As I'll discuss later, circuit simulation of the dc-dc converter and EMI filter is important in order to predict and confirm the attenuation performance before in-circuit validation. The goal of meeting EMI specifications is in terms of the total EMI noise measured (as prescribed by EMI standards). A segregation of individual DM and CM contributions[2] based on the total measurement provides a basis for understanding the relative impact from each mode.

Fig. 4 shows an EMI measurement setup for a synchronous buck converter based on the recommended setup for CISPR 25. C_{SW}, C_{VOUT+} and C_{VOUT-} explicitly denote the parasitic coupling capacitances from the switch node and output connections to GND.

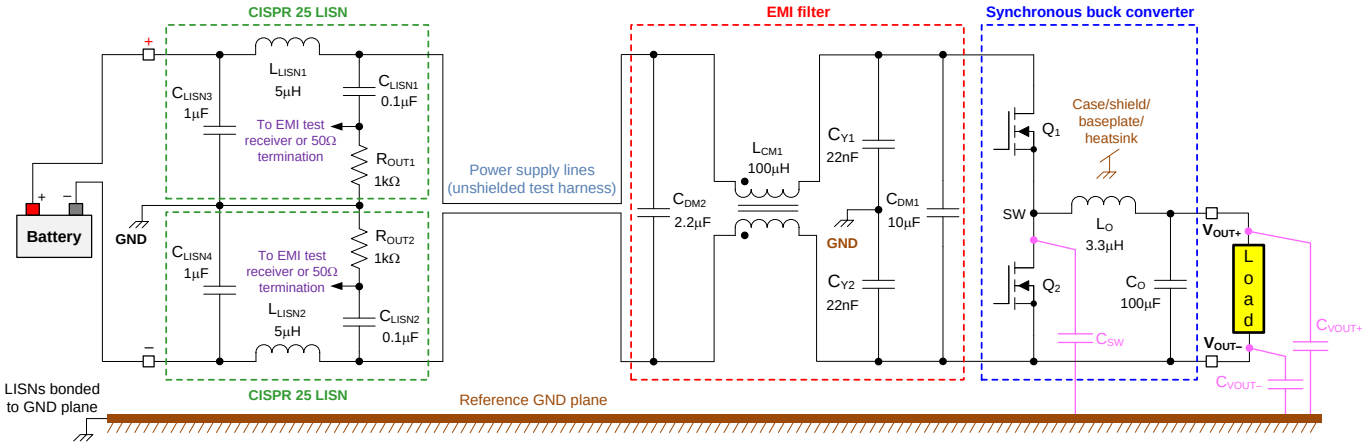

Fig. 4. A typical CISPR 25 conducted emissions measurement setup for a synchronous buck converter with an input filter.

According to the impedance mismatch criteria for EMI filter design, and given the relatively high source impedance of the CM noise circuit (the buck converter) at the frequency of interest and low load impedance of the CM noise circuit (the LISN), the implementation uses a second-order Γ-shaped filter (CL topology) for CM

noise suppression (similar to that shown in Fig. 2b) where the Y-capacitors face the dc-dc converter and the dotted terminals of the CMC attach to each LISN.

The following section details the CM filter design specifically, building on the DM filter design workflow outlined in part 15 to derive a unified filter structure for DM and CM attenuation.

CM Filter Design

As mentioned in part 15, a conventional way to design an EMI filter is to construct a hardware prototype of the system with an initial filter implementation derived from approximate calculations, practical experience, or both. Iterative EMI measurements and modification of the filter circuit yield a final design depending on the problematic frequencies until it is possible to meet the EMC standard with minimal cost and size of the filter components.

Determine The Required Filter Attenuation

The design of a CM input filter for dc-dc converters is typically performed at relatively high frequencies, 10 MHz and above. One option is to determine the *bare* noise measurement, which obtains the converter CM noise signature without a filter. Based on the measured result and applicable standard, calculate the required attenuation at the most demanding frequency.

Equation 5 gives the required filter attenuation as:

$$A_{cm}\left[\text{dB}\right] = A_{cm\text{-nofilter}}\left[\text{dB}\mu\text{V}\right] - A_{std}\left[\text{dB}\mu\text{V}\right] + m\left[\text{dB}\mu\text{V}\right] \qquad (5)$$

where $A_{cm\text{-}nofilter}$ is the magnitude of the maximum unfiltered (bare) CM noise voltage at the EMI receiver determined by simulation, calculation or practical measurement; A_{std} is the applicable standard limit (for example, CISPR 25 Class 5); and m is the safety margin (3 dBμV to 6 dBμV is typical).

As detailed in part 2, a measurement specifically of CM noise requires suitable DM and CM noise splitters at the LISN measurement ports.

Component Value Calculations

Here are some rudimentary expressions to derive component values for a CM input filter. Equation 6 specifies the required CM filter corner frequency, $f_{c\text{-}cm}$, assuming that LC filter attenuation starts at its corner frequency and increases at 40 dB per decade:

$$A_{cm}(f) = \left(\frac{f}{f_{c\text{-}cm}}\right)^2 \Rightarrow A_{cm}(f)\left[\text{dB}\right] = 40\log\left(\frac{f}{f_{c\text{-}cm}}\right)$$
$$\Rightarrow \quad f_{c\text{-}cm} = \frac{f_{design}}{10^{A_{cm}[\text{dB}]/40}} = \frac{1}{2\pi\sqrt{L_{\text{cm}}C_{\text{Y}}}} \qquad (6)$$

where A_{cm} designates the required attenuation in decibels (dB) at the design frequency, f_{design}, and $C_Y = C_{Y1} + C_{Y2}$ is the total Y-capacitance.

For a selected value of Y-capacitance, equation 7 gives the required CM inductance as:

$$L_{\text{cm}} = \frac{10^{A_{cm}[\text{dB}]/20}}{4\pi^2 f_{design}{}^2 C_{\text{Y}}} \qquad (7)$$

Noise reduction at high frequencies also depends on component parasitic parameters and nonideal characteristics. More specifically, the self and mutual parasitics of the filter elements degrade performance at high frequencies.

Select the CMC such that its core permeability bandwidth peaks close to the maximum frequency of the EMI specification (for example, 108 MHz for CISPR 25) where CM emissions dominate. The current rating of the CMC should also exceed the maximum converter input current. If the required CM series inductance is relatively low, one alternative is to use uncoupled ferrite beads on each input supply line instead of the CMC.

Case Study

Fig. 5 shows a simple example of a synchronous buck converter[18] with a rated load current of 6 A and a switching frequency of 400 kHz when set up for a CISPR 25 conducted emissions measurement using a first-order CM filter. The parasitics of the filter components are shown explicitly, while those of the LISNs are neglected for simplicity. The figure also includes the parasitic coupling capacitors from the switch node and load lines to GND. Red arrows denote the CM current conduction paths.

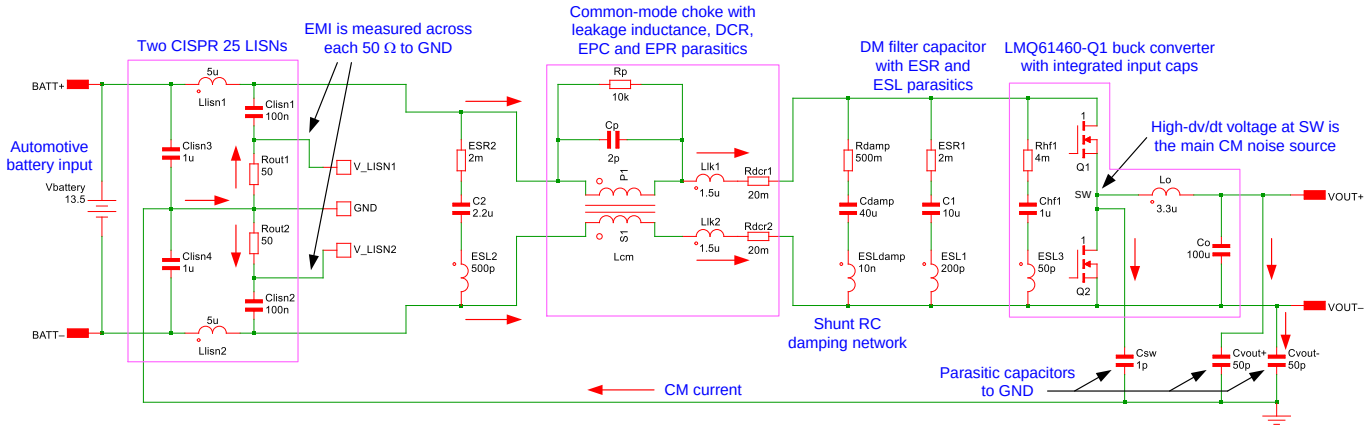

Fig. 5. A SIMPLIS simulation schematic of a synchronous buck converter in a CISPR 25 conducted-emissions test setup.

The leakage inductances of the CMC in Fig. 5 appear and behave as balanced self-inductances in series with each winding. Meanwhile, the effective parallel capacitance C_p and parallel resistance R_p model the CMC impedance peaking characteristic.

Fig. 6 shows the simulated waveforms of the total CM current and the two LISN output voltages. The currents through the parasitic capacitors to GND create in-phase voltages when measured across each 50-Ω measurement port. Thus, the LISN voltages that are in phase with respect to GND are CM emissions, while the out-of-phase components represent DM noise.[2]

In practice, you must consider the parasitic paths around the filter in the final simulation. Use an ideal filter schematic to generate a first-pass result; then modify it as the filter layout progresses to account for the actual board layout while adhering to the iterative steps outlined in Fig. 3.

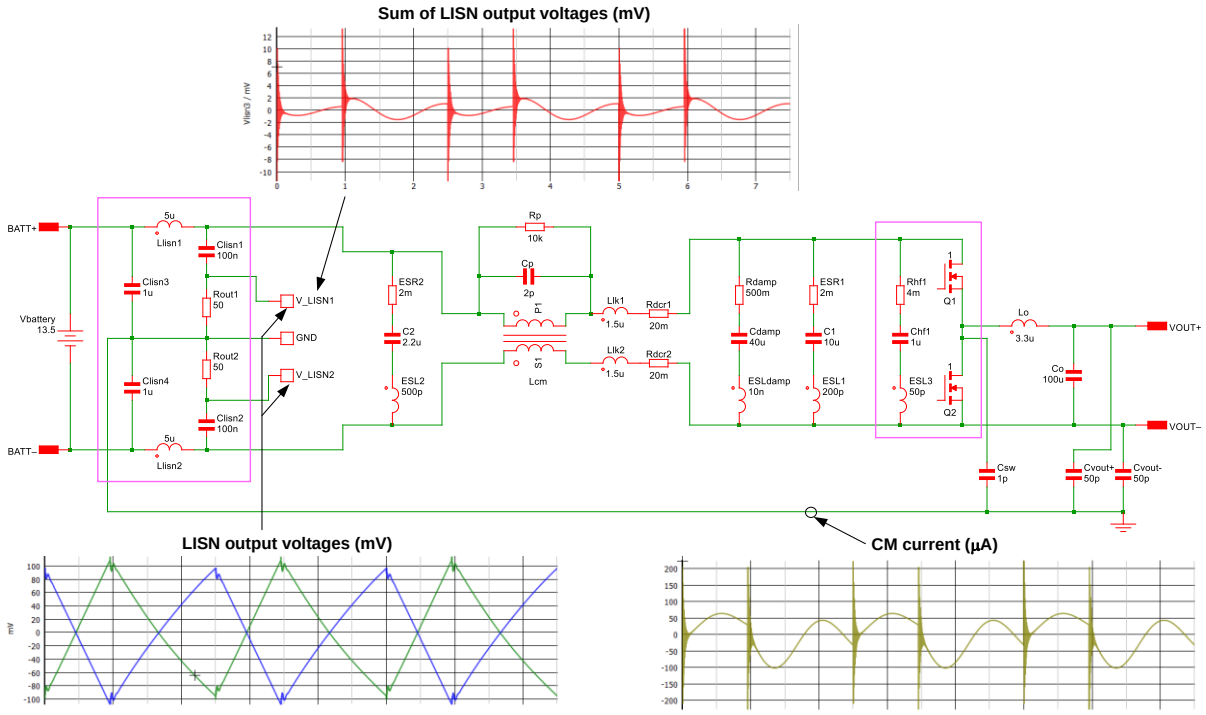

Fig. 6. Simulated time-domain waveforms with measurement points as indicated.

Summary

CM currents are strongly related to the voltage slew rates at the power semiconductor terminals and are mainly transmitted through coupling of a capacitive nature, which causes CM currents to have higher frequency ranges than DM currents. This article offered a consolidated overview of input filter design to mitigate the CM conducted noise signature of a dc-dc converter and included a design workflow applied to a synchronous buck converter in order to effectively suppress CM conducted noise. It is possible to extend simulation results designed to estimate CM filter attenuation performance to include the impact of layout-extracted parasitics if needed.

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For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".