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Simulation Demonstrates Impact Of Current-Loop Crossover Frequency On Stability

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Switching converters operating in current-mode control have been the subject of many debates regarding the modeling of the current loop and the modulator gain in particular. Without reopening the discussion here, this article modestly sheds some light on how too high a current-loop crossover frequency can impact the converter stability. Many engineers mistakenly believe that the subharmonic oscillations that occur at half the switching frequency in the voltage loop are caused by a peak in the current loop response at this frequency. In reality, the instability observed as a peak in the voltage loop at $F_{sw}/2$ is simply due to a poor phase margin in the current loop (caused by a pair of right-half plane zeros) not because of a peak there.

While this phenomenon was analyzed and explained many years ago through modeling of current-mode control, it can be difficult to find experimental results that demonstrate the underlying relationships between power supply crossover frequency, phase margin and the resulting instability. Although you do not need to measure the inner current loop when designing a current-mode-controlled converter, it is important to understand the phenomenon at play here. This article presents circuit models in SPICE and SIMPLIS that engineers can use specifically to simulate these effects.

This article begins by reviewing how current-mode controlled converters are susceptible to instability for duty ratios above 50% and how subtracting an artificial ramp from the current set point dampens the oscillations that occur with these higher duty cycles. These concepts are explained conceptually by applying perturbations to the inductor current waveforms and with some simple equations that explain how these perturbations die out or grow, depending on the duty ratio and the presence of the compensating current ramp. In the case, where the perturbations grow and are not damped, the previously mentioned subharmonic oscillations occur.

After explaining the instability and use of ramp compensation conceptually, a SIMPLIS model of a special test circuit is presented that enables simulation of the inductor current perturbations. This model can be used to visualize the effect of the duty ratio and the ramp compensation on the inductor current perturbations.

This SIMPLIS model not only demonstrates how the inductor current perturbations either grow or diminish over several switching cycles, it also demonstrates the sampling effect that Ridley first explained years ago in his seminal paper on the continuous-time model for current-model controlled converters. From this model, a sampled-data (*z*-domain) expression for the control voltage-to-inductor peak current response can be derived, which is then shown to confirm the duty ratio condition that governs converter stability.

The next section goes into detail on how this expression can be translated to the s-domain for plotting the control voltage-to-inductor peak current response, and observing the right-half-plane zeroes that are responsible for the aforementioned subharmonic oscillations. This section delves further into Ridley's model and related work.

All of this leads up to the presentation of a SPICE model version of Ridley's ac model for predicting the subharmonic oscillations in current-mode-controlled converters. This model is used to demonstrate the impact of varying amounts of compensating current ramp on converter stability. Specifically, it's used to simulate the impact of the compensating ramp on the crossover frequency on the control voltage-to-inductor peak current response and phase margin. This step is needed to analyze the current loop and then write its transfer function using Laplace equations.

In the last section, simulation is taken a step further as a SIMPLIS model is presented that models the response of the current loop as a function of duty ratio and peak inductor current. This is essentially a simulation of Ridley's model, which has been verified previously through analysis and experimental results, but not through a simulation. This step also is used to confirm the correctness of the equations found using SPICE.

Perturbing A Current-Mode Converter

If you perturb the inductor current of an uncompensated current-mode-controlled converter operated in continuous conduction mode (CCM), the disturbance dies out after a few switching cycles for duty ratios less than 50%. But bring the duty ratio beyond 50% and the same perturbation will grow exponentially, engendering an instability of frequency equal to half of the switching frequency: this is a subharmonic oscillation. A simple drawing shown in Fig. 1 graphically illustrates this fact for the two duty ratios.

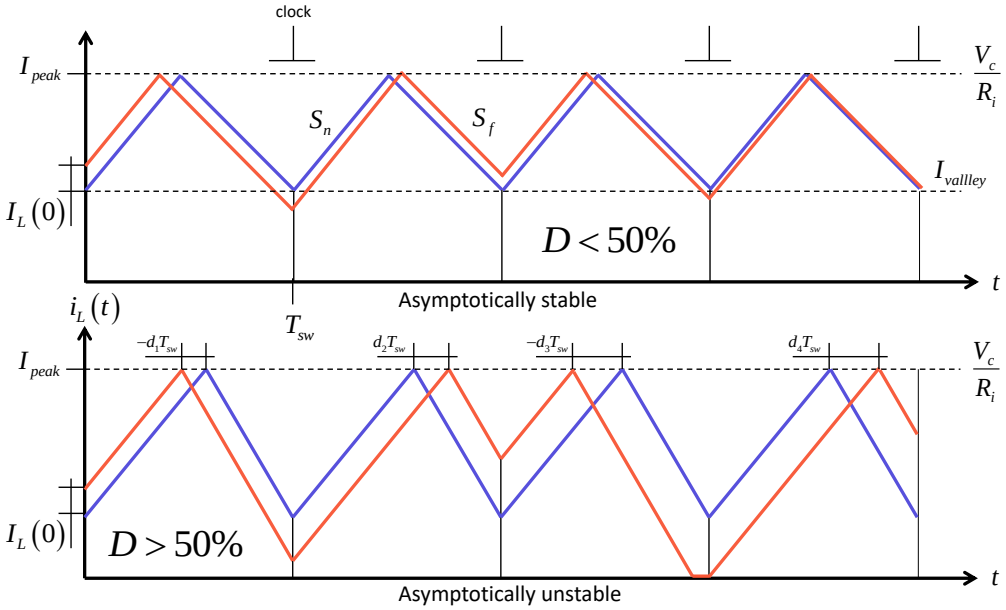

Fig. 1. The inductor current perturbation either dies out after a few switching cycles or grows exponentially depending on the duty ratio value.

In these graphs, the converter imposes a peak current setpoint via the control voltage V_c and the sense resistance R_i. The clock starts the switching cycle and turns the power switch on. The inductor current ramps up and reaches the setpoint at which the switch turns off.

Should you make a change in the control voltage V_c, the event at which the change is acknowledged is not the clock but the point at which the switch turns off. It is important to realize this fact before proceeding further. In the upper section of Fig. 1, the initial inductor current step (the orange waveform) propagates and disappears after a few cycles. Then as you increase the duty ratio, the damping reduces until the current waveform becomes unstable when the 50% threshold is crossed as depicted in the lower graph in Fig. 1.

Please note that this behavior occurs whether the voltage regulation loop is open or closed. A typical example, besides a true current-mode switching cell, is a voltage-mode converter featuring a maximum current limit: when it trips in some fault conditions, you can also observe these subharmonic oscillations before the converter resumes operation once the fault is gone.

Based on simple geometry,[1] it is possible to show that the perturbation in Fig. 1 propagates according to the following expression:

$$\Delta I_L(nT_{sw}) = \Delta I_L(0)\left[-\frac{D}{1-D}\right]^n \qquad (1)$$

where n is the number of cycles.

These oscillations naturally disappear if the ratio inside the brackets keeps below 1 which is ensured for a duty ratio *D* less than 50%. However, we want to operate across a wide range of duty ratios and, as we approach the 50% threshold, oscillations will grow in amplitude, potentially inducing undesirable instabilities.

A known cure to damp these oscillations for a duty ratio up to 100% consists of linearly reducing the setpoint value along the switching cycle. This is obtained by subtracting an artificial voltage ramp S_e from the control voltage V_c. When divided by R_i it gives a current slope $S_e^{'}$ expressed in A/s. Fig. 2 illustrates the principle in which S_n and S_f respectively designate the up and downslopes of the inductor current also expressed in A/s.

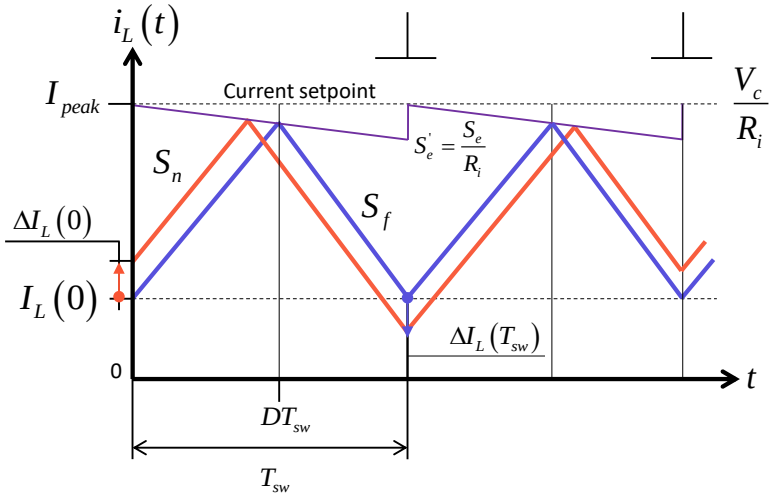

Fig. 2. Subtracting a ramp from the current setpoint helps suppress subharmonic oscillations.

As one can observe in Fig. 2, the effective peak current is now reduced as if we had artificially increased the sense resistance R_i. Now accounting for the compensating ramp's presence, we can graphically determine how the perturbation propagates cycle by cycle using the following formula:

$$\Delta I_L(nT_{sw}) = \Delta I_L(0)\left[-\frac{1-\frac{S_e^{'}}{S_f}}{\frac{D^{'}}{D}+\frac{S_e^{'}}{S_f}}\right]^n \qquad (2)$$

To ensure proper compensation up to a 100% duty ratio, you must inject a certain percentage of the inductor downslope S_f, again for keeping the ratio between brackets below unity. This is obtained for

$$S_e^{'} > 50\% \cdot S_f \qquad (3)$$

Please note that the recommendation is formulated considering a 100% duty ratio excursion. In a practical application, as the duty ratio rarely hits this extreme value, a smaller amount will ensure that you are not over-compensating the converter.

Visualizing The Perturbation

To illustrate the presence of a propagating perturbation, I have built a simulation template in SIMPLIS where two open-loop 100-kHz buck converters are perfectly synchronized by a common clock (Fig. 3). One delivers a certain amount of power with fixed operating conditions while the second will undergo a small input voltage change at a given point in time.

Note that these converters operate in open-loop conditions for the voltage regulation part but are working in *closed* loop for the inductor current. The setpoint voltage is fixed at 545 mV and imposes an inductor peak current of 5.45 A.

At the beginning of the simulation, inductor currents are similar and subtracting them leads to zero. Then, when the input voltage suddenly increases from 15 V to 25 V for the left-side converter, inductor current I_{L1} deviates from its original position and an error appears. By displaying the subtraction of both inductor currents along a few switching cycles via controlled sources G_5 and G_6, we can see in Fig. 4 how the error propagates and eventually disappears in this particular situation due to the compensation.

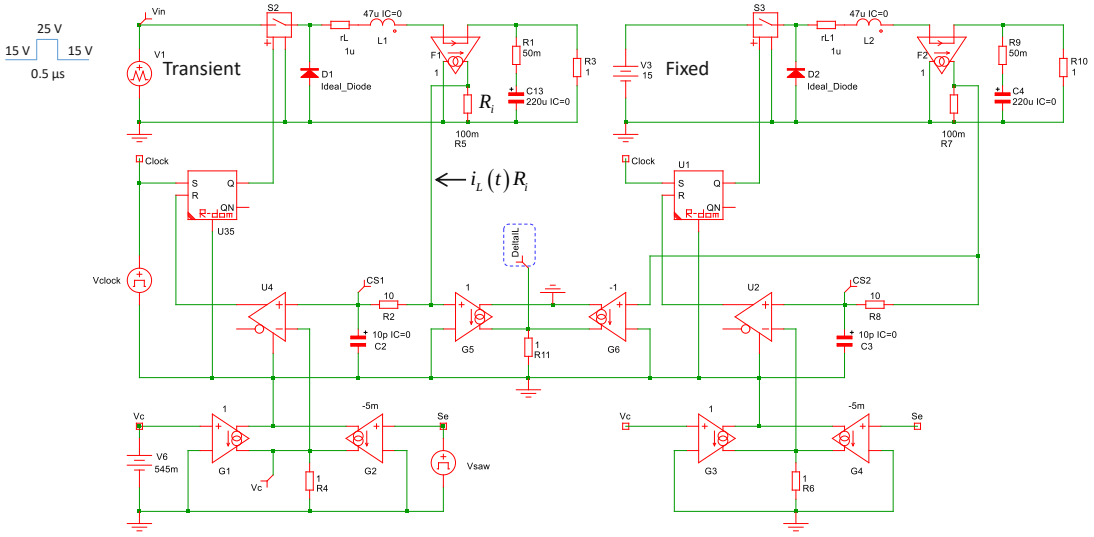

Fig. 3. Two converters are operated from the same clock but one of them sees its input voltage deviate at a given moment.

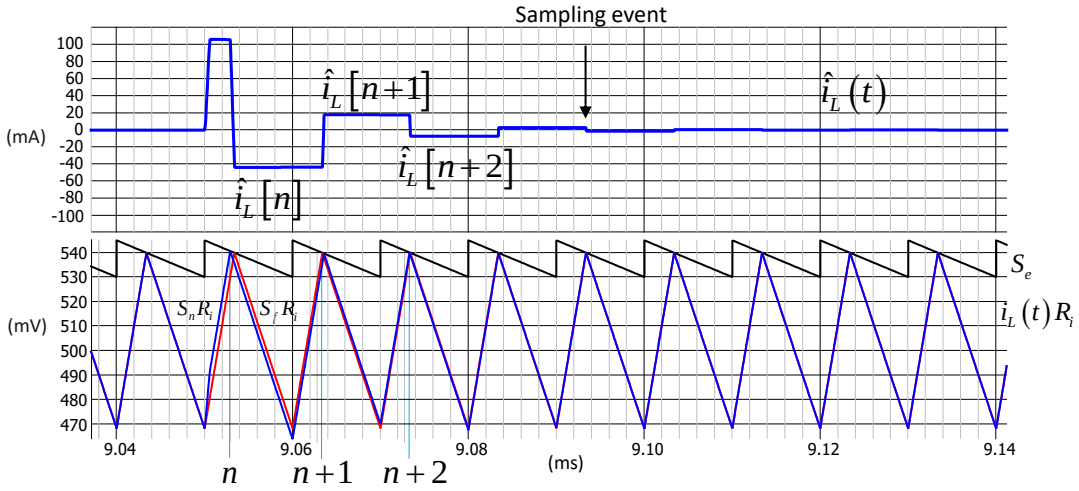

Fig. 4. The inductor current perturbation dies out after a few switching cycles or grows exponentially depending on the duty ratio value and whether or not there is compensation. In this case, the Fig. 3 circuit we're simulating is running with a duty cycle below 50%, but it also has the compensating ramp that allows for higher duty cycles.

Observing the blue waveform in Fig. 4 reveals a familiar shape which looks like the output of a sample-and-hold circuit where the system acquires the inductor current at the moment the switch turns off (target is reached) and holds it until the next sampling instant.

The step indicates a current difference at the perturbation point which eventually disappears after a few cycles. It is possible to isolate the inductor current error and plot it separately as Fig. 5 shows. As detailed by Ray Ridley in his thesis,[2] the transition from one sample to the other is not instantaneous. However, for the sake of simplicity, an immediate jump is assumed as represented in the lower portion of the figure. It is now possible to express the law linking each sample together by rewriting the expression given in equation (2).

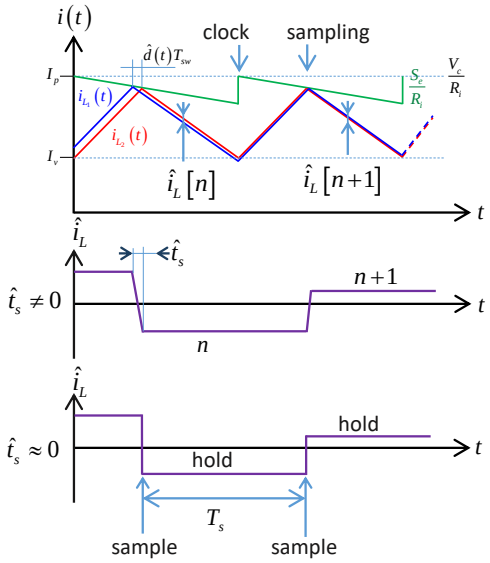

Fig. 5. The current perturbation representation is that of a sampling system.

First, by looking at the upper blue curve in Fig. 1 and realizing that $I_L(0) = I_L(T_{sw})$ at equilibrium, we can state:

$$S_f(1-D)T_{sw} = S_n D T_{sw} \tag{4}$$

Rearranging leads to:

$$\frac{1-D}{D} = \frac{D'}{D} = \frac{S_n}{S_f} \tag{5}$$

Then, substituting equation (5) into (2) and reformatting the expression leads to the difference equation we want:

$$\hat{i}_L[n+1] = -\alpha \cdot \hat{i}_L[n] \tag{6}$$

with

$$\alpha = \frac{S_f - S_e'}{S_n + S_e'} \tag{7}$$

Equation (6) describes how a perturbation occurring in the inductor current propagates cycle by cycle. To illustrate this phenomenon, we have kept the control voltage to a constant value (zero in ac) and we varied the input voltage for a small amount of time. What we observed is the *natural* response of the converter $r_n(t)$

obtained with a zeroed stimulus, V_c. Since we are interested in the control-to-inductor current transfer function, otherwise stated as the loop gain linking the control voltage v_c (the stimulus) to the inductor current i_L (the response), we need the *total* response $y(t)$ made of the natural and *forced* responses:

$$y(t) = r_n(t) + r_f(t) \qquad (8)$$

The forced response is obtained by keeping the input voltage constant but this time stepping the stimulus v_c. The results are shown in Fig. 6 for a 5-mV step in v_c. There is an immediate deviation when the event occurs followed by a propagation pattern described by equation (6). In the end, you can clearly see the 50-mA offset now created on the inductor current since we have increased the setpoint by 5 mV (R_i = 100 mΩ). As expected for a duty ratio less than 50%, the perturbation fades away after several switching cycles.

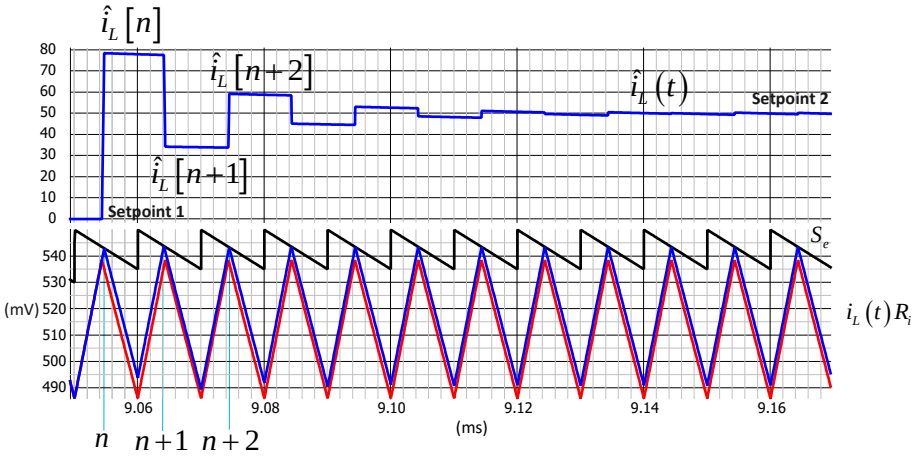

Fig. 6. In this mode, the control voltage is stepped while the input voltage remains constant.

Following reference [2], the diagram in Fig. 7 appears and can also be described with a difference equation as we previously did:

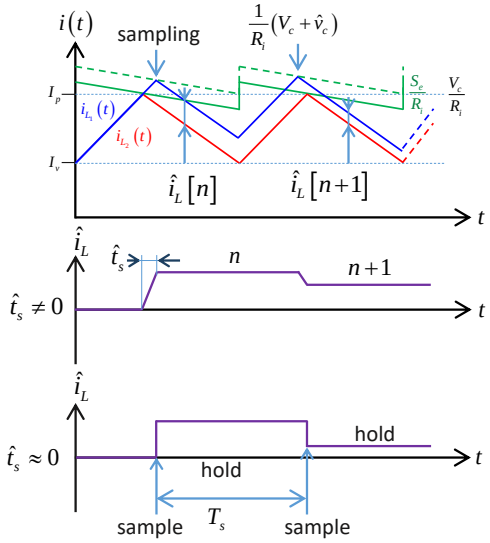

Fig. 7. This time the control voltage v_c is stepped and the perturbation propagation is analyzed.

$$\hat{i}_L[n+1] = \frac{1}{R_i}(1+\alpha)\cdot\hat{v}_c[n+1] \quad (9)$$

This equation predicts the peak inductor current deviation $\hat{i}_L$ at the sampling instant when the control voltage v_c is stepped while equation (6) describes how the perturbation propagates. According to equation (8), we can now combine the two responses proposed in equations (6) and (9), then write the complete or total *discretized* response:

$$\hat{i}_L[n+1] = -\alpha\cdot\hat{i}_L[n] + \frac{1}{R_i}(1+\alpha)\cdot\hat{v}_c[n+1] \quad (10)$$

We can rearrange and group terms as follows:

$$\alpha\cdot\hat{i}_L[n] + \hat{i}_L[n+1] = \frac{1}{R_i}(1+\alpha)\cdot\hat{v}_c[n+1] \quad (11)$$

Involving the *z*-transform, we have:

$$\hat{i}_L(z)\cdot(\alpha+z) = \hat{v}_c(z)\frac{1}{R_i}(1+\alpha)\cdot z \quad (12)$$

This is it! From this equation, we can define the sampled-data expression linking the control voltage to the inductor peak current:

$$\frac{\hat{i}_L(z)}{\hat{v}_c(z)} = \frac{1}{R_i}(1+\alpha)\cdot\frac{z}{\alpha+z} \quad (13)$$

This formula is also found in reference [3] but there it's derived without splitting the two responses. Because I believe it is important to understand the origins of this transfer function, the appendix at the end of the article shows how to determine it step by step with a colored graph for improved clarity.

The expression in (13) contains a pole located at $z_p = -\alpha$. To ensure stability, this pole must remain inside the unit circle as illustrated in Fig. 8.

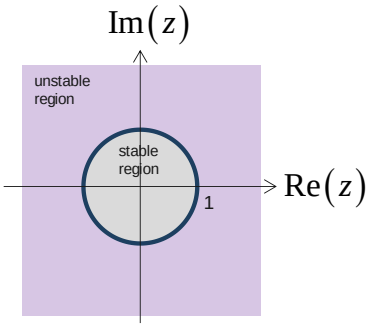

Fig. 8. The stable region lies inside the unit circle in the z-domain.

Therefore, to make sure the pole remains within the circle, we need to satisfy the following inequality:

$$|\alpha| < 1 \quad (14)$$

This condition is respected provided that $S_f < S_n$. Applying the definition for the inductor slopes during the on- and off-times of a buck converter, we can update this expression as:

$$\frac{V_{out}}{L} < \frac{V_{in} - V_{out}}{L} \qquad (15)$$

Knowing that for a CCM-operated ideal buck converter $V_{out} = DV_{in}$, we can update equation (15) to finally reach a similar conclusion as before to avoid instability:

$$D < \frac{1}{2} \qquad (16)$$

Loop Gain And Frequency Response

The expression from equation (13) represents a signal discretized in the *z*-domain and, as such, is not ideal to study the loop to further plot its frequency response. This formula describes the sampling of the inductor current when its value meets the setpoint and the hold of the acquired value until the next sampling instant. It is possible to represent this chain of operations with an equivalent simplified circuit as illustrated in Fig. 9.

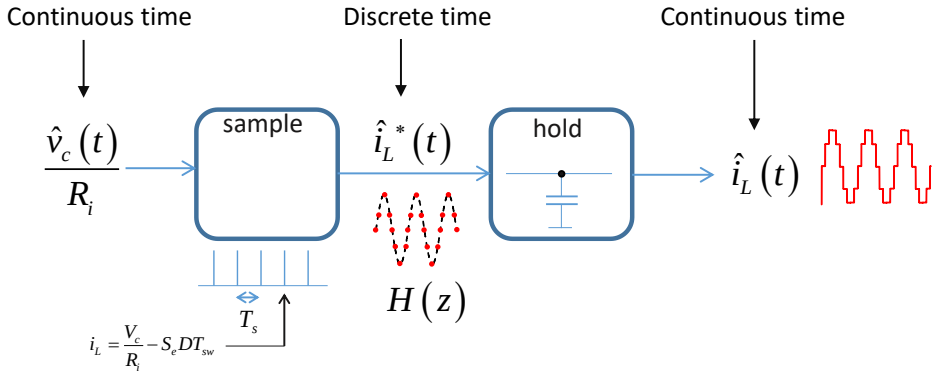

Fig. 9. The circuit illustrating the inductor peak current setpoint process involves a sample-and-hold equivalent model.

We can convert our discretized expression in equation (13) into the sampled-Laplace domain by replacing *z* by its definition e^{sT_s}. However, we need to account for the holding effect equivalent of going through a digital-to-analog converter (DAC) which, practically speaking, links the sampled- and continuous-Laplace domains. In that case, the newly converted expression needs to be supplemented by the transfer function of a zero-order hold (ZOH) which reconstructs a continuous-time function from a sampled sequence *x*[*n*]:[4]

$$H_{ZOH}(s) = \frac{1 - e^{-sT_s}}{sT_s} \qquad (17)$$

The frequency response of this ZOH can be studied with a mathematical solver such as Mathcad or via a SIMPLIS switching circuit. Both methods reveal a similar response to that shown in Fig. 10.

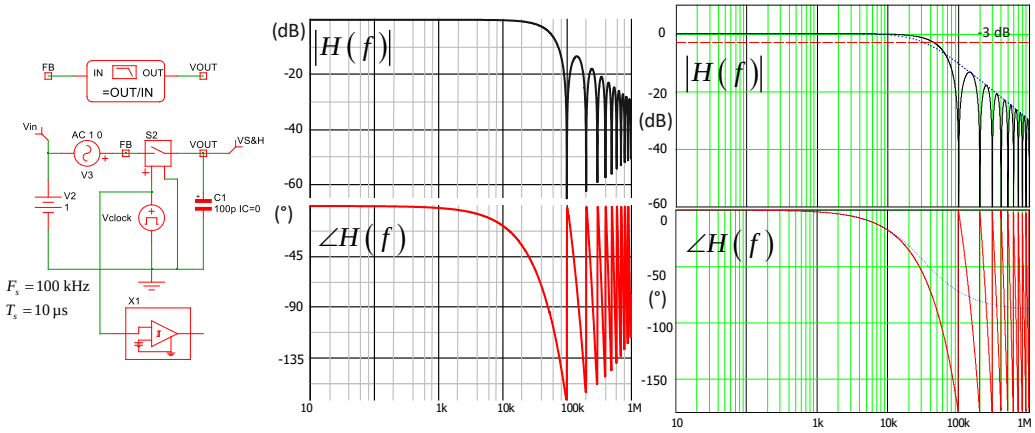

Fig. 10. SIMPLIS can quickly deliver the frequency response of a sample-and-hold circuit.

The dashed blue line represents a simplified first-order low-pass response as a reference with a pole located at F_s/π. If it predicts the magnitude well for the low-frequency portion, the phase quickly deviates from the complete response as frequency increases. The complete expression in the Laplace domain can now be defined as follows:

$$F(s) = \frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i}(1+\alpha)\frac{e^{sT_s}}{e^{sT_s}+\alpha}\frac{1-e^{-sT_s}}{sT_s} = \frac{1}{R_i}(1+\alpha)\frac{1}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \qquad (18)$$

At this point, we could replace e^{sT_s} by its second-order Padé approximant and this is what has been adopted in reference [5]. However, Ray Ridley in his thesis took a different path. His idea was to construct a model of the current-mode converter in which a block $H_e(s)$ models the sampling effects. As shown in Fig. 11, he placed this block after the sense resistor R_i rather than in the forward path as adopted by other authors. This choice has been commented on by Dennis Feucht in his series of articles on a unified current-model and the reader is invited to discover his work in reference [6].

Since we already know the closed-loop expression of the control-to-inductor peak current expression determined in equation (13), we can express the closed-loop relationship characterizing the model of Fig. 11 and work backwards to determine what transfer function H_e satisfies this closed-loop expression.

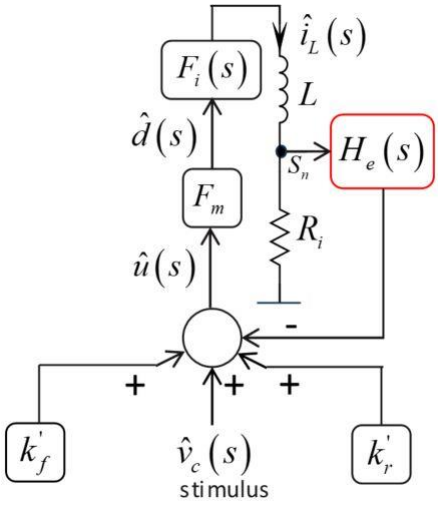

Fig. 11. The sampling effect is placed in the loop gain, after the sense resistor R_i.

To carry on with this analysis, we can transform the model of Fig. 11 into the block-diagram represented in Fig. 12 in which coefficients *k* (effects of input and output voltages, see reference [2] for more details) have been purposely reduced to zero as v_c is the sole stimulus here.

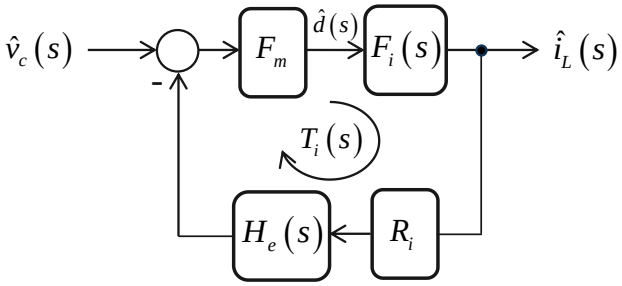

Fig. 12. The current loop appears clearly as an inner loop in this intermediate model.

The closed-loop transfer function of such an arrangement is immediate and equal to:

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{F_m F_i(s)}{1 + F_m F_i(s) H_e(s) R_i} \qquad (19)$$

In this expression, one can see a modulator block F_m, followed by another box, F_i, illustrating the duty-ratio-to-inductor current continuous-time transfer function. F_m designates the modulator gain which has been the object of many debates among the technical community. Ray Ridley recently wrote a series of articles explaining why the results found by other authors differed from his.[7]

Actually, we have shown in Fig. 7 that the external ramp S_e was subtracted from the control voltage but the ramp could also be added to the inductor current sense information scaled by the sense resistor R_i. This is, by the way, the method adopted by many commercial integrated circuits used to control switching power supplies. As illustrated in Fig. 13, both options lead to the exact same peak current setpoint.

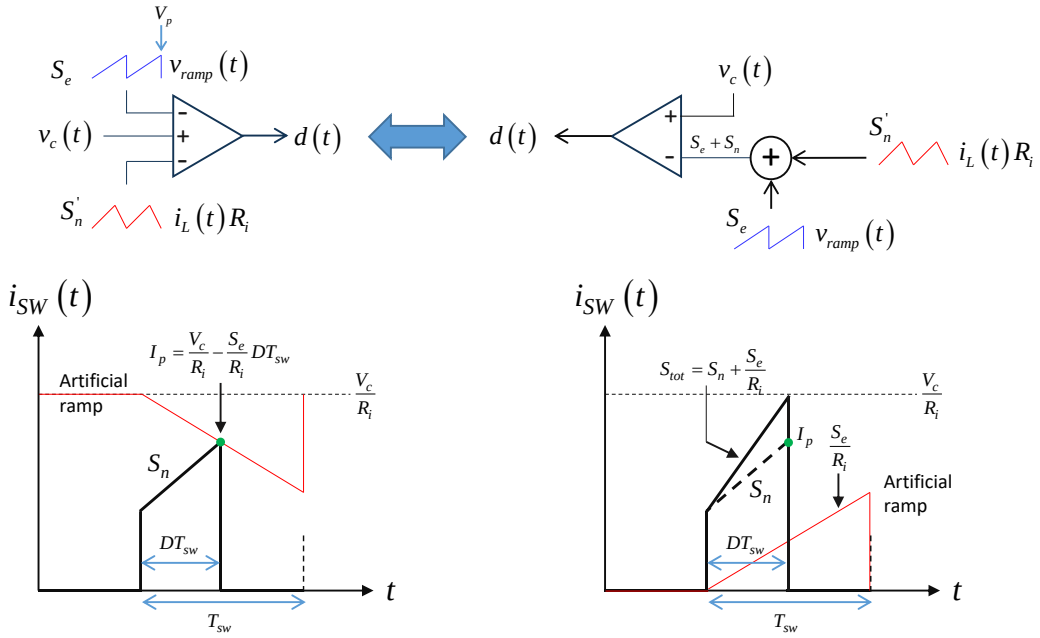

Fig. 13. The external ramp can either be subtracted from the control voltage (as shown on the left) or added to the current sense information (as shown on the right). Here the drawing represents the current flowing in the main power switch.

Based on the right-side modulator drawing in Fig. 13, it is *intuitively* possible to recognize a structure similar to that of the naturally sampled pulse-width modulator found in voltage-mode control whose small-signal gain depends on the peak amplitude V_p of the artificial voltage ramp S_e:

$$G_{PWM} = \frac{D(s)}{v_{err}(s)} = \frac{1}{V_p} = \frac{1}{S_e T_{sw}} \qquad (20)$$

In our case, the artificial voltage ramp S_e is summed with the inductor current signal scaled by R_i, leading to a small-signal gain equal to:

$$F_m = \frac{D(s)}{V_c(s)} = \frac{1}{(S_e + S_n R_i)T_{sw}} \qquad (21)$$

The second block which requires our attention is F_i which links the duty ratio to the inductor current. To find its definition, we need to resort to the PWM switch small-signal model in voltage-mode control described in detail in reference [8] and the object of an APEC seminar I taught in 2013.[9] Based on the equivalent circuit shown in Fig. 14 for a boost converter, the inductor current is obtained by dividing the voltage across the inductor by its impedance.

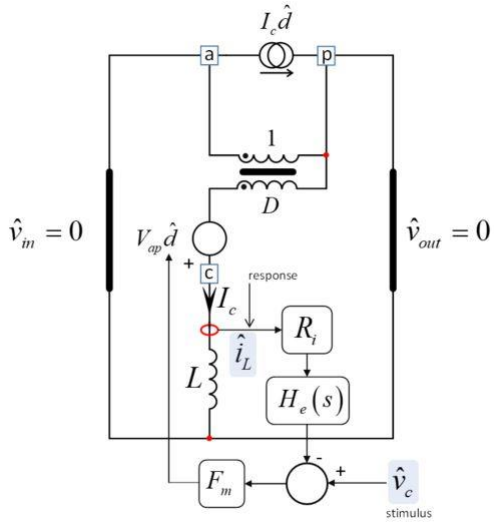

Fig. 14. The small-signal model of the PWM switch helps in determining the relationship linking the control voltage to the inductor current. It is represented here in a boost converter.

Considering ac-zeroed input and output voltages, the inductor current is immediate:

$$I_L(s)=\frac{V_{ap}D(s)}{sL} \tag{22}$$

From which we deduce the transfer function we want:

$$\frac{I_L(s)}{D(s)}=F_i(s)=\frac{V_{ap}}{sL} \tag{23}$$

The static voltage V_{ap} can be rewritten as an invariant combination of voltages at terminals *a*, *c* and *p*:

$$\frac{V_{ap}}{sL}=\frac{V_{ac}}{sL}+\frac{V_{cp}}{sL} \tag{24}$$

We can identify the inductor current *invariant* on- and off-slopes in a PWM switch-based model as:

$$S_n=\frac{V_{ac}}{L} \tag{25}$$

and

$$S_f=\frac{V_{cp}}{L} \tag{26}$$

If we combine these two definitions in (24), we have:

$$F_i(s)=\frac{S_n+S_f}{s} \tag{27}$$

We can now determine the value of $H_e(s)$ which satisfies the following equality:

$$\frac{F_m F_i(s)}{1+F_m F_i(s) H_e(s) R_i} = \frac{1}{R_i}(1+\alpha)\frac{1}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \tag{28}$$

Going through the math and simplifying leads to:

$$H_e(s) = \frac{sT_s}{e^{sT_s}-1} \tag{29}$$

This block placed after the sense resistor R_i models the sampled inductor current before entering the modulator box F_m. Such an expression, again, is impractical to use considering the presence of the exponential term. A possibility to simplify it consists of involving the second-order Padé approximant:

$$e^{sT_s} \approx \frac{1+\frac{1}{2/\pi}\left(\frac{s}{\omega_s/2}\right)+\left(\frac{s}{\omega_s/2}\right)^2}{1-\frac{1}{2/\pi}\left(\frac{s}{\omega_s/2}\right)+\left(\frac{s}{\omega_s/2}\right)^2} \tag{30}$$

If you substitute this expression into equation (29) and rearrange the whole thing, you have:

$$H_e(s) \approx 1-\frac{s}{\omega_s/\pi}+\left(\frac{s}{\omega_s/2}\right)^2 = 1+\frac{s}{\omega_n Q}+\left(\frac{s}{\omega_n}\right)^2 \tag{31}$$

with

$$Q = -\frac{2}{\pi} \tag{32}$$

and

$$\omega_n = \frac{\omega_s}{2} \tag{33}$$

where

$$\omega_s = 2\pi F_s$$

designates the converter switching frequency. This expression (31) describes a pair of right-half-plane zeroes (RHPZ) located at half of the switching frequency. The plot in Fig. 15 confirms this fact with a rising magnitude as any zero should bring, but the phase drops rather than also going up as would normally happen with zeros located in the left half-plane.

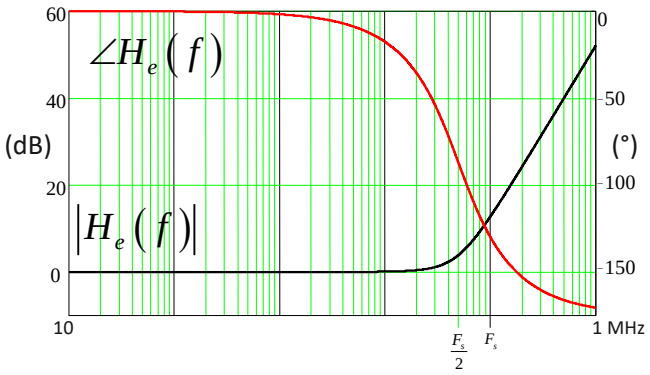

Fig. 15. The sampling block response is that of a right-half-plane zeros pair.

Considering The Current Loop

Looking at all the data we now have, it is possible to assemble a complete SPICE model predicting the sub-harmonic oscillations. This is what is proposed in reference [2] but offered in a netlist form only. I have rebuilt the entire model as proposed in Fig. 16 using the large-signal voltage-mode PWM switch model to which a duty ratio modulator featuring the sampling block H_e is added.

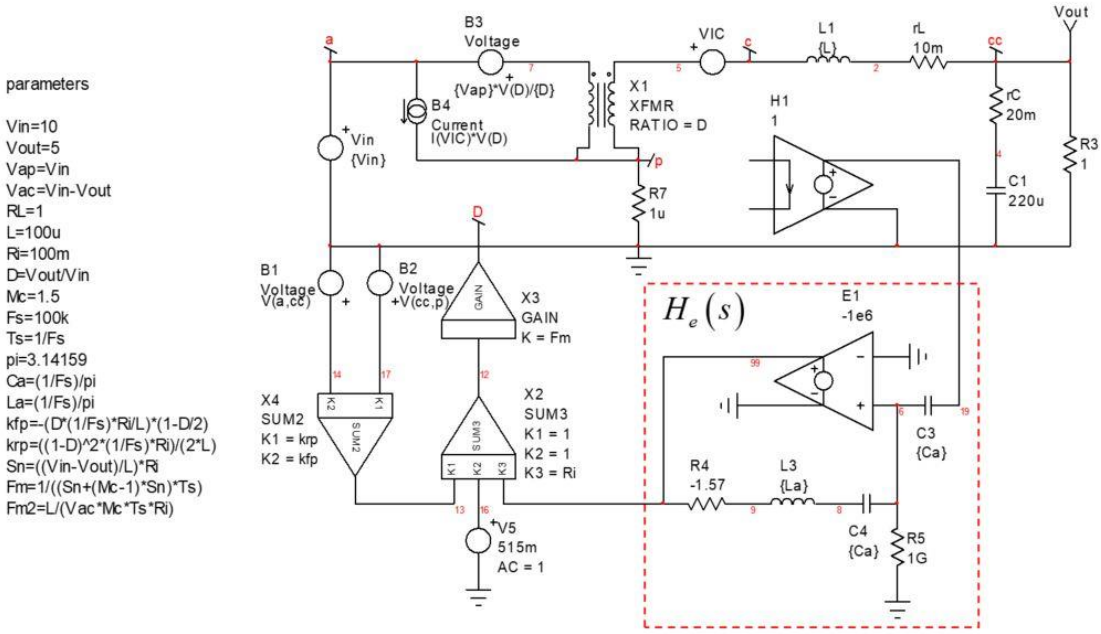

Fig. 16. The Ridley ac model predicts subharmonic oscillations through the added block $H_e(s)$.

Please note the presence of a negative resistance for realizing the sampling block transfer function. This subcircuit cannot transmit a dc component which unfortunately constrains the model to ac analyses only. If we run a simulation with and without compensation ramp, the classical control-to-output transfer function of the CCM buck operated in current-mode control appears in Fig. 17 with its subharmonic poles located at half the switching frequency.

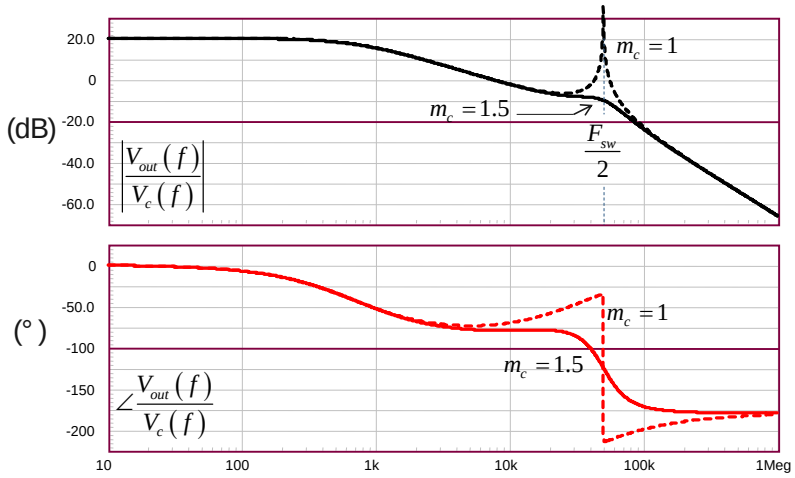

Fig. 17. The peaking located at $F_{sw}/2$ is quickly damped as external ramp is added.

Adding some compensation ramp $S_e^{'}$ via parameter m_c defined as

$$m_c = 1 + \frac{S_e^{'}}{S_n} \qquad (34)$$

damps the poles as expected (m_c = 1.5). We see in the model that parameter m_c does not affect the sampling block at all since all its elements L_a and C_a have fixed values depending on the switching frequency and the quality factor defined in equation (32). How does this added ramp tame the oscillations then?

We need to focus our attention on the inner loop characterized by the loop gain $T_i(s)$ highlighted in Fig. 12. To determine this transfer function, we can first simplify the SPICE model from Fig. 16 to determine this transfer function in an easy way: open the current loop after the modulating block X_3 and apply the stimulus to node *D*. Fig. 18 shows the modified circuit.

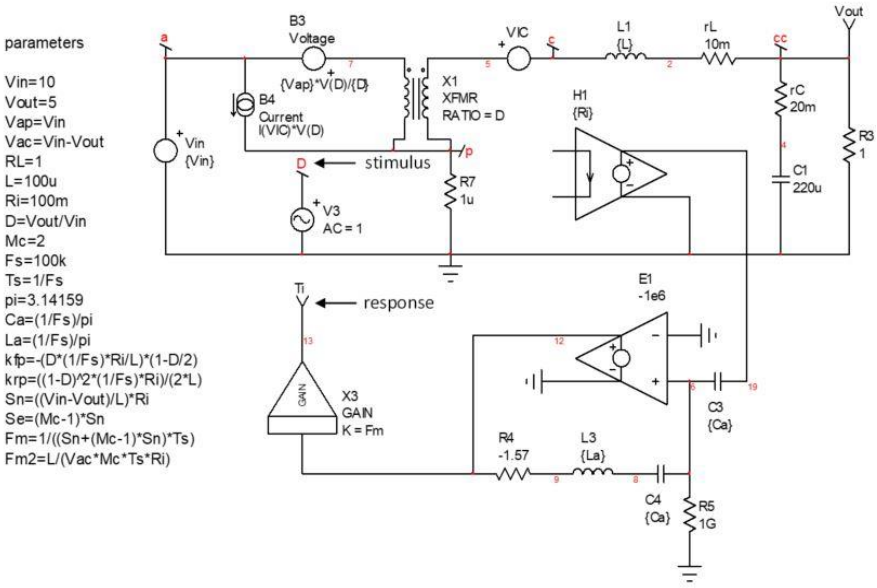

Fig. 18. By opening the loop after the modulator F_m, we can observe the current-loop response.

The simulation results for various compensation levels m_c are quickly obtained and they appear in Fig. 19. As you can see, injecting more ramp affects the magnitude but not the phase response of the current loop gain.

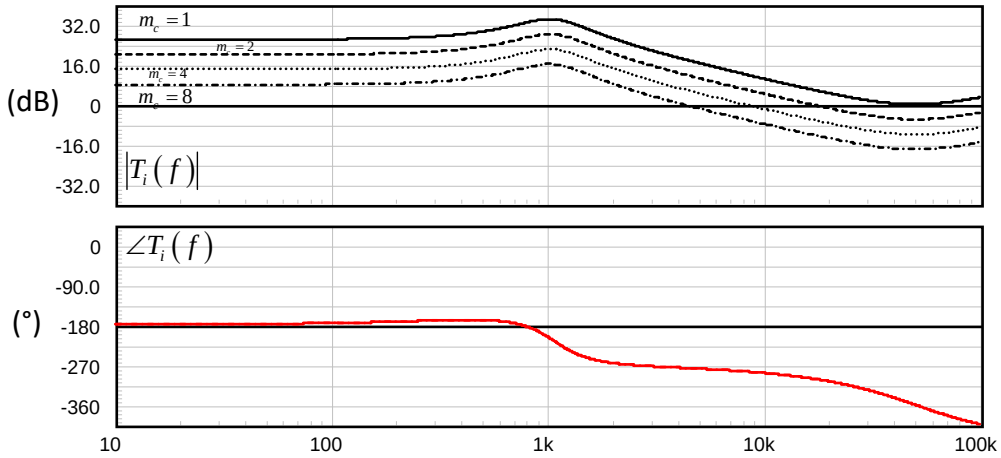

Fig. 19. SPICE gives us the response we expect from this simulation circuit.

To symbolically derive this transfer function, we can build an intermediate simplified schematic such as the one proposed in Fig. 20.

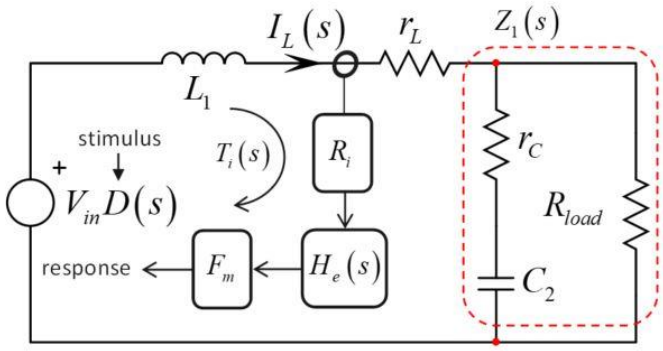

Fig. 20. The current loop transfer function is determined using this equivalent circuit.

The inductor current is immediately determined considering the modulated source $D(s)V_{in}$ driving the impedance made of the series connection of L_1, r_L and the impedance combining the output capacitor and the load:

$$I_L(s) = \frac{D(s)V_{in}}{sL_1 + r_L + \left(\frac{1}{sC_2} + r_C\right) \| R_{load}} \qquad (35)$$

The response we want is the inductor current scaled by R_i and affected by H_e and F_m. Rearranging to reveal T_i we have:

$$T_i(s) = \frac{V_{in} R_i}{sL_1 + r_L + \left(\frac{1}{sC_2} + r_C\right) \| R_{load}} \frac{1}{S_n R_i m_c T_s} H_e(s) \qquad (36)$$

Ridley in his thesis reworked the formula in a welcome low-entropy form in which a second-order polynomial expression appears:

$$T_i(s) \approx \frac{L_1}{R_{load} T_s m_c (1-D)} \frac{1 + sR_{load} C_2}{1 + \frac{s}{\omega_0 Q} + \left(\frac{s}{\omega_0}\right)^2} H_e(s) \qquad (37)$$

where

$$Q\big|_{r_L = r_C = 0} = \frac{1}{\omega_0 \left(\frac{L_1}{R_{load}} + r_C C_2\right)} \qquad (38)$$

and

$$\omega_0 = \frac{1}{\sqrt{L_1 C_2}} \qquad (39)$$

Now using this formula, I have plotted the response of the loop gain depending on the injected compensation ramp in Fig. 21. As already confirmed by the SPICE simulation, there are no subharmonic poles in this plot. You can see the peaking due to the buck *LC* resonating components but the instability comes from the crossover frequency f_c.

Without external ramp (m_c = 1), as we go up the frequency axis, the phase margin fades away because of the stress imposed by the RHP zeroes pair located at $F_{sw}/2$: no wonder the inner loop is unstable with this scenario. By injecting an extra amount of ramp, you lower the magnitude curve and force crossover at a more favorable location, where the phase stress is less severe.

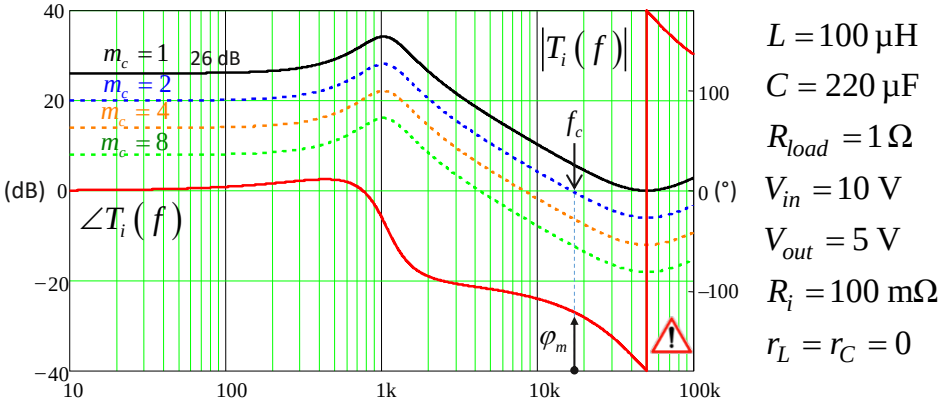

Fig. 21. The current loop gain does not show subharmonic oscillations but a lack of phase margin.

For instance, with a 100% compensation ramp (m_c = 2), the crossover is slightly below 20 kHz and the phase margin is now greater than 70°. As you keep increasing the compensation ramp amplitude, crossover reduces and phase margin improves. The compensation ramp, however, shall not be of too large an amplitude as it defeats the current-mode control scheme and makes the converter operate closer to a voltage-mode type of

control. This makes sense intuitively as the artificial ramp amplitude no longer becomes negligible with respect to the inductor information.

If we now consider the upper frequency portion of the spectrum while setting the sampling gain H_e to 1, it is possible to show that the high-frequency loop gain expression becomes

$$T_{i,\mathrm{HF}}(s) \approx \frac{L_1}{R_{load} T_s m_c (1-D)} \frac{sR_{load} C_2}{s^2 L_1 C_2} = \frac{1}{s \dfrac{m_c (1-D)}{F_s}} = \frac{1}{\dfrac{s}{\omega_{po}}} \qquad (40)$$

in which the 0-dB crossover pole is defined as

$$\omega_{po} = \frac{F_s}{m_c (1-D)} \qquad (41)$$

Without ramp (m_C = 1) and a duty ratio of 50%, the maximum crossover frequency the current loop can attain is

$$f_{c,\max} = \frac{\dfrac{F_s}{m_c (1-D)}}{2\pi} = \frac{\dfrac{F_s}{1\times(1-0.5)}}{2\pi} = \frac{F_s}{\pi} \approx 32\ \mathrm{kHz} \qquad (42)$$

which is what the blue dashed curve in Fig. 22 confirms.

Measuring The Current Loop

The model we have detailed here has been validated on many occasions by Ridley in his thesis and later on through other measurements. However, I wanted to show how this can be done with a simulator like SIMPLIS because it is not an obvious exercise. SIMPLIS is the choice here, rather than SPICE, because it allows easy generation of Bode plots without resorting to the use of an average model as would be required in SPICE.

Unlike in a classical Bode plot analysis in which the stimulus and the response are analog signals, the variables at play here are the duty ratio and the peak inductor current. Both are discrete values changing cycle by cycle. How can we then conduct a measurement on a working board?

The paper referenced in [10] describes how a digital modulator can do the job. The goal is to add a small modulation to the existing duty ratio while keeping the loop closed. The adopted principle is described in Fig. 23.

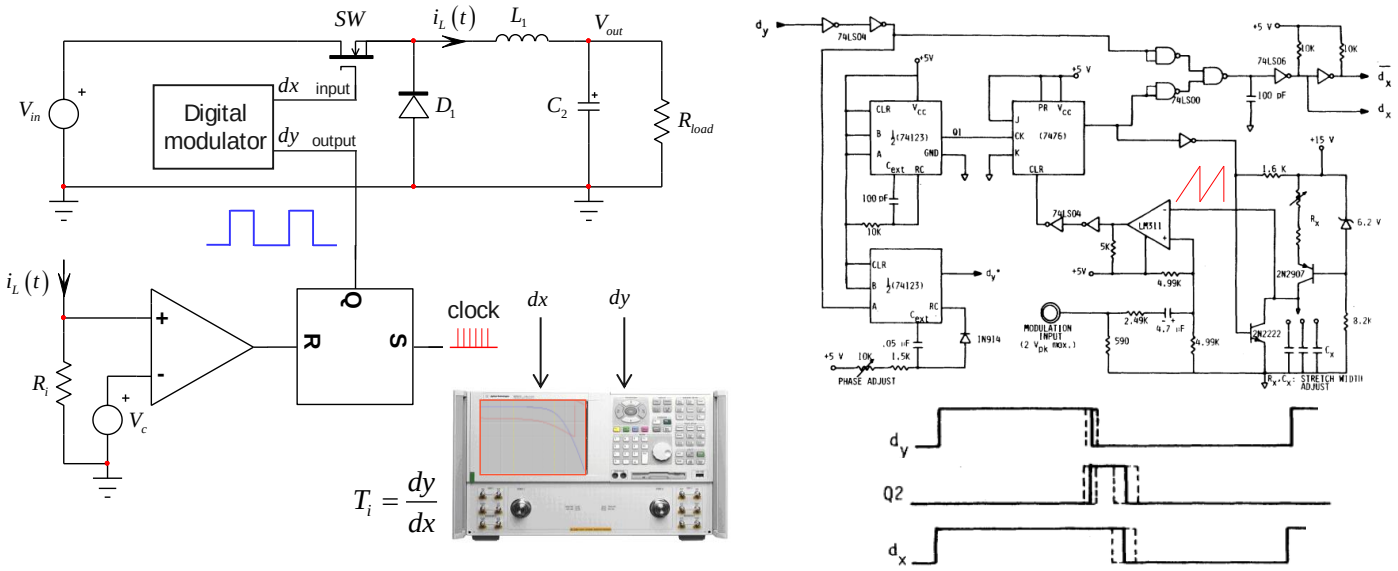

Fig. 23. A digital modulator takes the original duty ratio and adds a small ac modulation to it.

Basically, the output of the main PWM latch d_Y is immediately passing through the modulator and appears in d_X which drives the power MOSFET on. It stays in this mode for the on-time duration. When d_Y drops, output d_X does not immediately follow but a small amount of time is added before this happens. If this extra time is ac modulated by a pulse-width modulator, then you have a means to insert a digital perturbation in the loop gain. This is what the right-side schematic assembled with logic gates did back in 1986.

In order to test this circuitry under SIMPLIS, I have built a simpler architecture also featuring a pulse-width modulator. It is presented in Fig. 24.

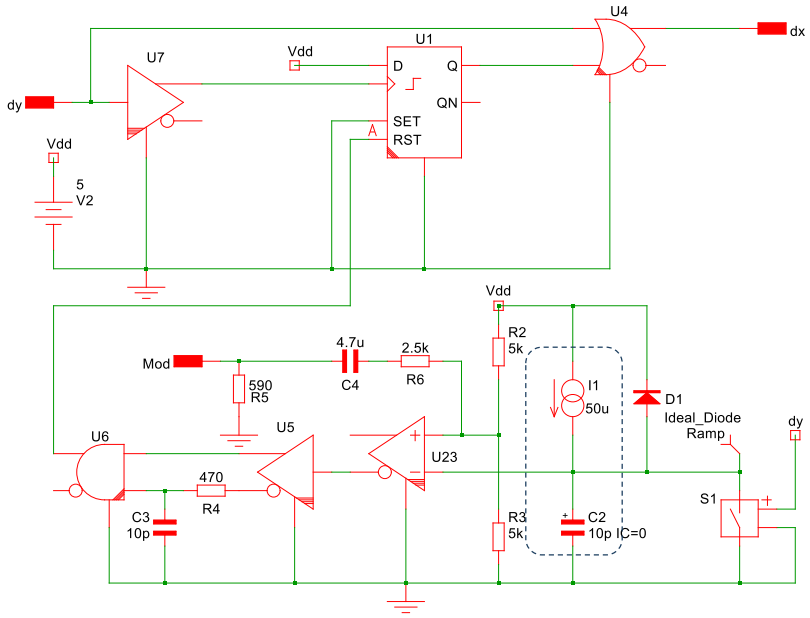

Fig. 24. A simpler digital modulator has been built in SIMPLIS to measure the current loop gain.

When d_Y goes high, d_X follows immediately via U_4 while the information is latched by U_1. Its output biases the second input of U_4 which maintains d_X high even if d_Y disappears.

While d_Y is high, the timing capacitor C_2 is discharged. When d_Y drops because the inductor current has reached its setpoint, d_X keeps high since U_1 is still armed. C_2 is released and starts to charge. When its voltage meets the setpoint imposed by R_2 and R_3, a reset pulse is sent to U_1 and d_X drops.

If an ac signal is now applied at the junction of R_2 and R_3, you modulate the duty ratio as expected by introducing a small delay. Once encapsulated into a subcircuit, the switching buck converter is ready to be analyzed as proposed in Fig. 25. The timing capacitor value is purposely kept small to prevent the insertion of too wide a delay which could perturb the analysis.

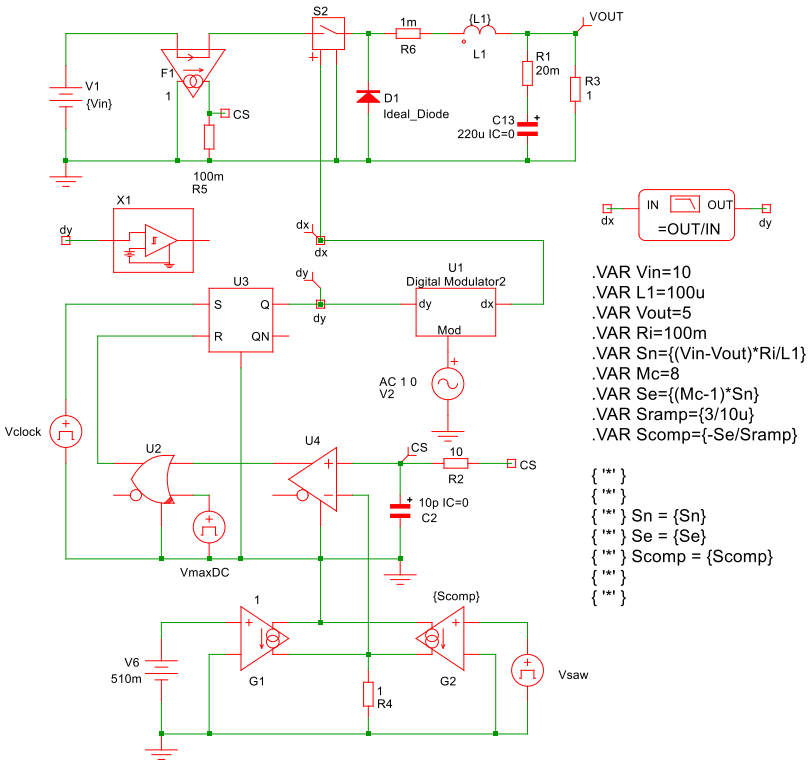

Fig. 25. The modulator is inserted between the driver output and the power MOSFET.

The results are given in Fig. 26 and confirm all the theoretical curves obtained in Fig. 21 for different values of the compensation ramp.

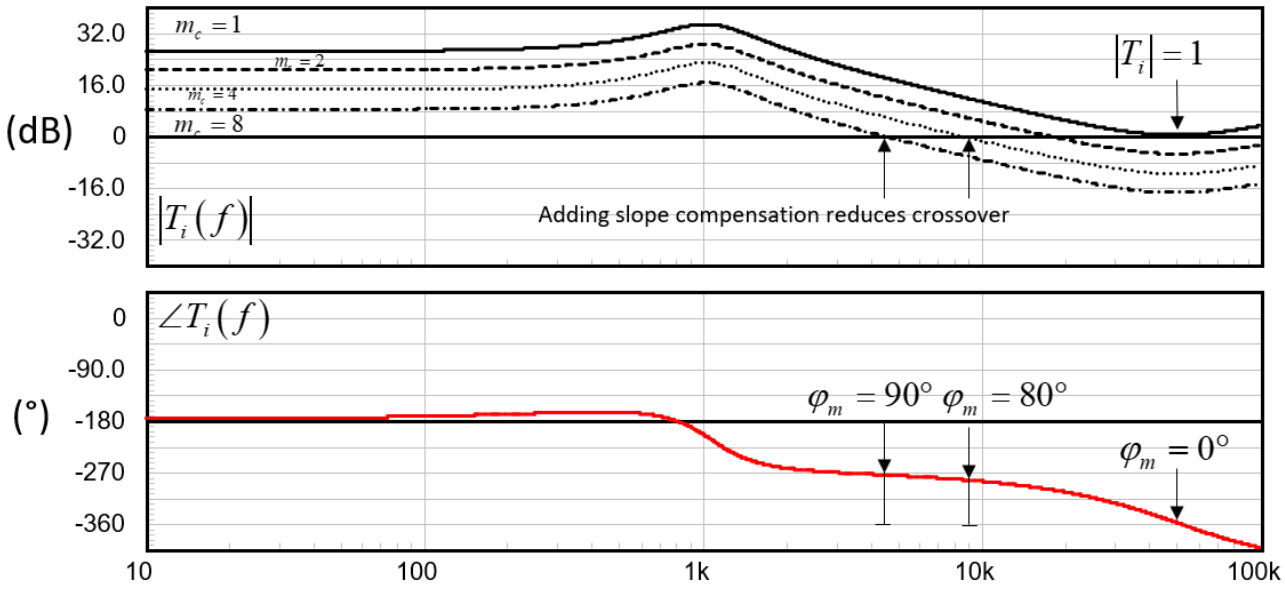

Fig. 26. The current loop gain magnitude and phase are in excellent agreement with the theoretical values.

Conclusion

This article details how the instability observed in a current-mode-controlled converter finds its roots in the inner current loop gain when its crossover frequency is selected too high. The subharmonic poles are actually the result of a right-half-plane zeros pair located at half the switching frequency in the current loop gain which turn into subharmonic poles once the control voltage is involved.

Adding some compensation ramp shifts down the current loop magnitude curve and forces crossover at a more favorable point where phase margin improves. It can be shown that doing so naturally dampens the subharmonic poles in the control-to-output transfer function of a current-mode-controlled converter.

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Appendix – Deriving the Control-to-Peak-Inductor-Current Discrete-Time Response

To determine this sampled transfer function, it is important to realize that the inductor current sampling instant occurs at the power switch turn-off event and *not* at the clock pulse. Fig. 27 details the inductor currents before and after the event. These plots will help us find the expression we need.

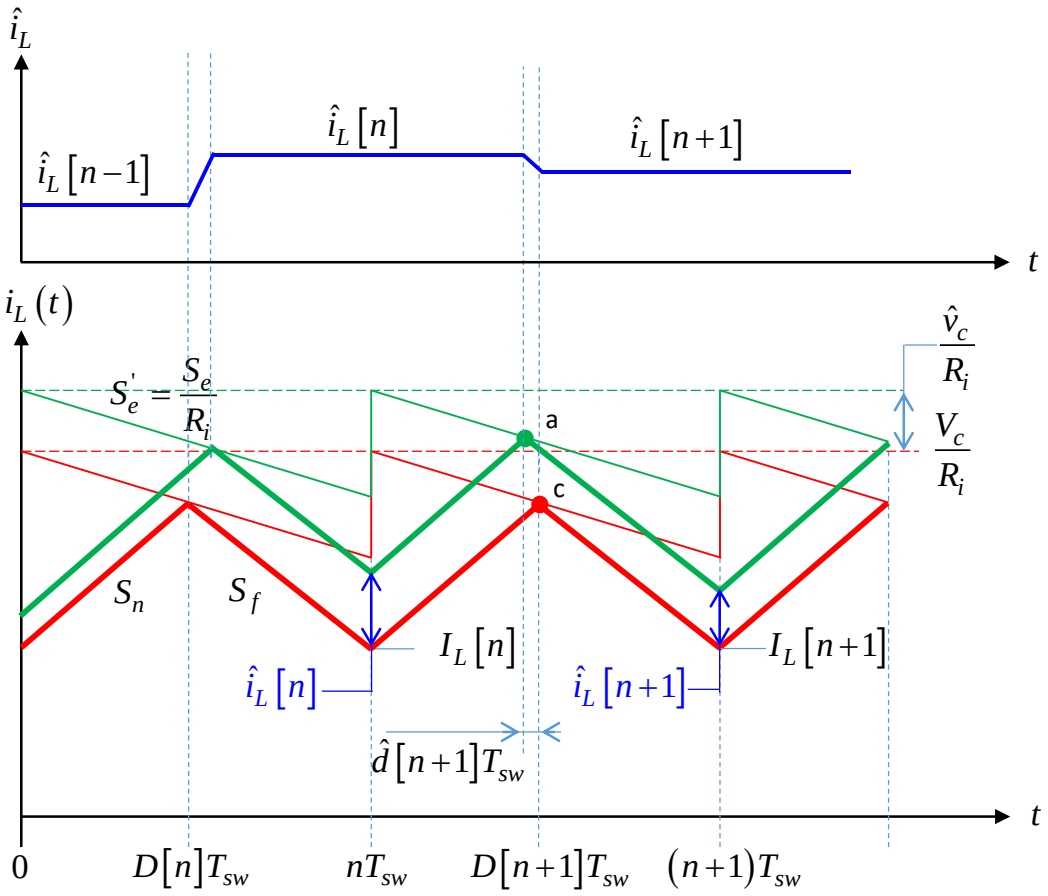

Fig. 27. This is how the inductor current changes after a change in the control voltage v_c.

First, we start from the valley current at sample [*n*] and we slide up to meet point *c*. Or we start from nT_{sw} and slide down the compensation ramp S_e scaled in A/s via R_i. Both results leading to the same point, we can write:

$$I_L[n] + S_n D[n+1]T_{sw} = \frac{V_c}{R_i}[n+1] - S_e' D[n+1]T_{sw} \qquad (43)$$

The important information to consider here is that the inductor valley current at nT_{sw} is part of sample n while the peak where c is drawn belongs to the next sample, n+1. Same remark for the duty ratio D which is already that of sample n+1 when the current ramps up at nT_{sw}. We can perturb this equation by adding a small variation to the variables at stake, I_L, D and V_c:

$$I_L[n]+\hat{i}_L[n]+S_n\left(D[n+1]+\hat{d}[n+1]\right)T_{sw}=\frac{1}{R_i}(V_c+\hat{v}_c)[n+1]-S_e^{'}\left(D[n+1]+\hat{d}[n+1]\right)T_{sw} \qquad (44)$$

This expression mixes dc and ac terms and we are only interested in the latter that we collect in a new expression:

$$\hat{i}_L[n]+S_n\hat{d}[n+1]T_{sw}=\frac{\hat{v}_c}{R_i}[n+1]-S_e^{'}\hat{d}[n+1]T_{sw} \qquad (45)$$

This expression actually describes how the current difference between the red (steady state) and green (perturbed) waveforms propagate sample by sample. From this expression, we can extract the small-signal time event separating the two points a and c:

$$\hat{d}[n+1]T_{sw}=\frac{\frac{\hat{v}_c}{R_i}[n+1]-\hat{i}_L[n]}{S_n+S_e^{'}} \qquad (46)$$

In equation (43), we arrived at point c starting from the inductor current at sample n. We can now go backwards and reach out to c while starting from the valley current at n+1:

$$I_L[n+1]+S_f\left(1-D[n+1]\right)T_{sw}=\frac{V_c}{R_i}[n+1]-S_e^{'}D[n+1]T_{sw} \qquad (47)$$

Similarly, we perturb and keep the ac expression only:

$$\left(I_L+\hat{i}_L\right)[n+1]+S_f\left(1-D[n+1]-\hat{d}[n+1]\right)T_{sw}=\frac{(V_c+\hat{v}_c)}{R_i}[n+1]-S_e^{'}\left(D[n+1]+\hat{d}[n+1]\right)T_{sw} \qquad (48)$$

And we have:

$$\frac{\hat{v}_c}{R_i}[n+1]-S_e^{'}\hat{d}[n+1]T_{sw}+S_f\hat{d}[n+1]T_{sw}=\hat{i}_L[n+1] \qquad (49)$$

We can rearrange the above by factoring the small-signal duty-ratio variation:

$$\frac{\hat{v}_c}{R_i}[n+1]+\hat{d}[n+1]T_{sw}\left(S_f-S_e^{'}\right)=\hat{i}_L[n+1] \qquad (50)$$

If we substitute (46) in (50), we obtain

$$\frac{\hat{v}_c}{R_i}[n+1]+\frac{\frac{\hat{v}_c}{R_i}[n+1]-\hat{i}_L[n]}{S_n+S_e^{'}}\left(S_f-S_e^{'}\right)=\hat{i}_L[n+1] \qquad (51)$$

which gives

$$\frac{\hat{v}_c}{R_i}[n+1]\left(1+\frac{S_f-S_e^{'}}{S_n+S_e^{'}}\right)-\hat{i}_L[n]\frac{S_f-S_e^{'}}{S_n+S_e^{'}}=\hat{i}_L[n+1] \qquad (52)$$

The slopes combination can be expressed as

$$\alpha=\frac{S_f-S_e^{'}}{S_n+S_e^{'}}$$

leading to a lighter formula:

$$\hat{i}_L[n+1]=\frac{\hat{v}_c}{R_i}[n+1](1+\alpha)-\hat{i}_L[n]\alpha \qquad (53)$$

We can now involve the z-transform and write

$$\hat{i}_L(z)\cdot z=\frac{\hat{v}_c(z)}{R_i}\cdot z\cdot(1+\alpha)-\hat{i}_L(z)\alpha \qquad (54)$$

Factoring and rearranging under the form of a transfer function, we obtain our final result, similar to that expressed by equation (13):

$$\frac{\hat{i}_L(z)}{\hat{v}_c(z)}=\frac{1}{R_i}(1+\alpha)\frac{z}{\alpha+z} \qquad (55)$$

It is possible to plot this response via equation (18) using Mathcad and compare it when the Padé approximant in (30) is used as a substitute for $e^{sT_{sw}}$ with the results shown in Fig. 28.

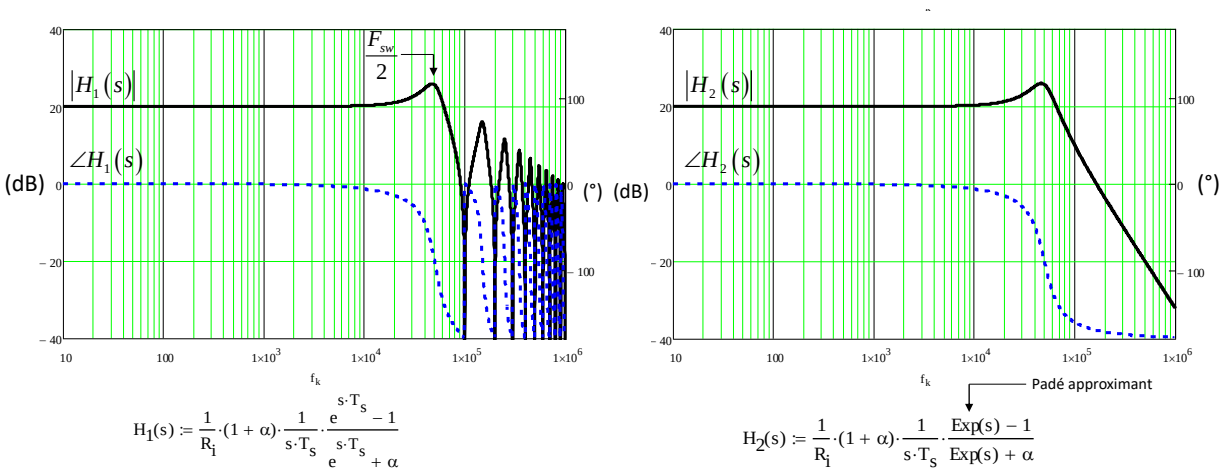

Fig. 28. As expected, the magnitude peaks at half the switching frequency with a severe phase stress at this point.

About The Author

Christophe Basso is a technical fellow at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "Linear Circuit Transfer Functions: An Introduction to Fast Analytical Techniques."

Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 25 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on power supply compensation, see the How2Power Design Guide, and do a keyword search on "compensation."