

## Developing A 25-kW SiC-Based Fast DC Charger (Part 2): Solution Overview

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In the previous installment of this series,<sup>[1]</sup> we introduced the main system requirements for a fast EV charger, outlined the key stages of the development process for such a charger and met the team of application engineers at ON Semiconductor which is developing the charger described here. Now, in part 2 we will take a closer look into the guts of the design and unveil more details of it. In particular, we will review the possible topologies, discuss their advantages and tradeoffs, and learn about the backbone of the system, which includes a half-bridge SiC MOSFET module.

As we've learned, fast EV chargers typically are comprised of a three-phase active rectification front-end to handle the ac-dc conversion from the grid and apply power factor correction (PFC), and of a subsequent dc-dc stage which provides isolation and adapts the output voltage to the needs of the EV's batteries (Fig. 1).



Fig. 1. A high-power fast dc charger with several power stages (left). A high-level architecture of fast EV dc charging systems (right).

In light of the challenging requirements introduced and the current market trends, the Systems Engineering team considered several alternatives to realize these two conversion stages. In the end, the conclusion was to utilize a six-switch active rectifier for the ac-dc stage and a dual active bridge (DAB) for the dc-dc relying on phase-shifted modulation. Both architectures can support the bidirectional functionality and help reap the benefits of 1200-V SiC-module technology, a cornerstone for fast and ultrafast dc chargers. Next, we'll dive deeper into the two main power stages.

### Active Rectification Boost Stage (PFC)

The three-phase six-switch active rectification stage helps achieve a 0.99 power factor with a total harmonic distortion below 7%, which are common requirements in commercial dc charger systems. It delivers a highly efficient bidirectional solution with a low component count compared to three-level PFC topologies such as T-NPC or I-NPC. Overall, this two-level architecture brings a superior cost-performance ratio, while achieving the system requirements.<sup>[2]</sup>

The dc link will operate at a high-voltage of 800 V to reduce peak currents and therefore maximize efficiency and power density (Fig. 2). For this reason, 1200-V  $V_{BD}$  power switches are required with the two-level architecture.

The switching frequency of the system is set at 70 kHz to keep the second harmonic below 150 kHz, which keeps conducted emissions at bay and facilitates compliance with the EN 55011 Class A (EU) and FCC Part 15 Class A (U.S.) norms (which are applicable to systems connected to the ac grid). Among others, these norms set limits on the degree of conducted emissions injected into the grid. Such an approach simplifies the complexity of the EMI filter and renders off-the-shelf solutions a good fit, which fulfills the purpose of this project.

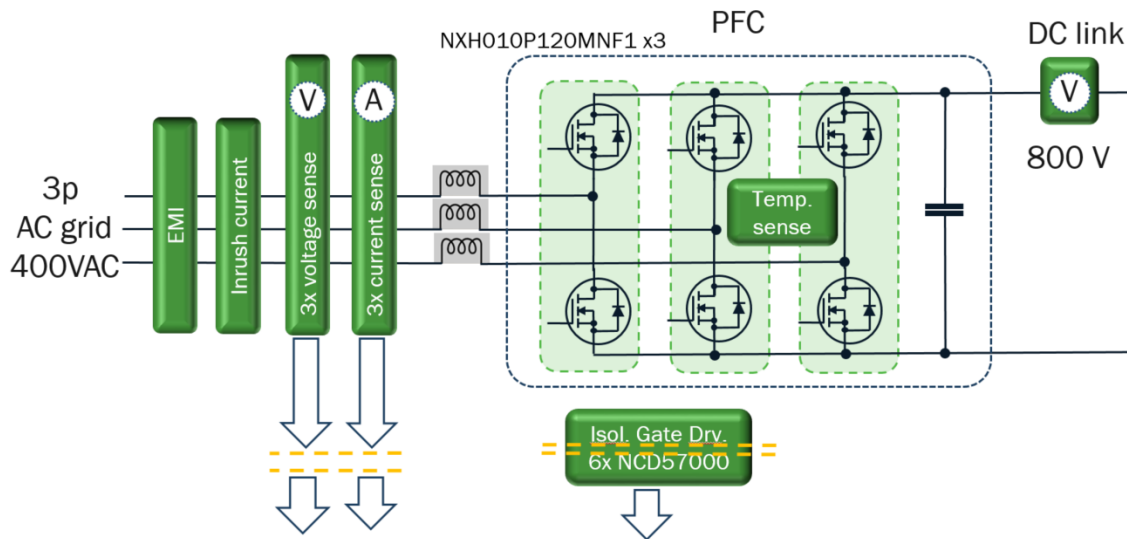


Fig. 2. The three-phase six-switch topology, active rectification stage with power factor correction (PFC), also known as the PFC stage.

### Dual Active Full Bridge (DC-DC)

The DAB dc-dc stage will consist of two full-bridges, a single 25-kW isolation transformer and an external leakage inductance on the primary side that enables zero voltage switching (ZVS) (Fig. 3). Realizing the converter in a single-transformer architecture facilitates bidirectional operation. Furthermore, the symmetry of the converter with a single transformer helps maximize the operating range where ZVS of the power switches is achieved, hence enabling a high efficiency.

This addresses a significant challenge of the project, to maximize efficiency over a wide output voltage range (200 V to 1000 V), with a peak target efficiency of 98% for the dc-dc. The converter operates at 100 kHz, a compromise to keep the switching losses at a reasonable level as well as the core and ac losses of the magnetic components.

Furthermore, the system will run flux-balancing control on the transformer, a technique that removes the need for a bulky series capacitor required to work with the transformer in DAB phase-shifted architecture. In this fast charger converter, such a capacitor would operate under stringent requirements, given the high RMS working current of 50 A, the necessary voltage rating of several hundred volts and the estimated capacitance value of a few tenths of a microfarad. With the existing technology nowadays, all these requirements will result in a large-size capacitor. Therefore, the flux-balancing control strategy helps reduce the size, weight and cost of the system.

Overall, the DAB dc-dc converter offers a well-rounded solution for fast EV chargers and it is becoming a typical solution in this new fast charger market. This topology can deliver high power and efficiency across a broad output voltage range utilizing phase-shift modulation. Furthermore, some developers can leverage their expertise on conventional full-bridge phase-shift ZVS converters as there are similarities between both systems.

An alternative could be the CLLC resonant converter, a frequency-modulated topology typically providing the highest peak efficiencies of converters when operating within limited output voltage ranges. This converter is an adaptation of the LLC to allow bidirectional operation. Nevertheless, the control, optimization and tuning of the CLLC for bidirectional functionality and operation for high output power across a wide output voltage range could become cumbersome and require the combination of frequency-modulation and pulse width modulation.

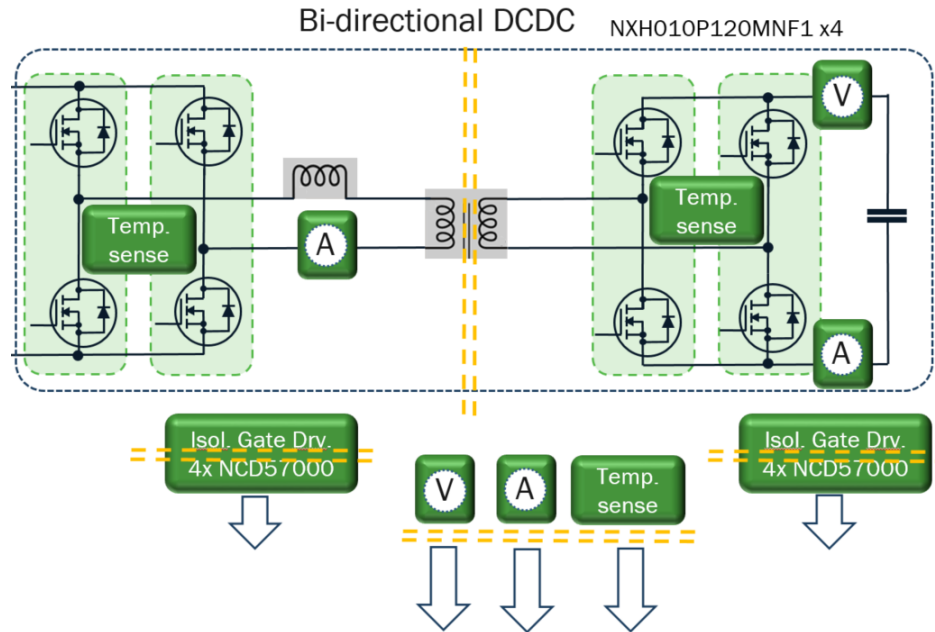


Fig. 3. The dual active bridge (DAB) dc-dc stage. The system consists of two full-bridges with an isolation transformer in between.

### Working Voltages And Power Modules

The dc link between the ac-dc and dc-dc stages will operate at high-voltage (800 V) to reduce current values and therefore maximize efficiency and power-density. The output voltage will swing from 200 V to 1000 V (as previously mentioned). The converters require 1200-V breakdown voltage switches to operate at such voltage levels, as they are based on two-level topologies.

The NXH010P120MNF1 half-bridge SiC-module (Fig. 4) features 1200-V, 10-m $\Omega$  SiC MOSFETs and is the backbone of the PFC stage and dc-dc converter. The module exhibits an ultralow  $R_{DS(ON)}$  that significantly reduces conduction losses, as well as a minimized parasitic inductance to cut down switching losses (compared to discrete alternatives).

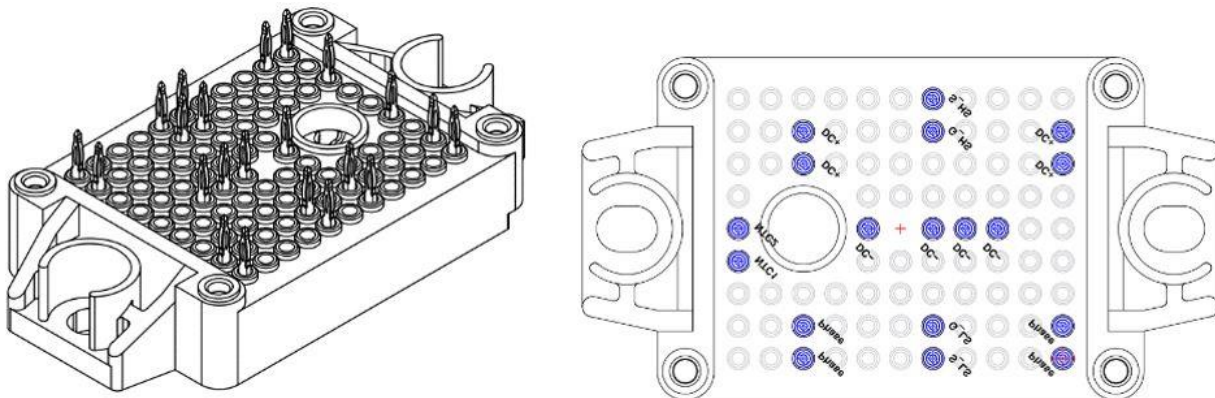


Fig. 4. The NXH010P120MNF1 SiC Module with 2-PACK half-bridge topology and 1200-V, 10-m $\Omega$  SiC MOSFETs is used to realize the ac-dc and dc-dc converters.

The superior thermal conductivity of the power module package increases power-density (versus discrete SiC devices), diminishes the cooling needs and enables a compact and robust solution. The SiC-module becomes an essential element to achieve the >98% efficiency of the ac-dc and dc-dc stages separately in compact and lightweight systems.

In addition, the shrunk magnetic components suitable for the higher switching frequencies that the modules enable, as well as the reduced cooling infrastructure requirements have a positive effect on the cost-per-watt of the complete system. In the 25-kW EV dc charger power stage, the use of fan-based active cooling on the SiC-modules should suffice to effectively dissipate the losses in the system. The selection of the capacitors and magnetic component aims to minimize their cooling requirements while fulfilling the technical specifications.

## Control Mode And Strategy

Digital control will run the system, relying on the powerful Universal Controller Board (UCB),<sup>[3]</sup> which features the Zynq-7000 SoC FPGA and ARM-based chip. Such a versatile control unit helps test and run with ease multiple control methodologies in the digital domain—such as the single-phase-shift, the extended-phase-shift, and dual-phase-shift, as well as flux-balancing on the DAB transformer—and handles all the communications on-board and external. Two UCB units will be used, one for the PFC stage and another one for the dc-dc.

## Drivers

Crucial as well for the overall system performance and efficiency are the gate drivers. In order to get the most out of SiC technology, it is essential to drive the SiC MOSFETs effectively and ensure fast transitions. Unlike with silicon-based devices, SiC MOSFETs typically operate in the linear region (rather than in saturation). One important aspect to consider when selecting the appropriate  $V_{GS}$  is that unlike their Si counterpart, SiC MOSFETs will continue to show a significant improvement in the  $R_{DS(ON)}$  when the  $V_{GS}$  is increased even at relatively high voltages.<sup>[4]</sup>

A  $V_{GS}$  of +20 V for the turn-on is recommended to ensure the lowest  $R_{DS(ON)}$  and significantly reduce conduction losses. For the turn-off, the recommendation is to use -5 V, which reduces losses during the “off” transitions and improves robustness preventing undesired turn-ons.

Additionally, high drive currents are necessary to enable the high  $dV/dt$  suitable for SiC MOSFETs that also help minimize switching losses. With that in mind, the NCD57000 5-kV galvanic-isolated high-current driver was selected for the PFC and dc-dc stages.

The single-channel chip ensures fast switch transitions with +4-A and -6-A source/sink currents and is well ruggedized, displaying high common-mode transient immunity (CMTI). Thanks to the split output, the turn-on and turn-off gate resistances are independent (Fig. 5), allowing for the on and off  $dV/dt$  values to be individually optimized and reduce losses.

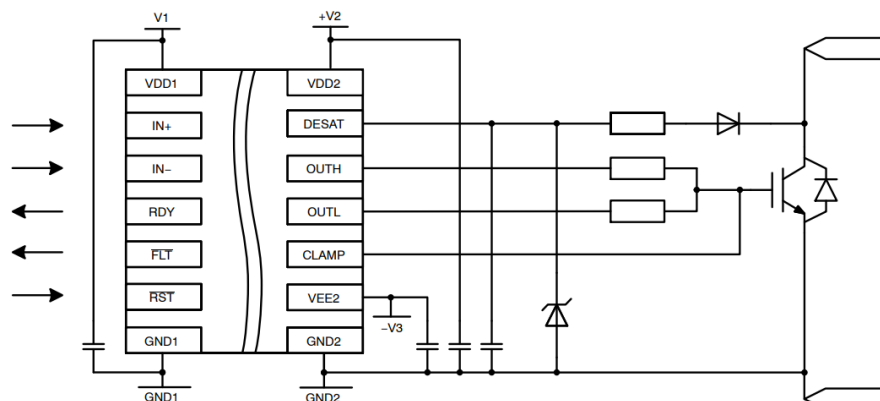


Fig. 5. Simplified application schematic of an isolated gate driver with DESAT protection and split output.

Additionally, the DESAT function on-chip is very convenient to ensure the fast overcurrent protection required for SiC transistors, characterized by shorter short-circuit withstand times compared to IGBTs. The low-side driver system will replicate the high-side as a proven good practice in high-power applications with fast switching systems.

The isolation and the symmetry of the circuitry (high side and low side) help deliver a more robust system by preventing issues stemming from different sources (EMI, noise, transients, etc.). The +20-V and -5-V isolated bias supplies will be delivered by the SECO-LVDCDC3064-SiC-GEVB which showcases industry-standard pin-outs.

### Key Bill Of Materials

Table 1 summarizes the key semiconductor components and functional blocks that will be used for the design.

Table 1. Key semiconductor components featured in the 25-kW EV dc charger.

|                    |  |
|--------------------|--|
| SiC power modules  | NXH010P120MNF1 half-bridge with 1200-V, 10-mΩ SiC MOSFETs <sup>[5]</sup>   |
| Gate driver system | NCD57000 driver <sup>[6]</sup> +20 V/-5 V<br>SECO-LVDCDC3064-SiC-GEVB isolated supply <sup>[7]</sup>   |
| Sensing            | NCD98011 12-Bit SAR ADC <sup>[8]</sup><br>NCID9211 high-speed dual-channel, bidirectional ceramic digital isolator <sup>[9]</sup><br>NCS21xR current-sense amplifier <sup>[10]</sup><br>NCS20034 7-MHz quad op-amp |
| Aux supply         | SECO-HVDCDC1362-15W15V-GEVB high-voltage PSU <sup>[11]</sup>   |

### Bringing Everything Together

Fig. 6 shows how all the system pieces presented above fit together in the actual design to deliver a complete solution. A good understanding of what the actual hardware will look like is provided in Fig. 7.

The PFC stage sits on top of the dc-dc stage, resulting in a compact and well-rounded structure. The overall max. size of these modules together adds up to 380 x 345 x (200 to 270) mm (L x W x H), with the height varying as a function of the assembled inductive parts. Eventually, several of these 25-kW units could be stacked together to achieve higher power levels in an ultra-fast EV dc charger.

### What's Coming

In the upcoming parts of this series, we'll discuss the development of the three-phase PFC stage and the DAB-phase shift converter in further detail, including simulations and other system considerations. Test results will be presented at the end of this series.

For any questions about this part 2 or other parts of this series, write to the authors at this [email](#).



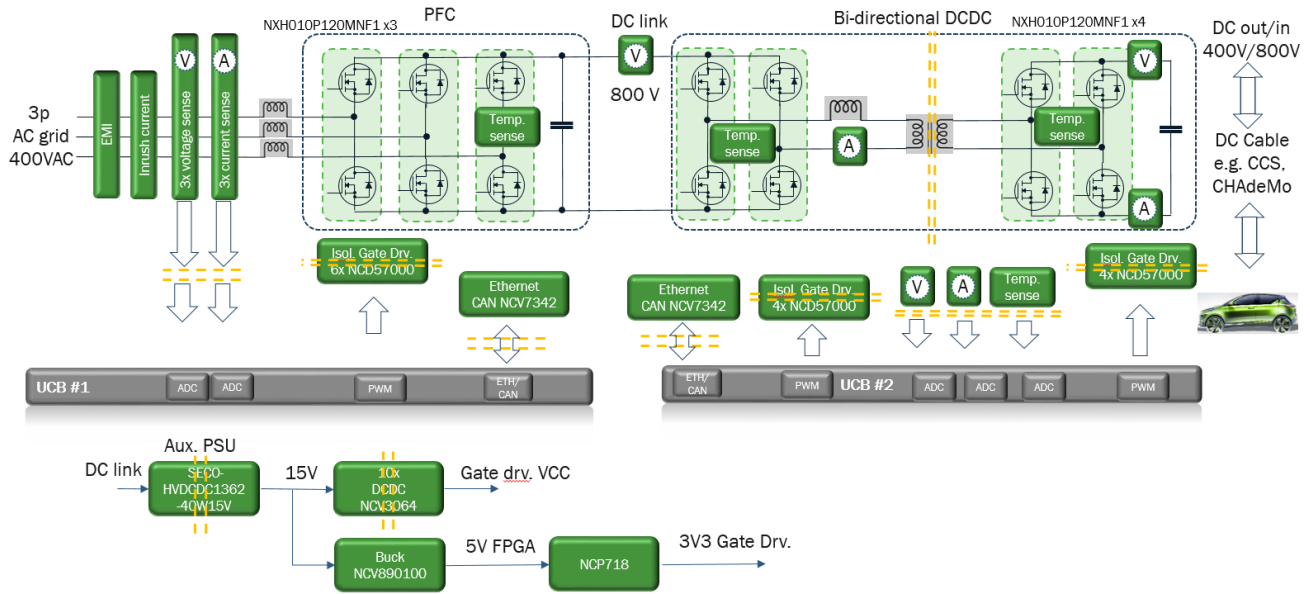


Fig. 6. A high-level block diagram of the 25-kW EV dc charger.

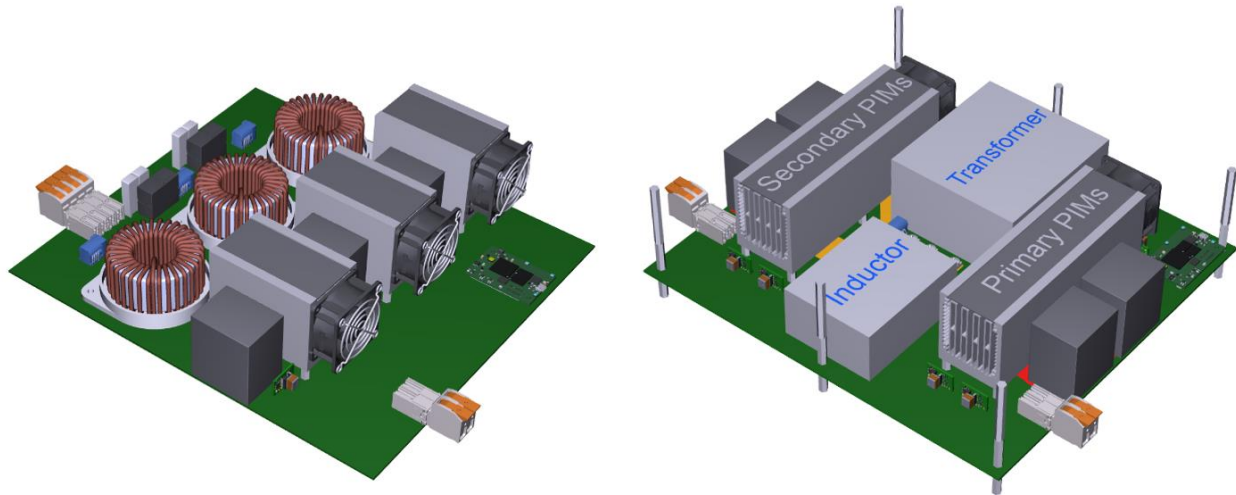


Fig. 7. 3D models of the actual PFC (left) and dc-dc (right) stages. The SiC-modules are located under each of the heat sinks. In the models, the gate driver supplies, the Universal Controller Board (UCB) and passive blocks are visible. Additional views of these components can be seen in an online video.<sup>[12]</sup>

## References

1. [“Developing A 25-kW SiC-Based Fast DC Charger \(Part 1\): The EV Application”](#) by Oriol Filló, Karol Rendek, Stefan Kostrec, Daniel Pruna, Dionisis Voglitsis, Rachit Kumar and Ali Husain, How2Power Today, April 2021.
2. [“Demystifying Three-Phase PFC Topologies”](#) by Didier Balocco, How2Power Today, February 2021.
3. SECO-TE0716-GEVB [product page](#).

4. [ON Semiconductor Gen 1 1200 V SiC MOSFETs & Modules: Characteristics and Driving Recommendations](#), application note AND90103/D.
5. NXH010P120MNF1: SiC Module [product page](#).
6. NCD57000 [product page](#).
7. SECO-LVDCDC3064-SiC-GEVB [product page](#).
8. NCD98011 [product page](#).
9. NCID9211 [product page](#).
10. NCS21xR [product page](#).
11. SECO-HVDCDC1362-15W15V-GEVB [product page](#).
12. "25kW SiC Module Fast EV DC Charger Power Stage" [video](#).

## About The Authors



*Oriol Filló serves as a solution marketing engineer for industrial applications at ON Semiconductor. He is responsible for the marketing strategy of industrial solutions, focusing on robotics and energy infrastructure. He has developed his career in the electronics industry with a focus on power and control, and gathered experience in industrial, IoT and automotive applications.*

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For further reading on designing EV chargers, see the How2Power [Design Guide](#), locate the Application category and select "Automotive".