ISSUE: June 2021

Developing A 25-kW SiC-Based Fast DC Charger (Part 3): PFC Stage Simulation

by Oriol Filló, Karol Rendek, Stefan Kosterec, Daniel Pruna, Dionisis Voglitsis, Rachit Kumar and Ali Husain, ON Semiconductor, Phoenix, Ariz.

In the previous installments in this series,[1,2] we introduced the main system requirements for a fast EV charger, outlined the key stages of the development process for such a charger and met the team of application engineers responsible for this design. Now, it is time to dive deeper into the design process of the 25-kW EV charger. In parts 1 and 2, we discussed the motivations, specifications and topologies chosen. In this part, we will walk through the simulations of the ac-dc conversion stage, also described previously as the three-phase active rectification front-end, and referred to here more simply as the PFC stage.

As discussed in the first part, power simulations assist in validating assumptions before designing or building hardware and help uncover possible issues or behaviors to be considered in the design and selection of components, PCB layout and even in the test procedures as we will see. For example, simulation allows us to test assumptions about working voltages, currents, switching frequency, power dissipation (losses), cooling requirements and control algorithm.

Beyond verification, the outcome of the simulation serves to address other important steps in the development process such as selection of passive components. A solid simulation reduces debugging and hardware iterations in the development cycle, accelerating the product development.

Before Clicking "Run"—Preparing The Simulation

Power simulations do not begin with the click of the Run button—they start way before. Several elements need to be ready before running the simulations. Here are the most important ones, and how we addressed them.

Goals And Purpose Of The Simulation

Having clear goals and purpose for the simulation upfront is crucial for its success. The purpose is defined by the questions to be answered. The goals will affect the detail of the required simulation model, as discussed in the next section. In this project, the power simulations for the PFC mainly helped the engineering team address the following requirements:

- Verify PFC stage functionality before designing hardware
- Confirm dc output voltages, currents and power are delivered for all operating points defined in the specification. All other system requirements should be fulfilled.
- Confirm that efficiency target with the defined switching frequency (70 kHz) is fulfilled
- Estimate power losses
- Establish gate-drive gate resistors' values (starting point for the prototypes)
- Validate PFC chokes' requirements/parameters (to be passed on to the inductor manufacturer)
- Select dc link capacitor based on ripple current (critical), ESR, capacitance and voltage rating.

Power Simulation Model And Software

The simulation model is the backbone of this effort. The model includes the parameters and functions that reproduce the behavior of each of the elements in the circuit. Every element in the model, e.g.: switch, diode, gate drivers and passives can be modeled with different levels of detail. There might be components and behaviors that are complex and cumbersome to model. A more-complex model takes longer to run. A simpler simulation gives the capability to simulate many different states of the system to answer various questions.

The approach in the development of the charger has been to simplify the models to enable fast simulations and an agile design process. Of course, it is important to take into consideration the accuracy of the model when evaluating the results. The models of components that do not influence functionality and electrical values are simplified, while critical elements are modeled with greater accuracy.

Simulation Software

Power simulations in power electronics are typically based on the known SPICE models of the components that influence the power management and conversion in the system. In this project, we use Simetrix, a mixed-mode circuit simulator offering enhanced SPICE for fast convergence.

Input Parameters

The last essential element of a simulation is the evaluation of specific components and parameters that provide degrees of freedom in the design. The simulations help determine the best combination of these parameters that fulfill the application requirements. In this design, the most important elements selected and used as inputs for the simulation were:

- PFC inductor: The value of this component was initially estimated based on the application requirements, input voltage, application power and current. Additionally, it needed to be of a reasonable size and use commercially available core material. The team calculated that the inductance would be in the range of several dozen microhenries.
- Output capacitors: In evaluating commercially available capacitors, device options were filtered based on the current and voltage ripple requirements. Because of the high-voltage levels (up to 1000 V), electrolytic capacitors were eliminated because they would require serial connection of capacitors to support the voltage.
- Switching frequency: This value was pre-selected for the given inductance values and the grid requirements. As described in part 2, 70 kHz was a good tradeoff between efficiency and compliance with EMI regulations.

Several initial values for these parameters were selected via various approaches for validation through simulation. Approaches used to identify the initial values included: standard inductor/capacitor design calculations, benchmarking with existing designs and scientific literature, and drawing on previous experience. Triangulating between these multiple approaches resulted in good educated guesses for the parameters, which will be listed in the simulation results section below.

Simulation Set-Up

This section will provide an overview of the simulation model (and sub-models) created and developed for this project and highlight which behaviors are included in the models and which ones are left out. Also we'll explain the measures we've taken in cases where the relevant behaviors are not part of the basic simulation model. A table at the end provides a summary of our findings.

Fig. 1 shows the simulation model in Simetrix which includes both the power model (top) and the PWM modulator model (bottom). (More details on this algorithm will be provided in upcoming installments.)

The PWM modulator relies on a typical space vector PWM algorithm, which helps to simplify the control loops and renders them addressable with PI-based regulators. To keep the model simple, the measured mains phase voltages are used as inputs to the controller. In the actual hardware system, a phase-lock-loop will be used in the digital domain to measure the instantaneous mains reference voltage.

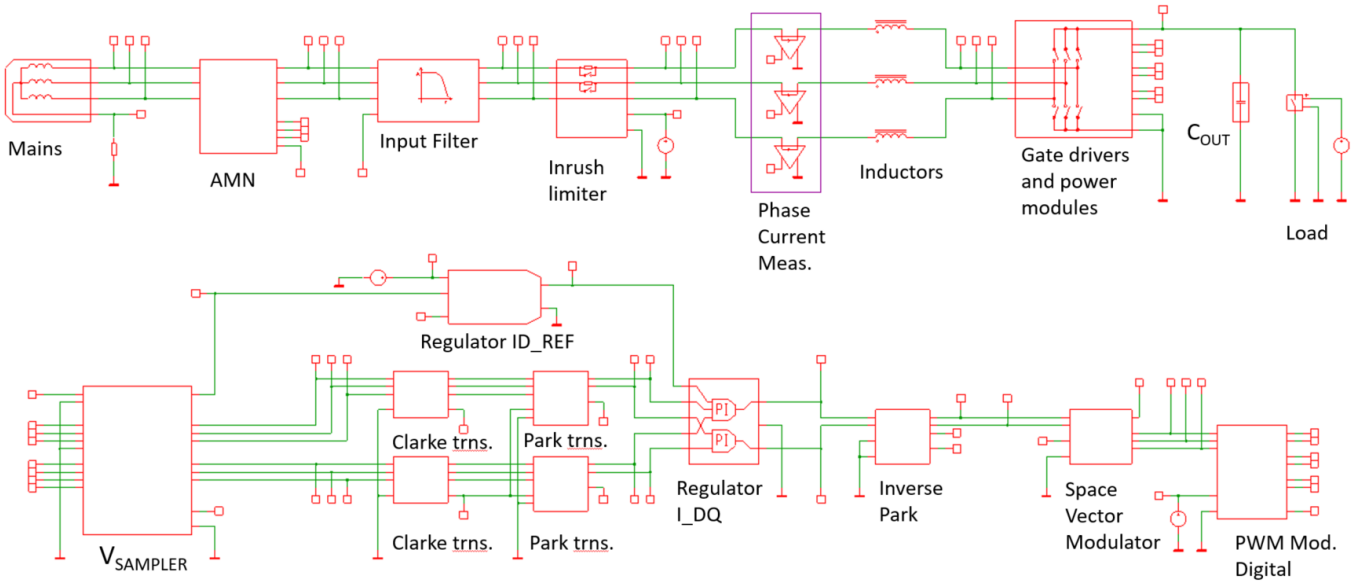


Fig. 1. The Simetrix model of the PFC stage.

Mains And Mains Network Model

The mains model consists of three configurable voltage sources, generating 50-Hz/60-Hz sine waves shifted by 120°each. The initial phase can be modified, which is useful to validate the inrush current protection circuit, for example. For simplicity, most of the simulations in this model have been performed with a resistive load.

In the case that a basic evaluation of differential conducted emissions and verification of the input filter are desired as part of the simulations, an artificial mains network (AMN)/line impedance stabilization network (LISN) (per CISPR22) could be inserted between the mains and the filter. The discussion of this element is beyond the scope of this series. The model of the grid also includes the ac grid impedance, which has an effect on the control, so including it here improves the simulation.

Input Filter

The input filter is the first element of the converter. The simulation uses a simplified model (see Fig. 2), as no design or tuning of the filter will be done. As discussed in part 2, an off-the-shelf-unit will be utilized.

Including the filter component in this simulation brings two main advantages. First, the output impedance of the filter plays a role in the control loop of the PFC; considering its effect helps to design a stable PFC stage. This is often a problem when the EMI filter is not considered in the design phase.

Secondly, we account for the power losses dissipated in the filter, for a more accurate estimate of the efficiency and thermal management needs of the system. Again, one of the goals of this simulation is to verify and validate our control strategy, as well as elements that can have an impact on performance.

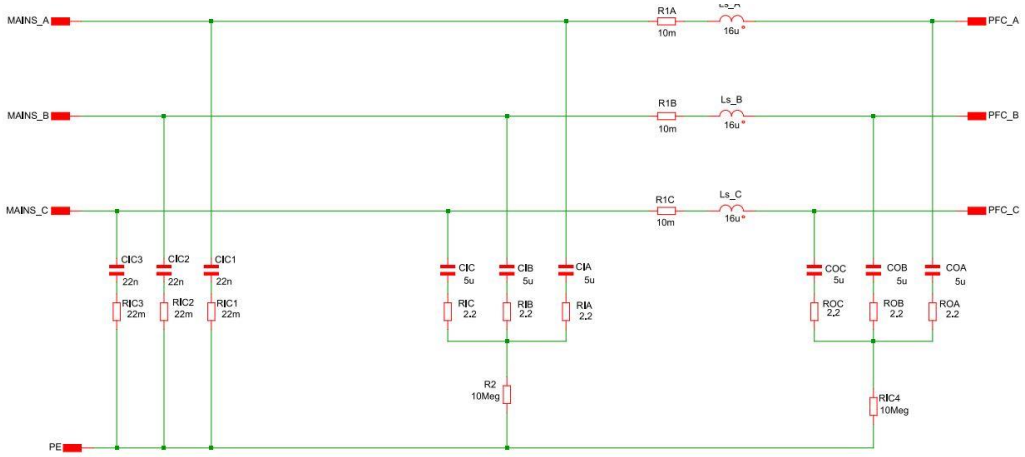


Fig. 2. The model of the input filter.

Inrush Current Protection

The inrush current protection is a key element of the EV-charger power systems and it is worth including as part of the simulations. The model implementation is rather simple and consists of a parallel relay and resistor in two of the three phase lines, as in Fig. 3. As the system does not incorporate a neutral path, there is no need for a resistor on the third phase. (The resistor R in Fig. 1 represents the parasitic resistance of the connection.)

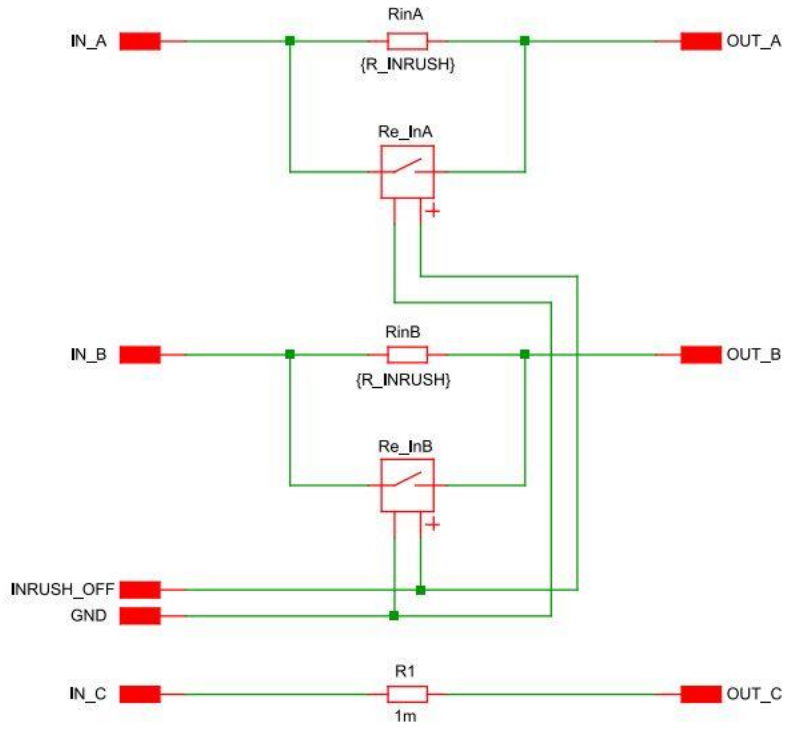


Fig. 3. The inrush current limiter model.

In general, simulating the inrush current will help verify the maximum energy dissipation expected in the resistors and thus help in the selection of the actual components.

PFC Inductor Model

SPICE simulation software provides built-in inductor elements, but these can be simple and, in this case, do not account for important behaviors of inductors in power systems, in particular inductor saturation and self-resonance effects. For our model, we used the model in Fig. 4 that incorporates these elements in the simulation. The inductor saturation effect is modeled in a look-up table, providing the relation between the magnetic relative permeability of the inductor (μ_r) depending on the magnetic field strength (H). The winding losses are modeled with a series resistor. Fig. 4 provides more details on how the elements in the model work together.

The core losses are not included in the simulation model because most approaches to account for these losses are either too complex or too inaccurate. Core losses will be evaluated during the hardware testing with the first prototypes. Using the first hardware prototypes to iron out or fine tune some of the design aspects is expected and not only for the inductors.

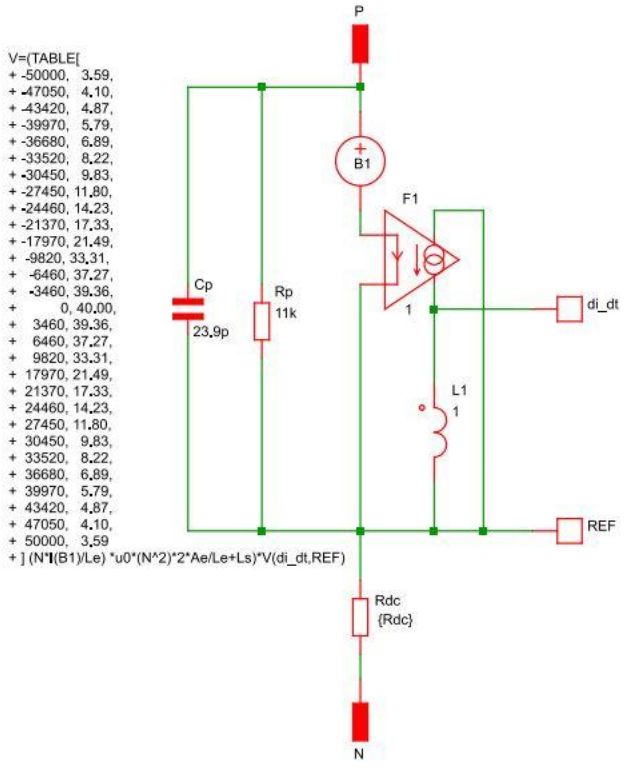


Fig. 4. The inductor model with saturation and self-resonance effect. The saturation effect (or inductance value variation at different operating current values) is modeled by a look-up table and standard magnetic design formulas: (1) $L = \mu_0 \mu_r (A_e/L_e) N^2$, (2) $H = (N \times I)/L_e$ and (3) Look-up table $\mu_r = f(H)$. B1 represents the voltage across the inductor, and it is given by (4) $V_L = L \times dI/dt$. Formula (1) provides L and dI/dt is derived by using (4) in the test inductor L1 (1 H). F1 is a current-driven current source with 1:1 ratio, outputting the same value as measured in the inductor model. Because L1 = 1 H it follows that dI/dt =V(di_dt-REF). F1 does not have any effect on the inductor model, it is introduced to derive dI/dt in the system used to compute $V_{L,PFC}$ at each point*. L(B1, F1 and L1), Cp and Rp model the self-resonance behavior of the inductance.*

Power Stage Model

The power stage is the backbone of the power converter and therefore a central part of the simulation model. It incorporates the three half-bridge SiC-modules as well as the gate drivers. The driver system will significantly impact the performance of the system (even more so for SiC-based systems), and therefore it is highly recommended to include it in the simulation—at least to some extent. One challenge is that existing gate driver

models are often very complex so they can be used for simulations with other purposes. In general, for system power simulation and, more specifically, for the goals of this project, a simplified model of the gate driver was sufficient and one was built.

Even though detailed I-V characteristics are usually not readily available in drivers datasheets, using the specified driver output capability (sink/source peak currents) for certain given points, in combination with rise and fall time information, results in an approximation of the output characteristic that improves the accuracy of the simulations while still providing acceptable computation time. This approach is used to simulate the NCD57000 driver (Fig. 5).

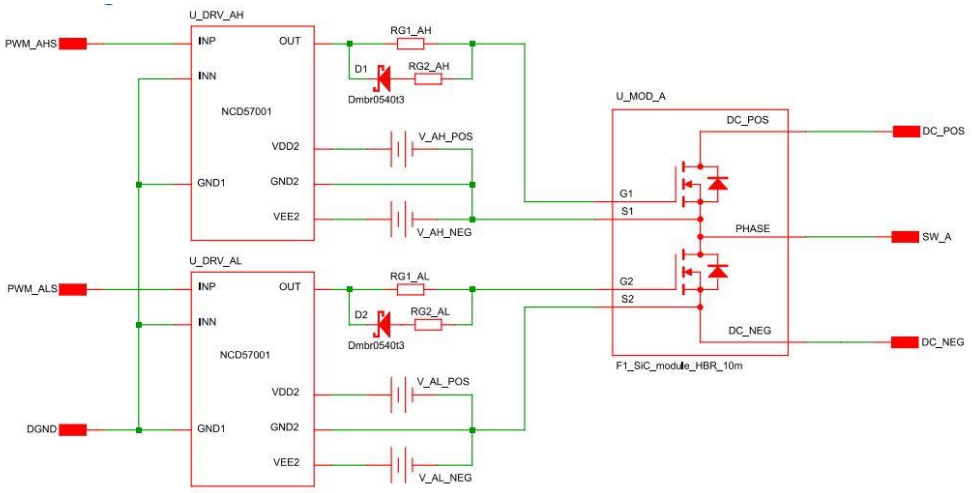


Fig. 5. The power stage model—phase A.

Power Module

Modeling the SiC-MOSFETs on the power modules is obviously a crucial step of the power simulations. Like the gate drivers, very detailed physical models for the SiC MOSFETs in the module exist, and these are typically used for device characterization and extraction of device parameters for any working condition. These models extend the information disclosed in datasheets, which is typically provided at specific operating points.[3]

However, in our simulation scheme, we need six different switches and using physical models would make the simulation painfully slow or inviable. Convergence issues often arise as well. A practical approach in this case is to create a simplified model that incorporates the main elements and behaviors that have a significant and relevant impact on the power system (Fig. 6).

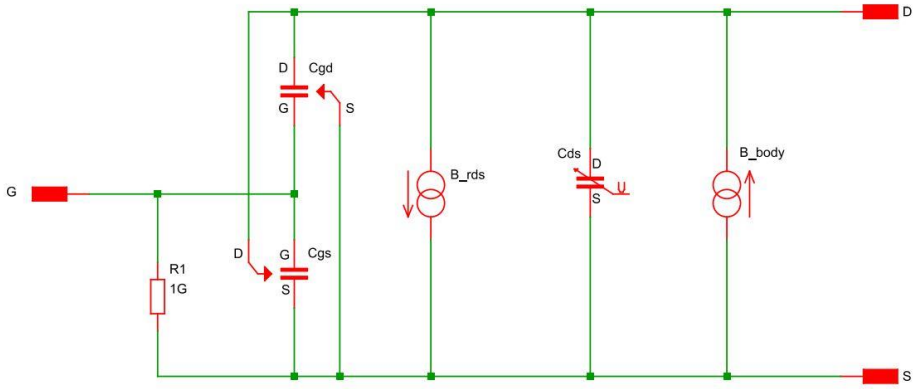


Fig. 6. The simplified MOSFET model.

The resulting model accounts for the following key elements in a SiC-MOSFET: the three main parasitic capacitances, the $R_{DS(ON)}$ and the V_F drop of the body diode. These are not single values but models with characterization curves for different working conditions.

Note that the values of these parasitic capacitances strongly vary with V_{DS}. The V_{DS} dependency is typically provided in charts in the device datasheet, but some derivation is necessary. The parasitic values are provided as C_{ISS}, C_{OSS} and C_{RSS}, so these formulas are used to calculate the model values:

$C_{gd} = C_{RSS}$

$C_{gs} = C_{ISS} - C_{RSS}$ (C_{ds} shorted)

$C_{ds} = C_{OSS} - C_{RSS}$

Fig. 7 illustrates the model created and utilized in this project (alternative approaches exist) which basically relies on a look-up table to reproduce the nonlinear curve of the capacitor's value.

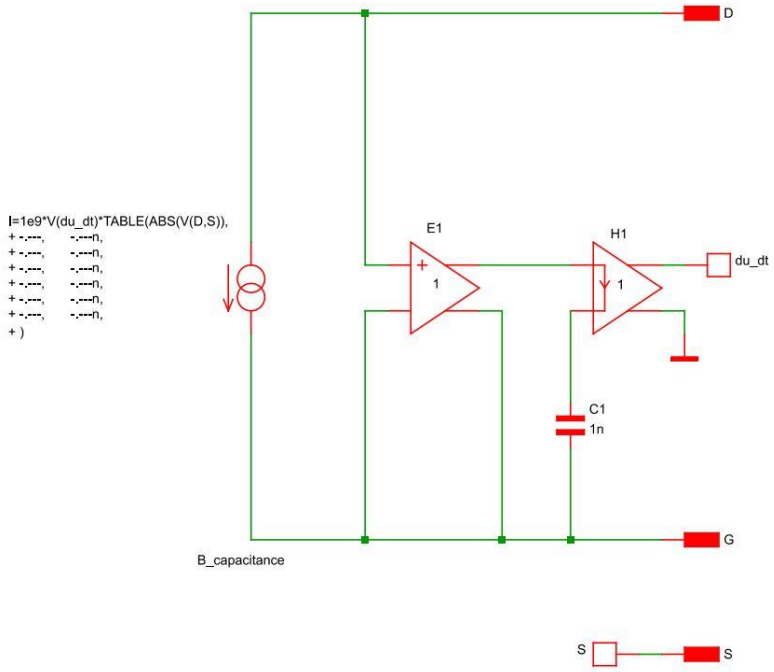


Fig. 7. The C_{gd} model. C_{gs} and C_{ds} have an identical model with different values.

The $R_{DS(ON)}$ of the SiC-MOSFET is strongly dependent on the gate voltage (V_{GS}), and the behavior is included in the model as "B_rds". Although V_{GS} is the principal factor affecting the $R_{DS(ON)}$ value, it also varies to a lesser degree with instantaneous I_D and V_{DS}; in this simulation these factors are disregarded.

The V_F-current characteristic of the body diode can be easily modeled using an arbitrary current characterized with a look-up table. The current is dependent on the body diode V_F. The body diode V_F characteristic might not be necessary for all applications, but in a three-phase PFC stage the body diode is actively used in the rectification, and its V_F-current behavior significantly influences the setting of the switching dead time, playing an important role in overall performance. The reverse recovery of the diode is not included.

It's important to note that the basic SiC MOSFET model does not include the parasitic inductances and resistances present in the device's pins. So adding an internal gate connection resistance may help to more accurately reproduce the switching characteristics (dV/dt levels) and thus the selection or optimization of the

gate resistor. Secondly, modeling the parasitic inductances is definitely recommended to accurately reproduce voltage spikes during operation, but it is typically not crucial for the system-level verification, and the switching behavior can be fine-tuned in hardware by adjusting the gate resistance value.

Table 1 summarizes the contents of the simulation model as well as the expected results for each of the blocks. As discussed, the results should achieve the simulation goals and answer our design questions.

Table 1. Simulation model summary: included elements and simulation outputs.

Simulation model	Elements in simulation model of PFC stage	Simulation outputs
Mains	Small bypass resistor.	
Input filter	Simplified. Does not serve to fine tune the filter, but to consider its effect in the power design (losses). An off-the-shelf filter will be used for this project.	P_{LOSS,R_INRUSH} (resistive). Output impedance impact on PFC control loop stability
Inrush current protection	Start-up resistors and losses on the closed relay.	$I_{PHASE,PEAK}/I_{PHASE,RMS}$ in the system. Both should be compliant with regulation. Selection of resistor component ($P_{LOSS,MAX}$ and I_{PEAK}).
PFC inductor model	Not built-in in Simetrix. Model includes saturation and self-resonance effect and winding losses, but not core losses.	Prove functionality of PFC stage. Check $I_{PHASE,PEAK}$ and $V_{PHASE,PEAK}$. Verify control loop stability, requirements for signal processing of voltage/current.
Power stage		
Driver model	Significant to include, affects performance (especially with SiC). Simplified from the original driver model—only gate-driver output characteristic (approximation with datasheet source/sink capabilities and rise/fall times).	Reproduce switching characteristics of SiC transistors. Basically, dV/dt levels and transition V-I curves.
Power modules	Simplified. • C_{gd}, C_{gs} and C_{ds} • $R_{DS(ON)}$ for channel – curve • $R_{DS(ON)}$ for body diode – curve • Not included: reverse-recovery diode.	Peak currents/voltages and $P_{LOSS,\ MODULES}$.

Simulation Results

Having completed the laborious and time-consuming task of building the simulation model, we jump into the fun part—using it and evaluating the results.

In order to answer our questions, a series of simulations have been carried out with the variables summarized in Table 2. In the following sections we will present the results obtained, our observations on these results and the design decisions based on them.

For the sake of clarity, Table 3 at the end of this part 3 wraps up and summarizes all these explanations and descriptions in the results that follow.

Table 2. Key variables in simulation of PFC stage.

V_{PHASE} (phase-to-neutral)	207 V, 230 V and 253 V, 50 Hz
Inductor and capacitor (The section above on simulation preparation, labeled "Input Parameters," summarizes the process to derive these initial values.)	L_{PFC}: 245 µH, 6.6 mΩ, C_{OUT}: 4 × 470 µF, 91 mΩ, 450 V (electrolytic). Series/parallel connection ~ 900 V
	L_{PFC}: 180 µH, 11.3 mΩ C_{OUT}: 130 µF, 1.3 mΩ, 900 V (film)
	L_{PFC}: 130 µH, 10 mΩ C_{OUT}: 130 µF, 1.3 mΩ, 900 V (film)
V_{OUT}	800 V
P_{OUT}	26.5 kW
Drivers	+20-V/-5-V supply
	Gate resistors source 1.8 Ω, sink 100 kΩ
f_s	70 kHz (PWM modulator clock = 84 MHz)
Modulation	Space vector modulation (SVM) for instantaneous PWM sequence
Dead time, pulse width	Fixed 142.8 ns, minimum pulse width 166.7 ns
Inrush	Relay closed contact resistance 10 mΩ

PFC Stage Efficiency

System efficiency is a key area and result of the simulations. Figs. 8, 9 and 10 show the efficiency values and the corresponding losses. As expected, higher input voltage results in higher overall efficiency because I_{PHASE} decreases (Fig. 8).

With respect to the results with different inductors, it might seem that the higher inductance values would lead to higher efficiencies. However, there are many other elements influencing these results. This is an example of how simulations are helpful. It would be cumbersome to estimate efficiency with calculations and consider all the elements for different operating points. Fig. 10 provides detail on the winding losses; the differences between the winding losses are lower than the differences between total system losses for the inductance values.

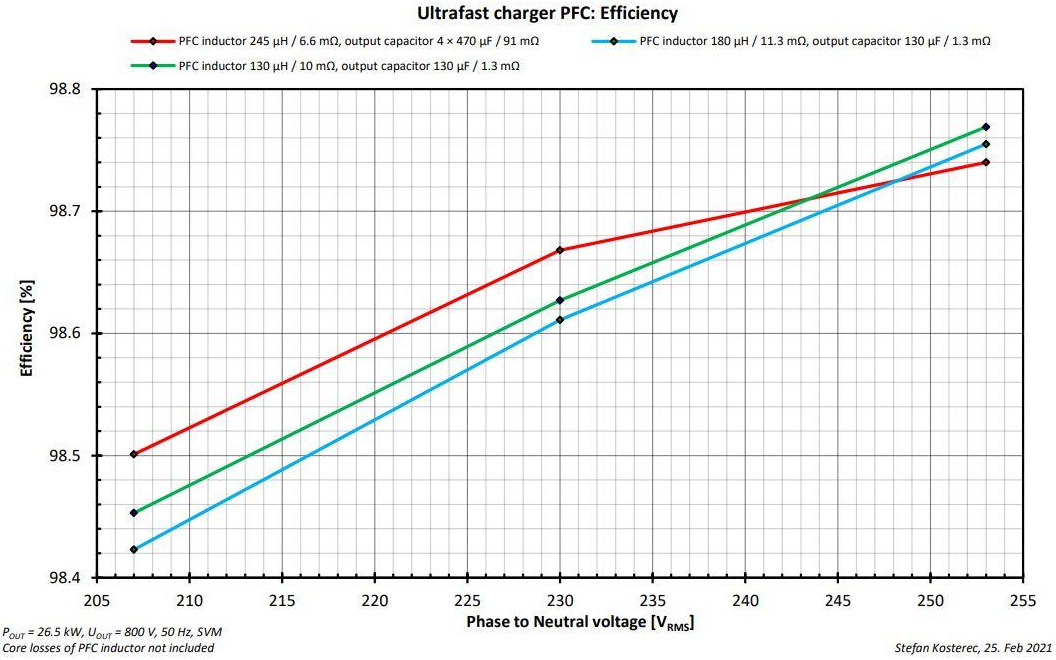


Fig. 8. PFC stage efficiency as a function of input voltage and inductor and output capacitor values.

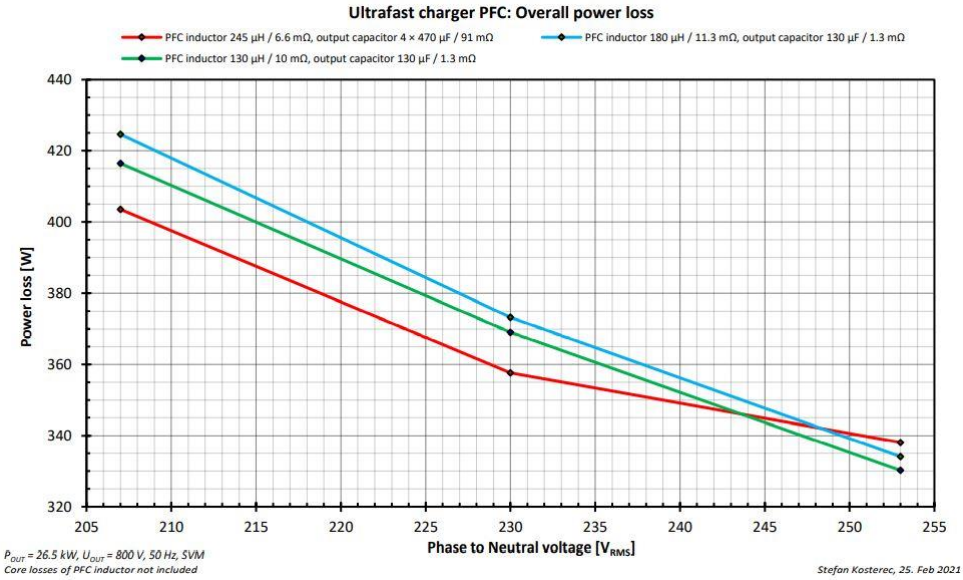


Fig. 9. PFC stage losses as a function of input voltage and inductor and output capacitor values.

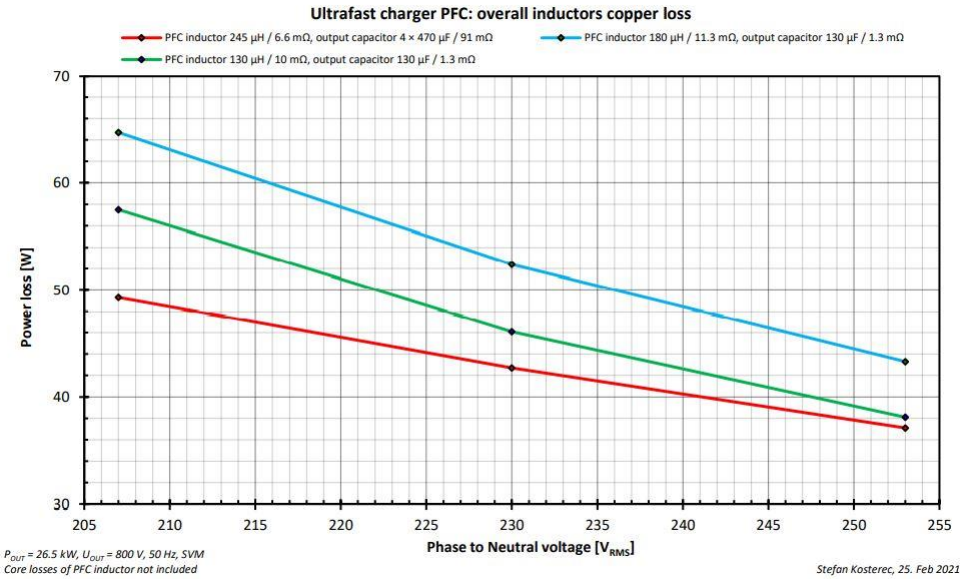


Fig. 10. PFC stage inductor losses as a function of input voltage and inductor and output capacitor values.

Focusing on the power module losses, the simulations reveal interesting information (Fig. 11). The dissipated losses on the module decrease along with the decrease in the inductance value. This could be due to the fact that lower inductance values lead to higher current ripple, and with the higher ripple lower turn-on current is present, which reduces the switching losses along with it.

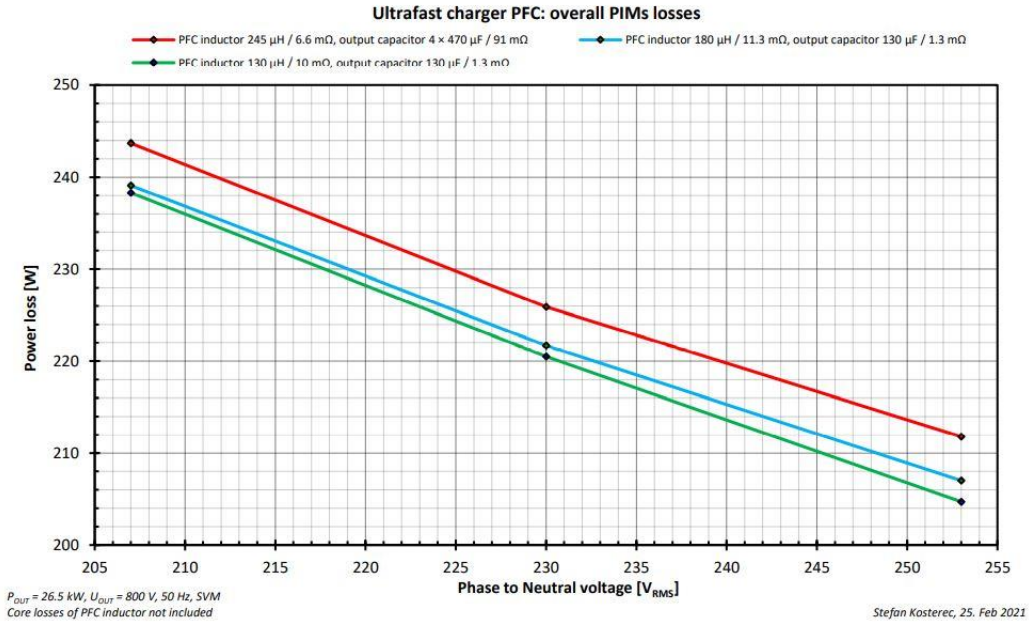


Fig. 11. Overall losses for PIM modules as a function of input voltage and inductor and output capacitor values.

Nevertheless, there is no direct relationship between power module losses and inductance value, as the regulation process and PWM scheme and other factors also play a role. Simulation, based on accurate models, helps estimate the results even if the actual relationships cannot be directly identified.

Most revealing and interesting is the distribution of losses across the multiple elements in the model (Fig. 12). The distribution helps us clearly understand the main drivers of the losses and which areas we could focus on to improve the efficiency—if needed at all. In our case we have proved that efficiency is above 98% for all cases, so no major issues need to be addressed in terms of efficiency. With these results at hand we can select the solutions that will best fulfill the rest of the system requirements.

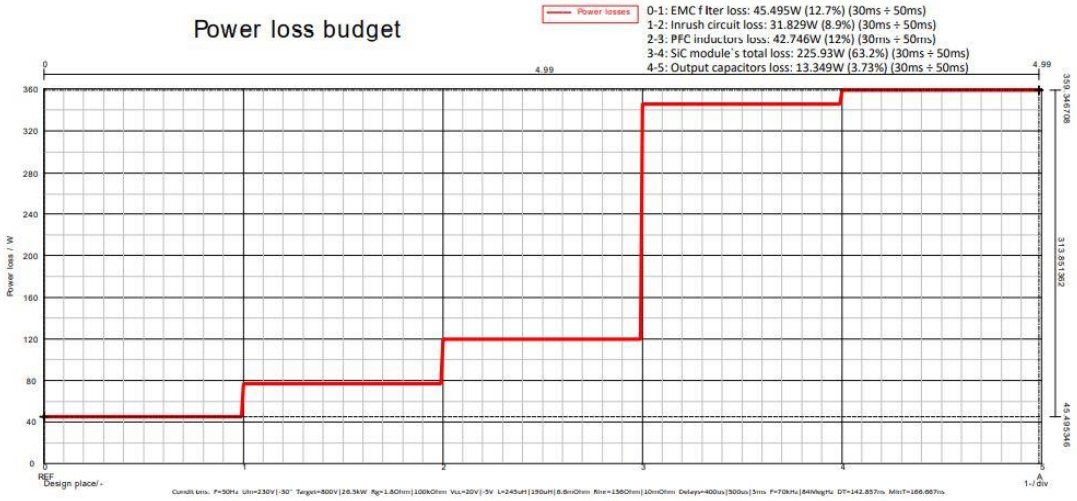


Fig. 12. An example of a power loss budget. Main conditions for this simulation are V_{IN} = 230 V, P_{OUT} = 26.5 kW, V_{OUT} = 800 V and the inductor and capacitor set = 245 µH and 4 x 470 µF. Simulation time is 50 ms. Time window considered for the energy loss (power loss) computation is from 30 ms to 50 ms (as indicated by "30ms % 50 ms" in the key), in order for the system to be running in steady state.

Inrush Current Simulation

The main purpose of the inrush current control simulation is to identify peak and RMS currents and the power dissipation on the current-limiting resistor at start-up. This will help, among others things, to validate the selection of the inrush resistor.

Generally, the peak phase current is limited at start up (within 100 µs) to a multiple of the nominal value. The maximum RMS phase current is also limited by setting a period (of a few seconds) to wait before repeating startup.

Figs. 13 and 14 show the results for our system in a worst-case scenario: mains phase-to-neutral voltage is 310 Vrms, mains phase A is shifted -30° from the zero point and we have a fully depleted 450-µF output capacitor. Simulations show that repeated start-ups should have a cool-down time of 4.19 s to remain below the 7-W limit (inrush resistors' power rating). Nevertheless, typically the charging system will not be start up repeatedly during short periods of time (seconds).

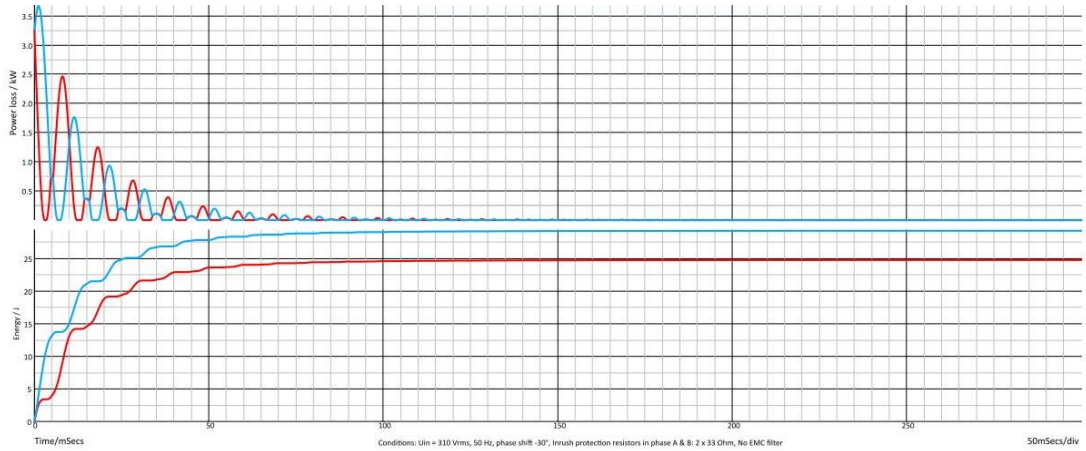


Fig. 13. Inrush current protection. Examples of startup waveforms showing power loss (top) and energy dissipation (bottom) under worst-case conditions, C_{OUT} = 450 µF with inrush protection activated and V_{IN} = 310 Vac. This protection consists of 2 x 33-Ω resistors in series with each phase (four resistors total). Red trace: power and energy on one inrush resistor (phase A). Blue trace: power and energy on one inrush resistor (phase B). Phase A dissipates 24.81 J and phase B 29.29 J, which with the 7-W limitation translate into 3.55 s and 4.19 s cool-down times.

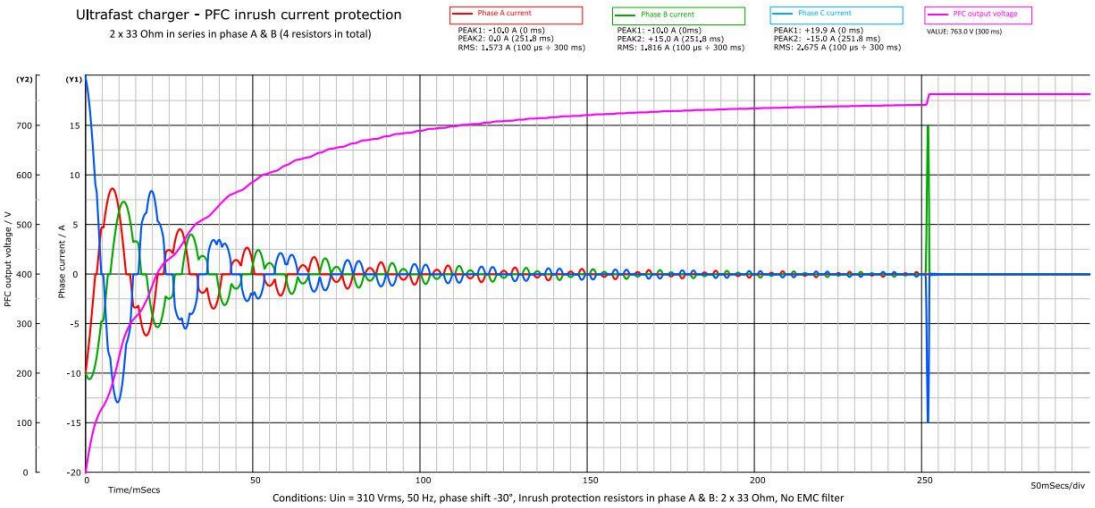


Fig. 14. Inrush current protection. Input currents on phases A & B and PFC output voltage at startup with inrush protection activated. Same conditions as Fig. 13 with respect to protection circuit and C_{OUT}.

PFC Parameters

The power factor is a key requirement, as regulations require power factors in excess of 0.99 under full load condition for fast EV chargers. Fig. 15 helps verify that all the designs fulfill this requirement and Fig. 16 shows the perfectly sinusoidal current waveforms and the I_{PHASE}-$V_{INPHASE}$ dependencies.

The $I_{PHASE,RMS}$ values remain almost the same regardless of the inductor value (Fig. 17), which coincides with the overall efficiency result (Fig. 8) as variations between inductor versions are very small as well. A slightly larger variation can be observed on the peak currents (Fig. 18), but $I_{PHASE,PEAK}$ values are not critical for the power losses because $I_{PHASE,RMS}$ is the main current component used to estimate losses and efficiency.

This is in line with the fact that higher currents in the system will result in higher losses. A similar pattern is present in the total harmonic distortion (THD) results (Fig. 19).

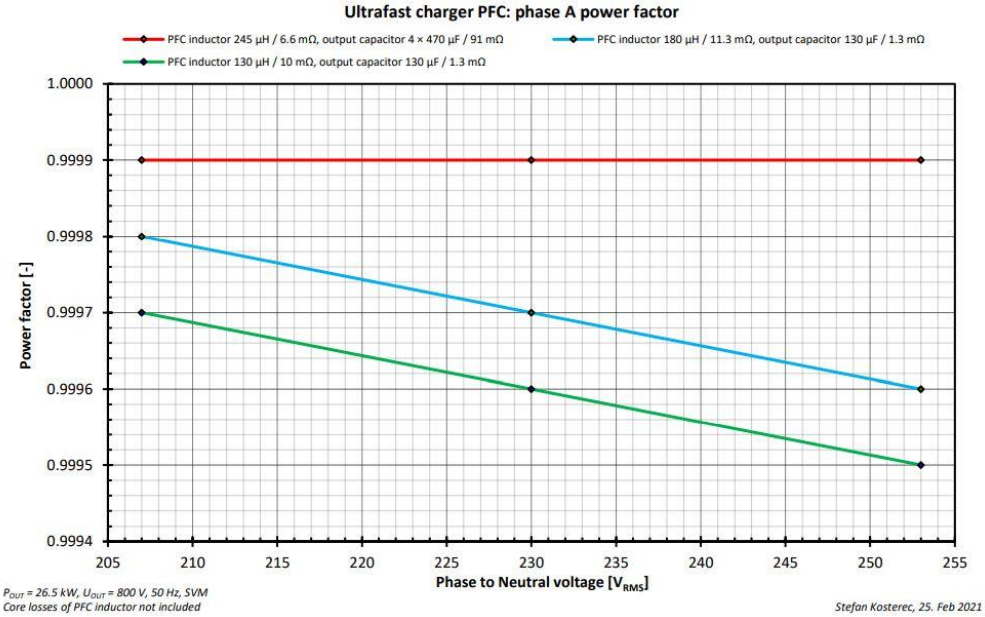


Fig. 15. Power factor as a function of input voltage and inductor and output capacitor values. All variants fulfill the requirement of PFC > 0.99.

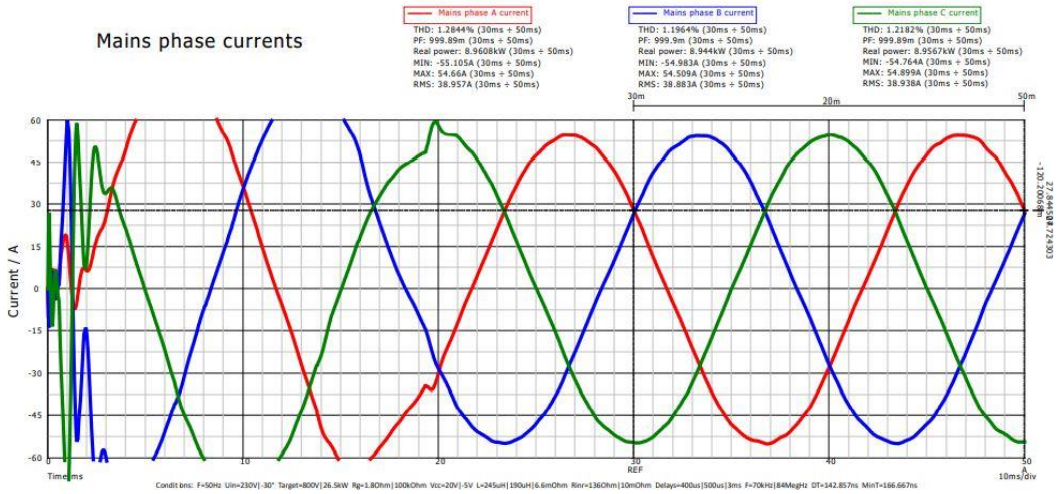


Fig. 16. Typical mains phase currents at ac input of PFC unit with a 245-µH inductor. PFC Phase A, C = 0.999. V_{IN} = 230 V.

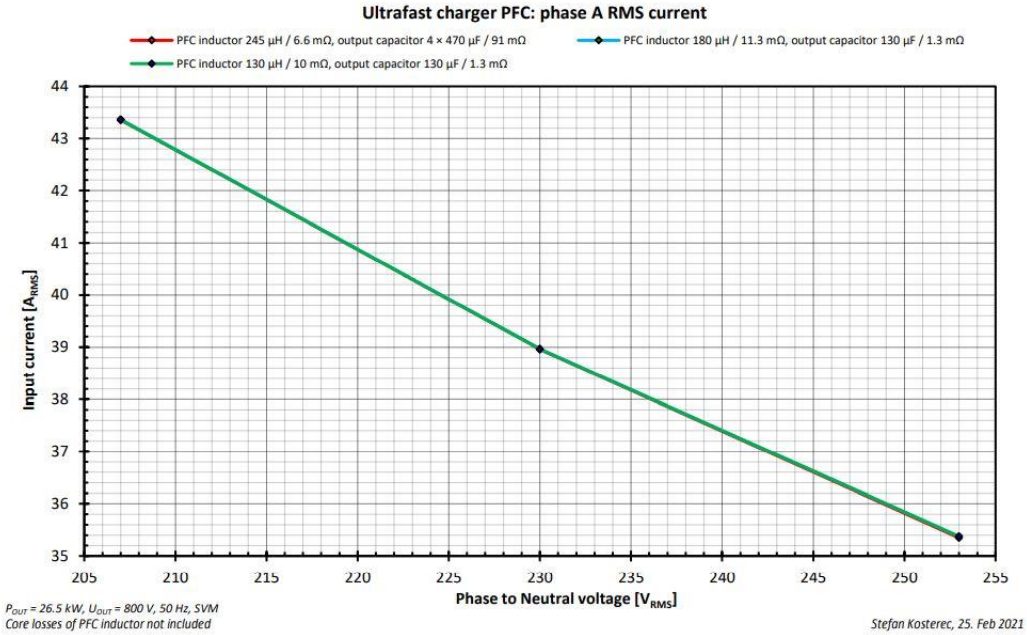


Fig. 17. RMS input current as a function of input voltage and inductor and output capacitor values.

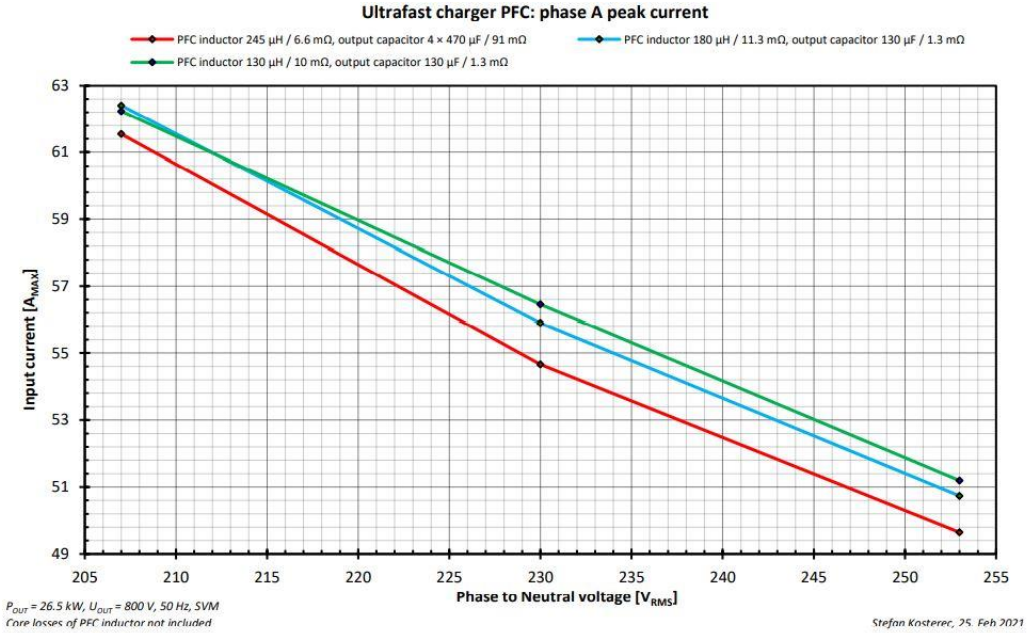


Fig. 18. Peak input current as a function of input voltage and inductor and output capacitor values.

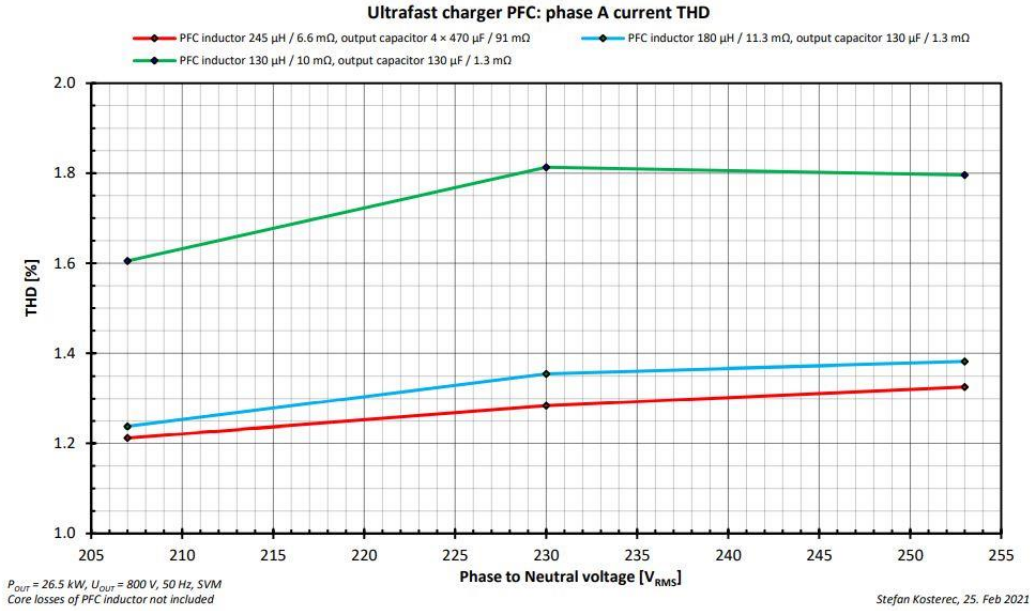


Fig. 19. Input current THD as a function of input voltage and inductor and output capacitor values.

PFC Inductor Operating Conditions

As advanced in Table 1, a good understanding of the inductor currents is critical to designing an effective and optimized PFC inductor. There are four critical current values that are used as inputs for the design or selection of an adequate inductor, and these current values can be obtained with the simulations:

- $I_{PHASE,RMS}$ for thermal considerations (Fig. 17)
- $I_{PHASE,PEAK}$ to account for the magnetic saturation level of the inductor core (Fig. 18)
- $I_{RIPPLE,PEAK-PEAK}$ to estimate the core losses (Core losses were not included in this simulation, but those losses can be considered separately.)
- $V_{PHASE,PEAK}$ (across the inductor) to define the insulation level of the winding.

Fig. 20 shows the peak-to-peak values of the ripple current in the inductor based on different $V_{PHASE-NEUTRAL}$ values. The 245-µH versions exhibit 40% less ripple than the 130-µH inductors. Another revealing detail of the simulation is how the actual $I_{RIPPLE,PEAK-PEAK}$ values reach their maximum and minimum values when the waveform crosses zero and at its peak, respectively. Figs. 21 and 22 depict these differences.

It can also be seen that the actual shape of the ripple waveform and frequency is different in both points. Such behaviors are common in SVM systems and not an issue. (Further discussion of this topic is beyond the scope of this installment but relates to the converter operation in CCM and DCM.)

In terms of inductor design, it will be important to consider the maximum peak-to-peak value of the current ripple. Another important factor in the inductor design, and isolation, is the determination of peak voltages that the inductor needs to withstand. Figs. 23 and 24 show these values as generated by the simulations.

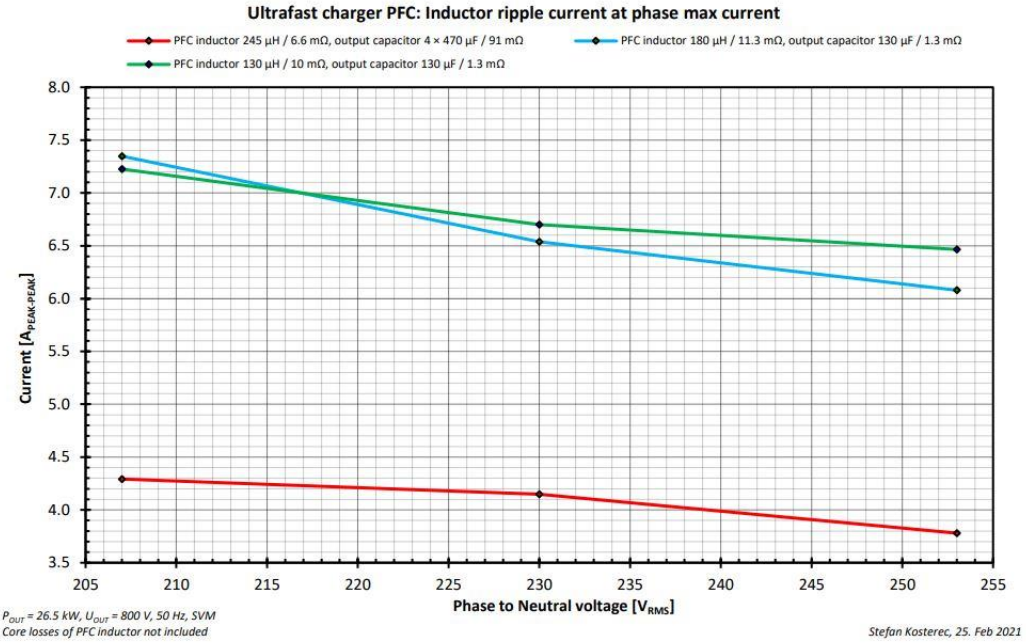


Fig. 20. Inductor ripple current as a function of input voltage and inductor and output capacitor values.

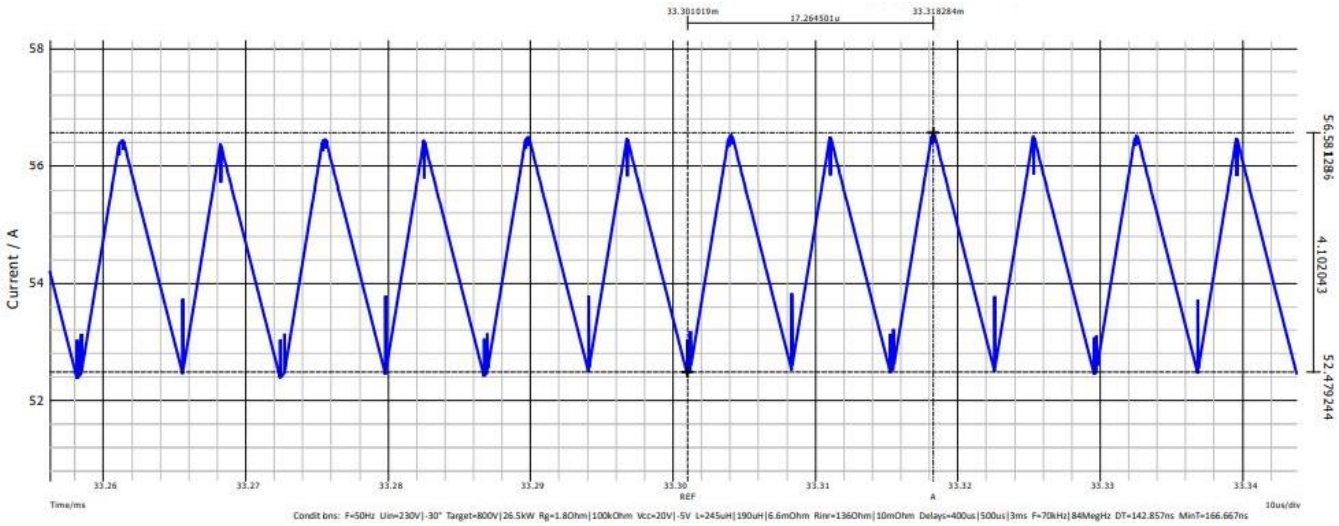


Fig. 21. Inductor current detail at the peak of the current sinusoidal waveform. Conditions: Phase B, V_{IN} = 230 V, P_{OUT} = 26.5 kW and L_{PFC} = 245 µH. Waveform values: $I_{PHASE,RMS}$ = 38.9 A and $I_{PHASE,PEAK-PEAK}$ = 4.1 A. X-Axes: 10 µs/div.

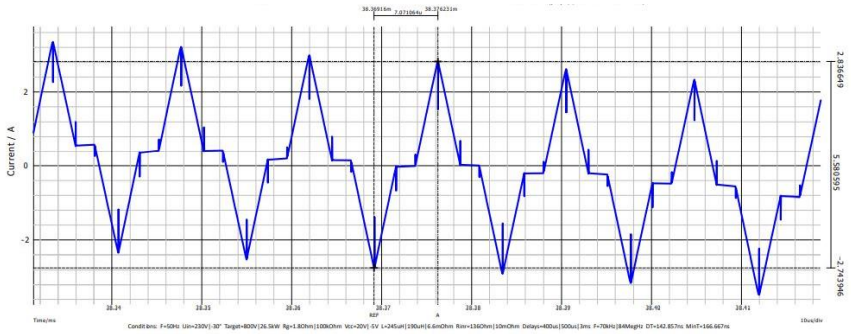


Fig. 22. Inductor current detail at the zero-crossing of the current sinusoidal waveform. Conditions: Phase B, V_{IN} = 230 V, P_{OUT} = 26.5 kW and L_{PFC} = 245 uH. Waveform values: $I_{PHASE,RMS}$ = 38.9 A and $I_{PHASE,PEAK-PEAK}$ = 5.58 A. X-Axes: 10 µs/div.

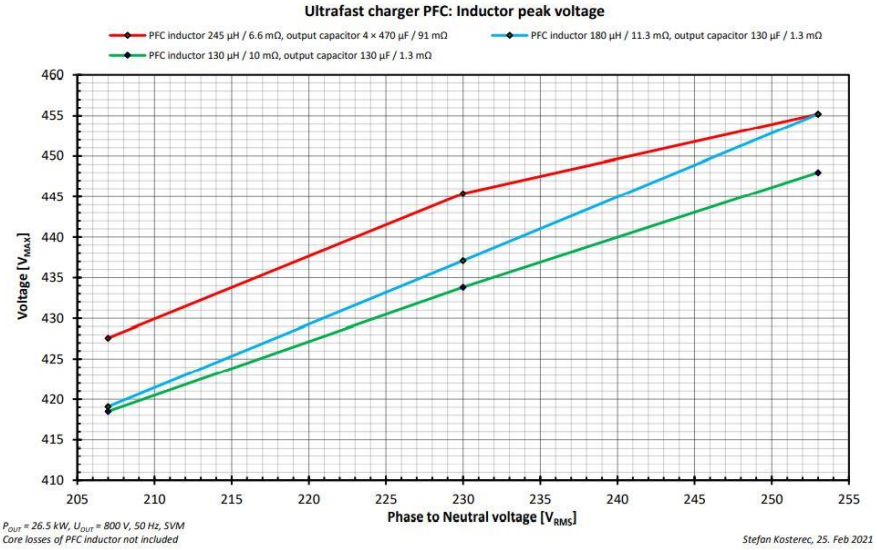


Fig. 23. Peak voltage across the inductor as a function of input voltage and inductor and output capacitor values.

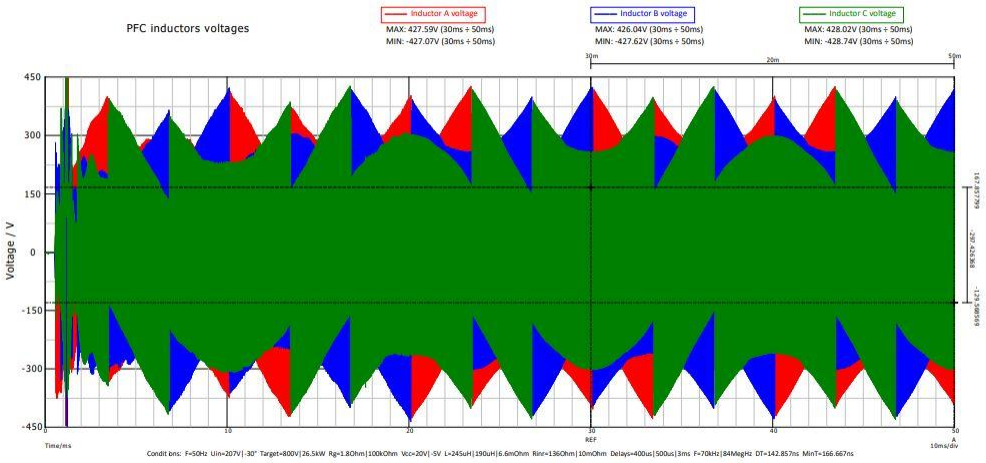


Fig. 24. Simulation of PFC inductor voltage envelope. This is a typical waveform for systems using space-vector modulation.

Voltages Between Mains And DC Output

In three-phase PFC systems and inverters, voltage differentials may arise between the phase line, neutral (N) or protective earth (PE) and the negative dc output (- VDC) of the converter, as there is no galvanic isolation (in the PFC stage) between front- and back-end of the system. It is very important to consider this possibility in the development stage and in the simulations.

Fig. 25 illustrates voltage envelopes between input line voltages and the -VDC of the converter, as well as the voltage between the N or PE lines and the dc negative output. Figs. 26 and 27 show that voltages in the range of - 300 V to + 1100 V arise. These voltage levels need to be considered, at least, during the inductor and PCB design. Such heavy voltage swings will partly influence the isolation requirements of the inductor and elements on the PCB. Moreover, these high voltages and dV/dt levels between N/PE and the –VDC can introduce noise of a different nature, especially if systems connected to the PFC output are vulnerable to common-mode noise.

Looking forward to the hardware testing and evaluation stage, the high voltages between N/PE and the (-VDC) might require extra care and additional safety measures. Again simulation played a vital role in revealing issues that must be addressed to achieve robust designs and also assist in the development process further down the road.

Interestingly, the envelopes of N and PE to dc output GND voltage get modulated by three times the grid frequency, while modulation depth is related to the saturation level of the PFC inductors (Fig. 25). These phenomena are influenced by the PWM modulation strategy applied, and in our case correspond to the envelopes seen in SVM-modulated systems.

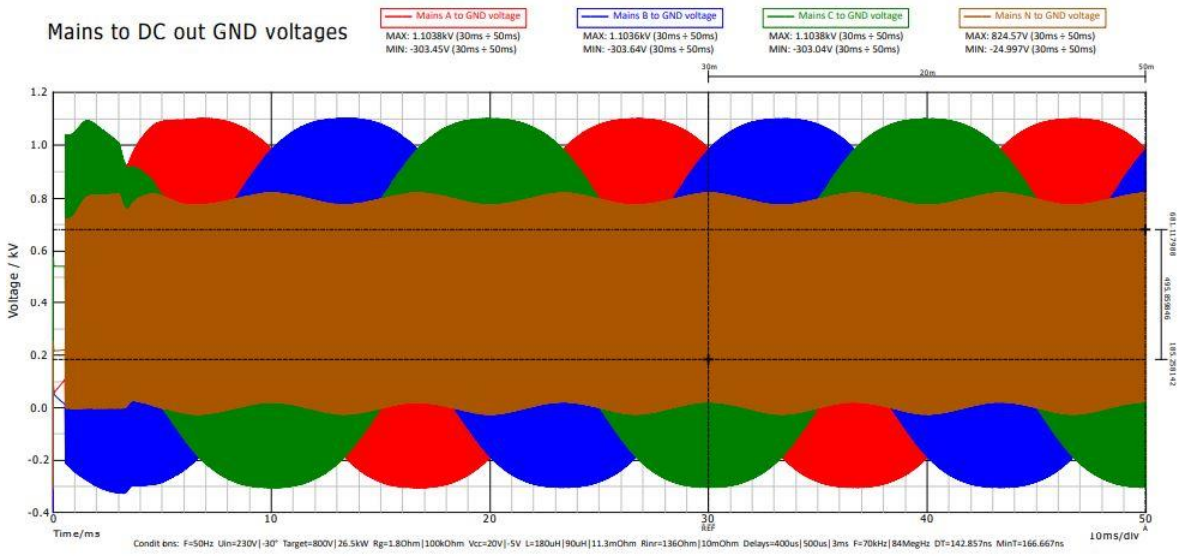
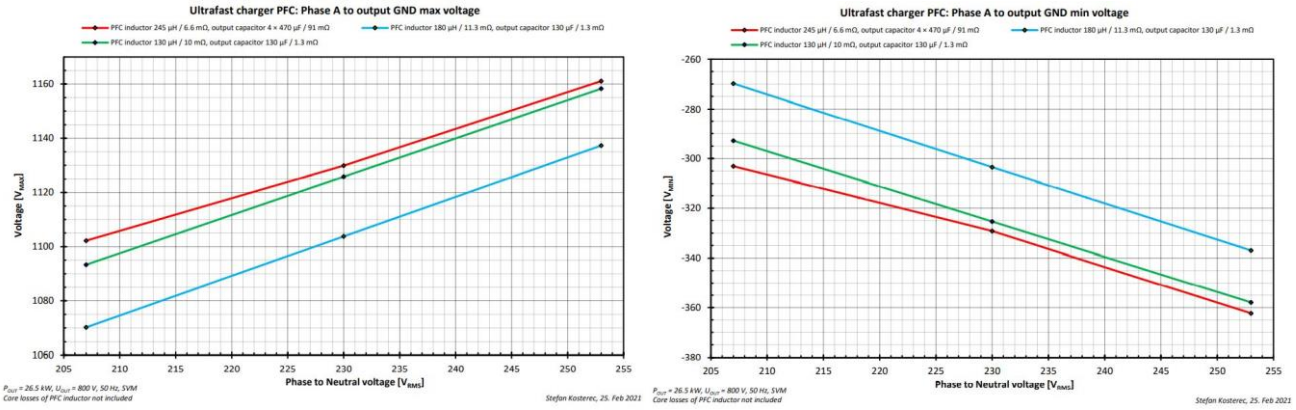
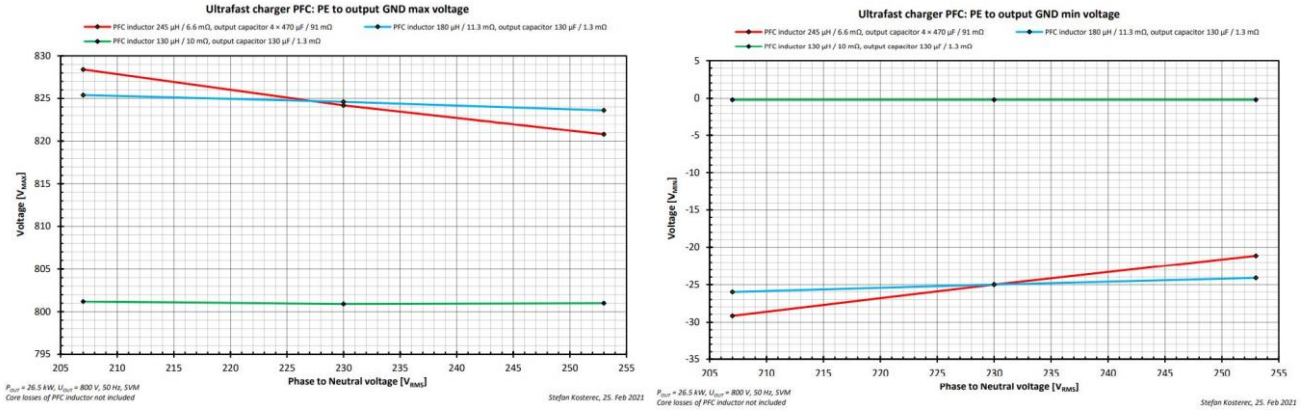


Fig. 25. Envelopes of typical mains phases and N/PE voltages to dc output GND line.



(a) *(b)*

Fig. 26. Maximum voltage differential (a) and minimum voltage differential (b) from phase A to negative dc output (- VDC) as a function of input voltage and inductor and output capacitor values.



(a) *(b)*

Fig. 27. Maximum voltage differential (a) and minimum voltage differential (b) from protective earth to negative dc output (- VDC) as a function of input voltage and inductor and output capacitor values.

PFC Output Capacitor

After the PFC function, the foremost role of the PFC system is to boost the dc-link voltage and hold it up at the reference level. The dc-link capacitor, placed at the output of the PFC, should support this function and effectively handle the current ripple generated when a load is connected to the output. Simulations help reveal how these two variables (dc-link voltage level and current ripple) will behave once the actual hardware is built.

Fig. 28 shows that the output current on the capacitor does not change drastically with either inductor or capacitor value. On the other hand, variations of ±10% on the input V_{PHASE} result in changes in the dc output capacitor ripple current of roughly ±15% (Fig. 29).

For the output voltage ripple ($V_{PEAK-PEAK}$), the value is not dependent on input V_{PHASE}, but mostly influenced by the dc output capacitance in combination with the parasitic equivalent series resistance (ESR). Fig. 30 shows the worst case of 4 x $V_{PEAK-PEAK}$, using four 470-µF capacitors in parallel.

Although the overall capacitance is higher in this configuration, the ESR of the electrolytic capacitor is also much higher (91 mΩ) in comparison with the alternative solutions featuring film capacitors (1.3 mΩ). In light of the small $V_{PEAK-PEAK}$, and considering that there are no stringent hold-up requirements for the capacitor, it was concluded that the output capacitance might be substantially reduced, which results in a significant reduction in capacitor size.

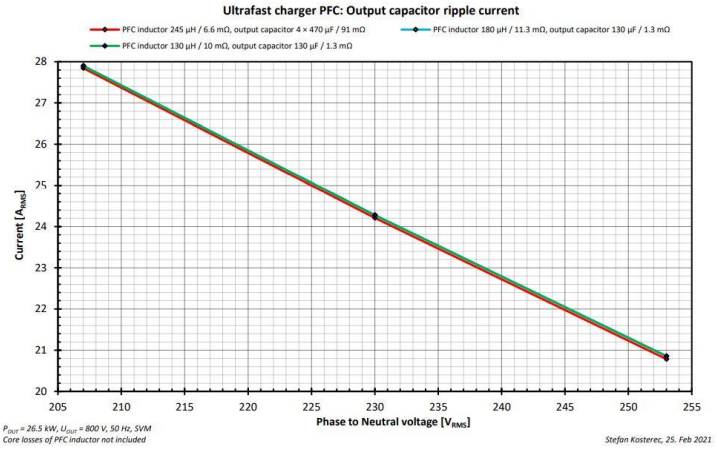


Fig. 28. Output capacitor $I_{CAPACITOR,RMS}$ as a function of input voltage and inductor and output capacitor values.

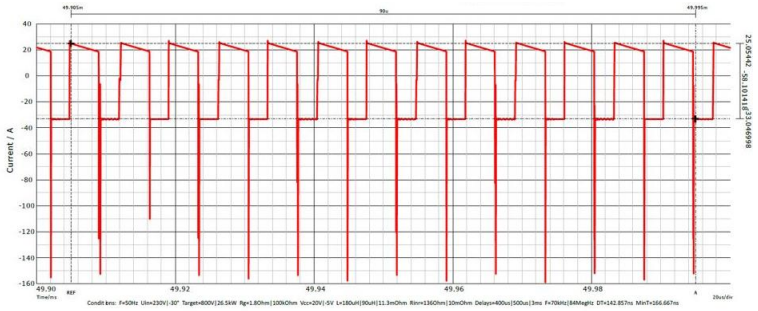


Fig. 29. Typical output capacitor current waveform. Conditions: V_{IN} = 230 V and P_{OUT} = 26.5 kW Results: $I_{CAPACITOR,PEAK-PEAK}$ = 58 A, $I_{CAPACITOR,PEAK}$ = 25 A and $I_{CAPACITOR,RMS}$ = 24.78 A. X-Axes: 20 µs/div.

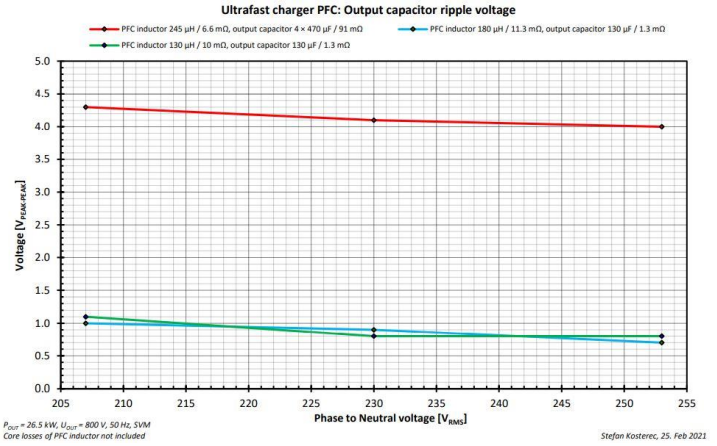


Fig. 30. Output capacitor ripple voltage as a function of input voltage and inductor and output capacitor values.

Switching Transitions: Turn-On And Turn-Off

One of the key parameters in evaluating the switching performance of the PFC stage is the speed of the switching transitions (Fig. 31), or in other words the dV/dt of the MOSFETs. In theory, the faster the switching transitions, the lower the exhibited losses and the better the efficiency. However there are other limitations on the switching speed. For example: the capability of the transistor itself to sustain such high gradients or EMI or other common-mode (CM) noise generated by fast transitions.

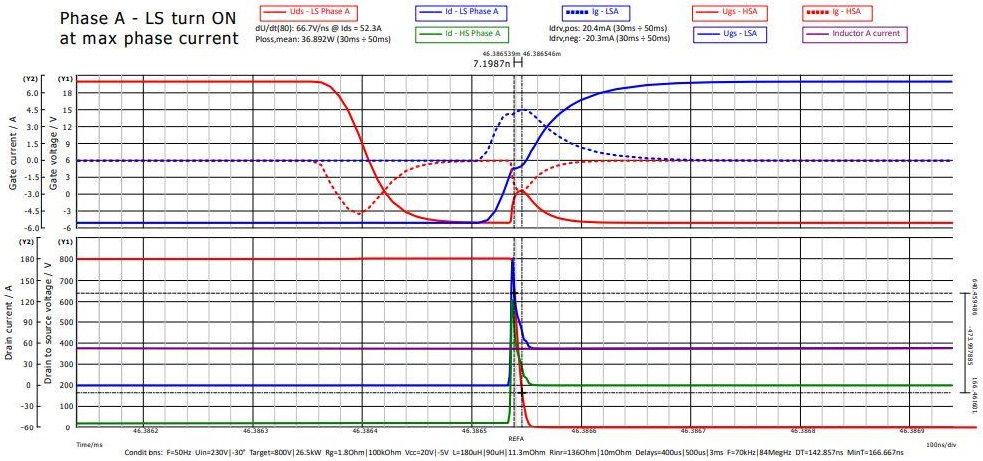


Fig. 31. Typical turn-on waveforms for the PFC stage MOSFETs.

Fig. 32 shows dV/dt values in excess of 66 V/ns with the configuration given for this simulation. Such values represent really fast transients indeed, only enabled by wide-bandgap technologies. Actually, such high dV/dt values could become harmful (even for SiC-modules) and high overvoltage spikes could be generated by the parasitic inductances in the actual application, easily surpassing the maximum V_{DS} rating of the component.

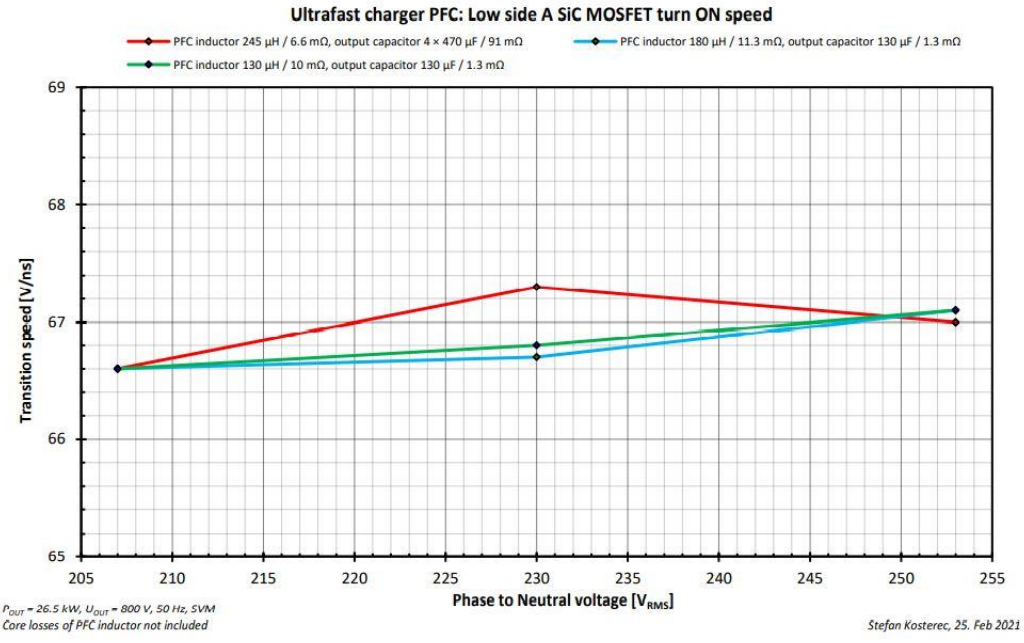


Fig. 32. Low-side phase A SiC MOSFET turn-on speed as a function of input voltage and inductor and output capacitor values.

Modifying the value of the gate source-resistor (for the turn-on) is the simplest way to reduce the dV/dt. A higher gate resistor value will result in slower transitions, and bring the application on the safer-side, with the tradeoff of a small additional power loss (as the transition will not be as fast). Based on the results of this simulation, it was decided to increase the original value of the gate source-resistor (1.8 Ω) by a factor of ~2.5 (to 4.7 Ω), in order to keep the turn-on transition around 25 V/ns, which serves as a good compromise. This will be the starting value used to evaluate the actual hardware.

Another element affecting the efficiency of the switching transitions is the turn-on current. Fig. 33 shows the values obtained for turn-on current in our simulation. In any case, the efficiency of the system has already been validated previously and major modifications to the turn-on are not foreseen at this point in time.

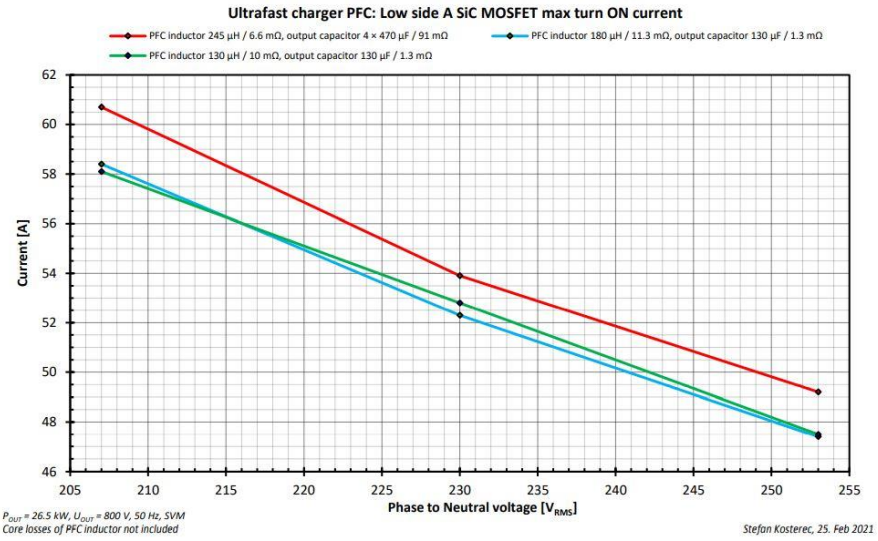


Fig. 33. Low-side phase A SiC MOSFET max turn-on current as a function of input voltage and inductor and output capacitor values.

Regarding the turn-off transitions a similar approach has been followed. Figs. 34, 35 and 36 show the results for these simulations. The off-transitions are also fast (up to 40 V/ns) with a 100-kΩ gate sink-resistor. The resistor value will be increased in the prototypes to tune the off-transition to around 25 V/ns.

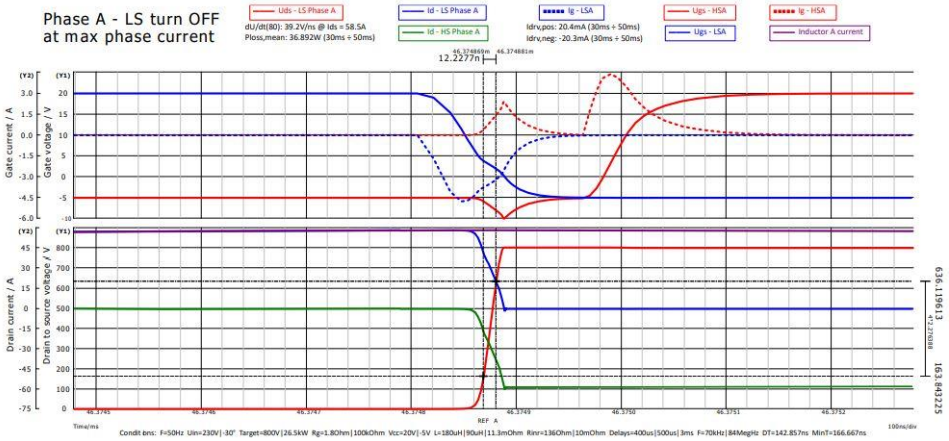


Fig. 34. Typical turn-off waveforms for the PFC stage MOSFETs.

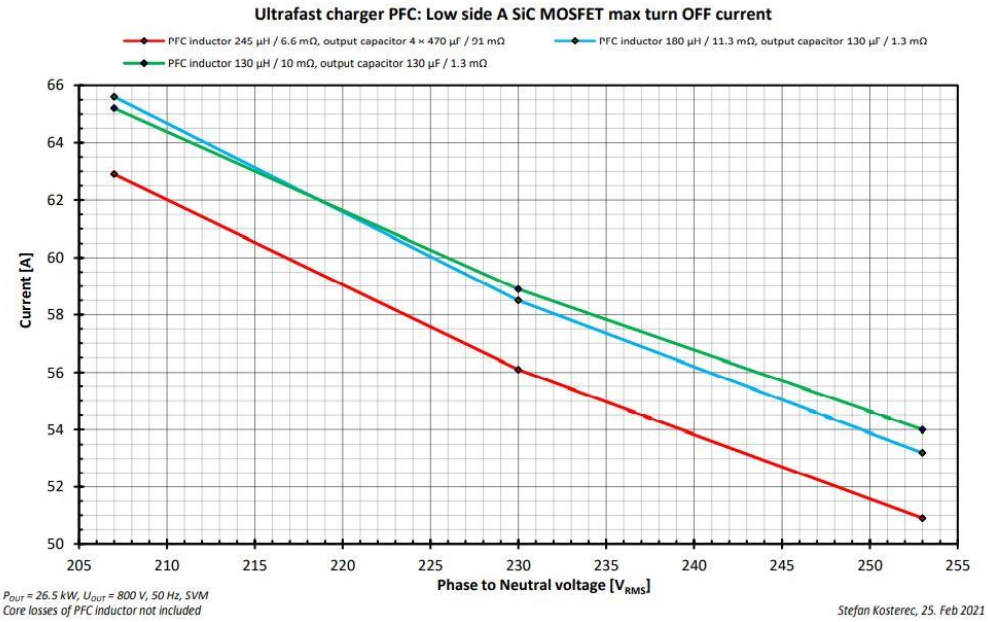


Fig. 35. Low-side phase A SiC MOSFET max turn-off current as a function of input voltage and inductor and output capacitor values.

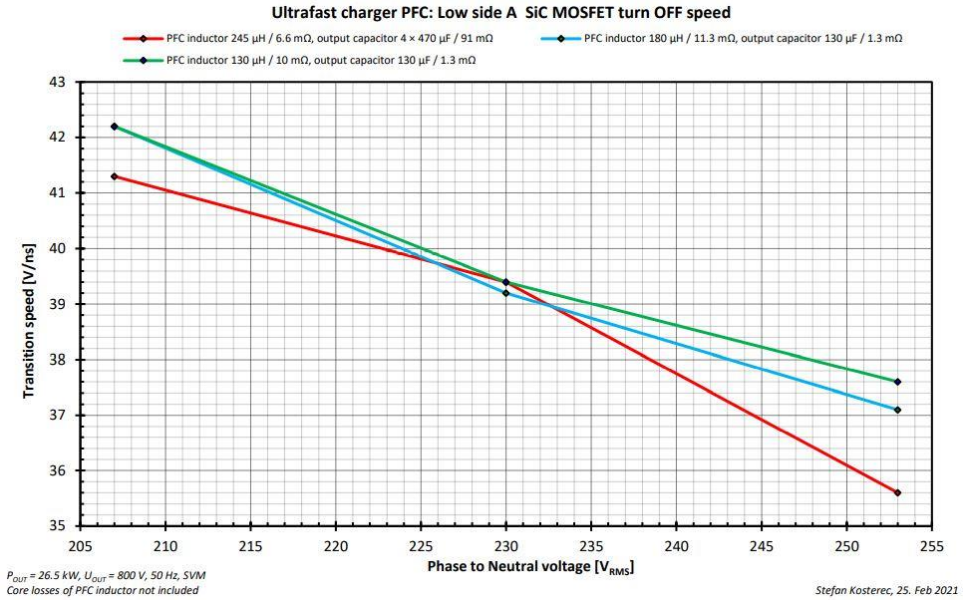


Fig. 36. Low-side phase A SiC MOSFET turn-off speed as a function of input voltage and inductor and output capacitor values.

Results And Conclusions

One of the ultimate goals of the simulations is to reduce the number of hardware iterations and accelerate the time-to-market of new products. Over the course of this article we have seen how important it is to have clear goals before the simulations and develop models that effectively help to achieve the goals. The results of the simulations will serve to answer our open questions, validate our assumptions or unveil necessary modifications for the system to work or to be optimized. Table 3 summarizes the outcomes of the simulations discussed above.

Table 3. Results of simulations of PFC stage.

Simulations	Results required	How they are used	Findings	Decisions made?
Functionality	V_{OUT}, I_{OUT} for all the specified operating points (for the specified V_{IN} range).	Verify that the PFC delivers specified voltage, current and power and fulfills the efficiency and all other requirements.	Requirements are fulfilled.	System is validated and design of the PFC (and passive components) can continue.
Efficiency and losses	• Efficiency • P_{LOSS} and distribution of losses across several components.	• Verify 98% peak target efficiency. • How P_{LOSS} and efficiency varies with different inductor values. • P_{LOSS} in each component and possible thermal management needs.	• Efficiency within range. • P_{LOSS} ≈ 330 to 430 W with 26 kW output and across the V_{IN} range. • $P_{LOSS,L,winding}$ small part. • Power switches account for ~70% of the system losses	Selected PFC choke with DCR maximum of 10 Ω.
Inrush current	• $I_{PHASE,MAX}$ • $R_{INRUSH,MAX}$ • P_{LOSS,R_INRUSH} • $I_{PHASE,PEAK}$	• Selection of capacitors. • $I_{PHASE,PEAK}$ below standard norms. • Verify start-up sequence.	• Max. repetition time of 4.19 seconds.	Proved functionality of designed circuit and selected values.
PFC functionality	PF value THD	• Verify above 0.99 target. • Verify THD.	• All inductor versions compliant. • $I_{PHASE,RMS}$ equal for all inductors. • THD all compliant (1.2% to 1.8%) but all compliant.	• Selected 180-µH inductor (to balance performance vs. form factor vs. DCR)
PFC (operating conditions)	$I_{PHASE,RMS}$	Thermal considerations	42.5 Arms	Complete. This is the spec. to pass on to the inductor manufacturer.
	$I_{PHASE,PEAK}$	Verify it remains below the magnetic saturation threshold of the core.		60 A
	$V_{MAINS-OUT}$ $V_{L,PEAK}$	Define and verify winding insulation of the inductor and other PCB elements.		2000-Vac inductor insulation. Set hi-pot test at 2 kV.
	$I_{PHASE,PEAK-PEAK}$	Estimation of P_{LOSS,L_CORE} (these losses are not simulated).	PFC inductor current shape changes quite a lot with actual mains phase.	10 A peak-peak

DC-link capacitor	• $I_{CAPACITOR,PEAK-PEAK}$ • $V_{CAPACITOR,PEAK-PEAK}$	• Validate capacitance value. • Verify $I_{OUT,PEAK-PEAK}$ in the system fulfills requirement.	• $I_{CAPACITOR,PEAK-PEAK}$ is 58 A (discharge-charge current). • Low ESR preferred.	Critical parameters are ESR and ripple current. Capacitor value might be reduced (for smaller system footprint).
T_{ON}/T_{OFF}	• dV/dt transition levels • $I_{PEAK,SPIKE}$ • $V_{PEAK,SPIKE}$ • Gate driver V-I transition waveforms	• Verify the elements are within acceptable range. • Modify gate-resistors' values if-not. • Estimate gate resistors' values for prototype.	• T_{ON} = 66 V/ns. • T_{OFF} = 40 V/ns (dV/dt).	• Turn-on R_g = 4.7 Ω. • Turn-off R_g = 3.3 Ω. • Expected results = ~20 V/ns.

References

1. "Developing A 25-kW SiC-Based Fast DC Charger (Part 1): The EV Application" by Oriol Filló, Karol Rendek, Stefan Kosterec, Daniel Pruna, Dionisis Voglitsis, Rachit Kumar and Ali Husain, How2Power Today, April 2021.
2. "Developing A 25-kW SiC-Based Fast DC Charger (Part 2): Solution Overview" by Oriol Filló, Karol Rendek, Stefan Kosterec, Daniel Pruna, Dionisis Voglitsis, Rachit Kumar and Ali Husain, How2Power Today, May 2021.
3. To learn more about physical models, see "Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results," ON Semiconductor publication TND6330/D, February 2021.

About The Authors

Oriol Filló serves as a solution marketing engineer for industrial applications at ON Semiconductor. He is responsible for the marketing strategy of industrial solutions, focusing on robotics and energy infrastructure. He has developed his career in the electronics industry with a focus on power and control, and gathered experience in industrial, IoT and automotive applications.

Prior to joining ON Semiconductor in 2019, Oriol worked at Industrial Shields and PRAX Inductive Components in technical sales and business development roles, where among others, he propelled growth of the export business. Oriol received an engineering degree in energy engineering and a M.Sc. in industrial automation systems and industrial electronics from Universitat Politècnica de Catalunya. Oriol also holds a master in management from EADA Business School.

Karol Rendek is an applications manager at the Systems Engineering Center at ON Semiconductor. Karol joined ON Semiconductor in 2020. Previously, he spent nine years working as hardware engineer, system engineer and project manager in development of embedded systems, Class D amplifiers, rolling stock control and safety systems and industrial electric vehicle chargers. Karol has Master's degree and Ph.D. in Microelectronics from Slovak University of Technology in Bratislava. He spent three years during his Ph.D. study focusing on low frequency noise analysis of GaN HEMT transistors.

Stefan Kosterec is an application engineer at the Systems Engineering Center ON Semiconductor. Stefan joined ON Semiconductor in 2013. Previously, he spent eight years at Siemens PSE as ASIC/FPGA designer where he developed digital solutions targeted for various areas, among others communications, power conversion and motor control. He spent also two years at Vacuumschmelze acting as inductive components designer and also took a role of product integrity engineer at Emerson Energy Systems responsible for verification of telecom power systems. Stefan has a master's degree in Applied informatics from the Faculty of Materials Science and Technology of Slovak Technical University Trnava.

Daniel Pruna is an applications section manager at the EMEA Systems Engineering Center at ON Semiconductor. Before joining On Semiconductor in 2019, he worked for nine years as development engineer and later as head of engineering for an OEM company in Germany. His work was mainly focused on battery chargers, switch-mode power supplies and motor controllers. Daniel holds an M.Sc. degree in Embedded Systems from Technical University of Chemnitz (Germany) and a B.Eng. from Lower Danube University of Galati (Romania).

Dionisis Voglitsis is an applications engineer at ON Semiconductor. He is responsible for the development and implementation of control algorithms and control schemes for motor control and charging applications. Before joining ON Semiconductor in 2019, Dionisis worked as a researcher for various European and national research projects, while he had also joined the Advanced Technology Center of Philips. Dionisis is the author and co-author of more than 30 research and technical papers in his field, published in high-quality journals (IEEE Transactions and Journals), which have been cited in more than 200 papers. He is also a guest editor for the "Energies" MDPI journal. He holds an engineering degree in energy engineering, an M.Sc. in wireless power transfer from TU Delft, The Netherlands, and a Ph.D. in electrical engineering from Democritus University of Thrace (DUTH), Greece.

Rachit Kumar is a senior applications engineer at the Systems Engineering Center at ON Semiconductor. Rachit joined ON Semiconductor in 2020. Rachit has been engaged for more than ten years on embedded software development focusing on motor control algorithms. Prior to joining ON Semiconductor, Rachit worked at Nanotec Electronics doing embedded systems development for low power BLDC and stepper motor controllers. Rachit has a master's degree in mechatronics from the University of Applied Sciences, Ravensburg-Weingarten, Germany.

Ali Husain is senior manager for Strategy and Corporate Marketing, focusing on power electronics. He has previously worked in Technical Marketing at Fairchild Semiconductor and International Rectifier in various roles for nine years. Ali has a bachelor of electrical engineering and a bachelor of economics from the University of Pennsylvania and a Ph.D. in electrical engineering from the California Institute of Technology.

For further reading on designing EV chargers, see the How2Power Design Guide, locate the Application category and select "Automotive".