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Bidirectional Switches Permit ZVS Operation In Single-Ended Forward Converters

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The single-ended forward converter has several significant advantages over the widely used converters operating in push-pull modes, such as bridge and half-bridge. First, it provides simplicity, as it can be realized with just one switch on the primary side. Secondly, this topology's reliability is higher, because there are no paths for cross-conduction and associated shoot-through conditions that could cause active component damage.

Another advantage is its immunity to transformer saturation, which is associated with the flux imbalance caused by a momentary difference in control pulse duration, or pulse skipping. Finally, a reduction in input and output capacitor RMS currents, which is inherent to push-pull operation, can also be achieved with forward converters by interleaving the converter stages.

Despite all these benefits forward converters lose the power density competition to push-pull converters because they are larger as a result of their hard-switching operation. Hard switching in the forward converter topology effectively becomes a showstopper for increasing the switching frequency and operating frequency of the magnetic components, which limits the usage of forward topologies to low-power applications up to a few hundred watts.

Meanwhile, implementation of soft switching in the forward converter is problematic. In the conventional approach, it requires using additional active components on the primary side for creating resonant switching transitions, which results in increased complexity, size, and design costs, and essentially brings back some of the previously mentioned shortcomings of push-pull operation. For all these reasons, push-pull-mode bridge and half-bridge topologies with zero voltage switching (ZVS) have become and remain the leading converter choices in the PSU power density race.

However, recent developments in high-voltage-rated SiC MOSFET and bidirectional GaN switch technologies[1-3] have created new opportunities for forward converter design. These components can simplify the implementation of ZVS mode operation in the forward topology and make it highly competitive in the power range above 1 kW. This article studies opportunities to employ such devices in the forward converter topology and discusses the benefits that such applications can provide.

This discussion begins with a review of how the single-ended forward converter operates in hard-switched mode, and why adding a resonant capacitor (in place of the reset winding) on the primary side fails to achieve ZVS. The addition of a buffer inductor on the secondary side, offers a simple means to obtain ZVS operation, but requires adoption of a variable switching frequency.

This limitation can be overcome with use of a bidirectional switch in place of the secondary-side rectifier diode and the buffer inductor, which is the basis for the ZVS single-ended forward converter topology proposed here. The operation of this converter, with back-to-back MOSFETs used as the bidirectional switch, is explained and equations for key operating parameters are given. Configurations of the ZVS single-ended forward converter that provide multiple outputs and synchronous rectification are also described.

The Obstacle To ZVS In Forward Converters

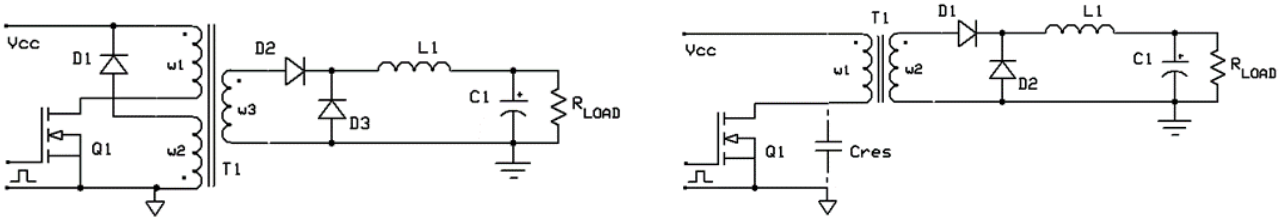
Zero voltage switching can be defined as the transition of a converter's active components into their on-states after voltages across them have already reached the zero level. The advantage of this operating mode is an opportunity to increase the switching frequency due to the significantly reduced switching losses associated with non-zero turn-on transition times and dissipating the energy stored in the parasitic capacitance at each switching cycle. Let's examine what prevents enabling such switching in the conventional forward converter operating in its most energy-efficient continuous-conduction mode.

A basic schematic diagram of this converter is shown in Fig. 1a. A typical switching waveform for the MOSFET Q1 is shown in Fig. 1c by the yellow trace. Once Q1 is on, freewheeling diode D3 gets reverse biased by positive voltage, generated at the dot end of secondary winding w3. Rectifying diode D2 is forward-biased and provides the energy flow from the primary side to the load.

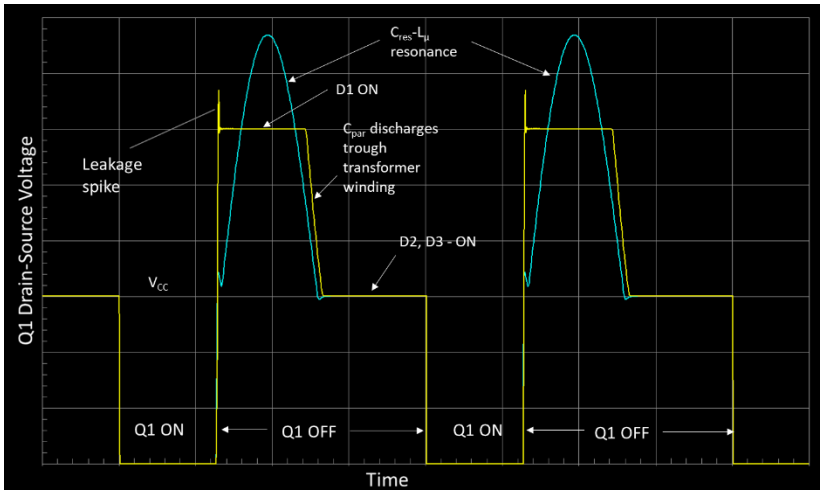
After Q1 turns off, the voltages across transformer T1's windings change polarity, filter inductor L1's current starts to flow through freewheeling diode D3, and the circuit lumped parasitic capacitance (which can be considered connected in parallel with the switch) starts charging by the magnetizing current of T1's primary winding.

Once the voltage across Q1 reaches the $V_{cc} + V_{cc} \cdot w_2/w_1$ value, the voltage across Q1 gets clamped at this level. The spike exceeding the clamp voltage level is caused by the leakage inductance between the T1 windings. Once the energy stored in T1's magnetic field gets recuperated into the primary source through clamping diode D1, the parasitic capacitance starts discharging through transformer winding w1.

When the voltages across the transformer windings cross zero, D2 becomes forward-biased, and winding w3 gets "shorted," i.e. shunted by the two conducting diodes (D2 and D3). The voltages across the T1 windings during this time interval remain at the zero level, and the voltage across Q1 gets held at the V_{cc} level forming a plateau until the next control pulse turns the MOSFET on (Fig. 1c).



(a) Basic forward topology. *(b) Forward topology with added resonant capacitor.*



(c) Comparison of voltages across the switch in the basic topology (yellow) and the topology with a resonant capacitor (blue).

Fig. 1. Forward converter schematics and timing diagrams.

With larger duty ratios and the same voltage clamp level, the transformer reset process may last longer without forming the V_{cc} plateau and there will not be enough time for C_{par} to discharge to this voltage level.

If for the sake of experiment, we eliminate the reset winding and add a resonant capacitor C_{res} (C_{res} >> C_{par}) in parallel with Q1 (Fig. 1b) to use more energy for the resonance and to keep the transformer reset more deterministic, the voltage waveform will change, indicating that leakage energy is absorbed and showing a C_{res}-L_μ resonance (where L_μ is the transformer magnetizing inductance). This process is shown by the blue trace in Fig. 1c.

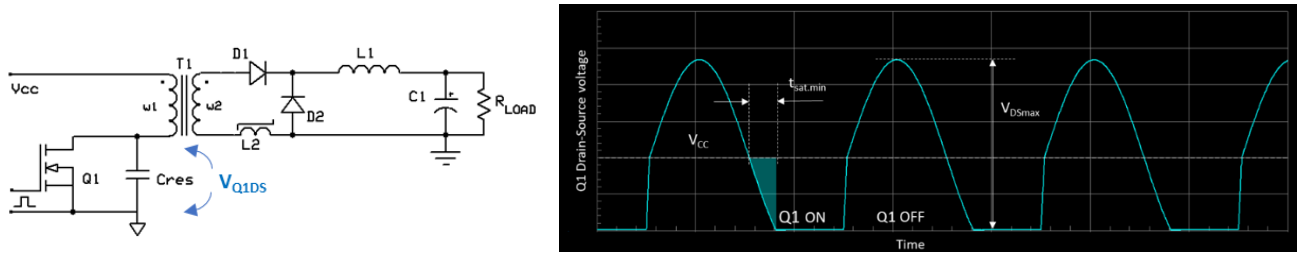
As can be seen from this waveform, as with the basic topology, the voltage across Q1 in this case also gets held at the V_{cc} plateau and the next Q1 turn-on will occur at this voltage level, which makes ZVS operation impossible just as it is with the basic topology in Fig. 1a. To drop the voltage across the switch below V_{cc} the magnetizing current (referred to the secondary side) needs to exceed the L1 current flowing through D3, which would make converter operation very inefficient.

As stated above, adding an active and passive component network on the primary side could force the voltage to drop, but this would make the converter's complexity and operating mode comparable with push-pull topologies. This makes it necessary to consider a more robust and cost-effective means of enabling ZVS operation.

Buffer Components on The Secondary Side

As follows from the above considerations, the voltage across the primary switch Q1 gets held at the plateau level prior to the switch transition into the on-state because the secondary transformer winding is shunted by two conducting components. To eliminate this shunting effect, a "buffer" element, which represents a large impedance for the magnetizing current, can be placed in series with the secondary winding.

The simplest way to realize such a buffer element is to use a saturating inductor. This could delay the current flow through D1 by the time interval required to saturate the inductor and for V_{Q1DS} to reach the zero level. The converter topology implementing this concept is shown in Fig. 2a with the switching waveform illustrating its operation in Fig. 2b.



(a) *(b)*

Fig. 2. The forward ZVS converter with saturating inductor (a) and its switching waveform (b).

Note, that in order to have enough energy to bring the voltage across the switch to the zero level, the magnitude of T1's primary winding voltage needs to be no less than V_{cc} and the peak Q1 drain-source voltage must exceed the $2V_{cc}$ level.

The saturating choke inductance L_2 needs to be much larger than the T1 magnetizing inductance L_μ as referred to the secondary side. The minimum saturating volt-seconds value required to provide ZVS is shown as a shaded area in Fig. 2b, hence the minimum saturation time of the added inductor needs to be equal or larger than the minimum time interval $t_{sat.min}$ required for the drain-source voltage to reach the zero level (Fig. 2b):

$$t_{sat} \geq t_{sat.min} = \sqrt{L_\mu C_{res}}\,\sin^{-1}\frac{V_{cc}}{(V_{DS.max} - V_{cc})}$$

The saturating inductor can be implemented using a core material with a nearly rectangular-shaped B-H curve providing larger permeability in its nonsaturated state. Its physical parameters can be determined based on the

expression for the relationship between the volt-second area applied to the winding, selected core dimensions, and saturation flux density of the core material. From this expression:

$$w_{L2} \cdot A \geq \frac{V_{cc} w_2 t_{sat.min} \left(\widehat{V_{DSmax}} - \sqrt{\left(\widehat{V_{DSmax}} - 1\right)^2 - 1} \right)}{w_1 B_{sat} \sin^{-1}\left[1/\left(\widehat{V_{DSmax}} - 1\right)\right]}$$

where $\widehat{V_{DSmax}}$ is the peak drain-source voltage normalized over V_{cc}, w_{L2} is the number of turns in the winding, A is the core cross-sectional area and B_{sat} is the saturation flux density of the core material.

Assuming that realistically $\widehat{V_{DSmax}} = (V_{DS.max}/V_{cc})$ always has a minimum value in the 2.1 to 2.2 range, this equation can be simplified and with sufficient accuracy such that the product of the L2 winding's number of turns and its core cross-sectional area can be determined as:

$$w_{L2} \cdot A \geq \frac{V_{cc} w_2 t_{sat.min}}{2 w_1 B_{sat}}$$

Other equations for calculating basic parameters of this converter are given in reference 4.

The main advantage of the converter in Fig. 2a is that it can provide ZVS operation in the single-ended forward topology by a very simple means—using just one passive component. The magnetizing and leakage energies in this converter are applied to capacitor C1 and then flow back into the primary source without the need for additional windings or active components on the primary side. Its performance could be further improved by using standard synchronous rectification on the secondary side. The shortcoming of this implementation is that to maintain regulation of the output voltage, it needs a constant off-time control which results in a varying switching frequency.

It is important to note that using a cap in parallel with the primary-side MOSFET makes the resonance process insensitive to variations in component parasitic capacitance. Besides providing ZVS, this cap also absorbs the leakage voltage spike and decreases the drain voltage rise rate:

$$dV_{DS}/dt = (I_{L1} w_2/w_1 + I_{\mu})/(C_1 + C_{par})$$

where I_{L1} and I_{μ} are filter inductor and transformer current magnitudes, respectively. This reduces power loss during the turn-off process. The drain voltage rise could be slowed down further if the inductor current flow through secondary winding w2 is interrupted prior to the Q1 turn-off time, which would make the first component in the numerator parenthesis of the above equation equal zero.

On the other hand, in order to realize a PWM output voltage control, the pulse duty ratio at the output filter input needs to be controlled at a fixed switching frequency. In this topology such an operating mode can be provided by controlling the D1 current flow time duration, while Q1 on- and off-time intervals remain fixed. It is easy to see that both these functions could be potentially enabled with the same active secondary-side current flow blocking component.

Such action cannot be completed with just replacing D1 in Fig. 2a with a standard synchronous rectifier because of the body diode intrinsic to the device's structure, which creates a path for current flow when the switch is off. This means that such control needs to be realized with a different type of switch, capable of blocking both positive and negative voltages.

Active Blocking Component on The Secondary Side—Two Operating Modes

As it was stated above, if a "delaying" current flow component (inductor L2 in Fig. 2a) can be replaced with a switch, capable of blocking both voltage polarities, such a switch would be able to interrupt the filter inductor current flow through secondary winding w2 at any time when voltage at w2 dot end goes positive. In other words, both ZVS and PWM control can be realized by replacing L2 and D1 components in Fig. 2a with a

bidirectional switch (BDSw) arrangement, which could either be created by connecting two MOSFETs back-to-back or implemented by a single-package component.

The proposed ZVS implementation method utilizing a bidirectional switch is illustrated in Fig. 3a. This converter can have two operating (control) modes:

1. Primary-side switch Q1's on-time is shorter than secondary-side switch Q2's on-time.

2. The primary switch's on-time is equal to or exceeds the secondary-side switch's on-time.

The converter's main component voltage waveforms for these two control options are shown in Fig. 3, parts b and c, respectively.

Output voltage regulation at constant switching frequency (PWM control) can be achieved in both of these modes. In the case of the first control mode, the primary switch Q1's voltage waveform shown in Fig. 3b for the proposed ZVS circuit is similar to the switch-voltage waveform for the saturating inductor case shown in Fig. 2b: it has a relatively fast primary-side MOSFET voltage rise in the 0 to V_{cc} region. What's different from the saturating inductor case is that at Q1 on-time durations shorter than the BDSw conduction time, the switch-voltage waveform has a plateau at the V_{cc} level associated with a magnetizing current circulating through two conducting secondary components.

Fig. 3c waveforms represent a more efficient operating mode with no voltage plateau, which is achieved using the second control mode. As can be seen from the comparison of the waveforms in Fig. 2b and Fig. 3c, besides realizing the PWM with a BDSw on the secondary side, interrupting the secondary current flow prior to Q1 turn-off time eliminates the losses associated with ineffective magnetizing current circulation, slows down the Q1 drain voltage rise in the 0 to V_{cc} region, and provides additional reduction in Q1 turn-off switching loss. Such benefits make this second operating mode the optimal choice for the ZVS implementation.

Basic ZVS converter parameters can be derived based on the balance of the volt-seconds of each voltage polarity applied to the primary transformer winding w1 over one complete switching cycle. They are shown as shaded areas in Fig. 3c. From this balance equation, the resonance frequency ω_{res} can be defined as follows:

$$\omega_{res} = \frac{1}{\sqrt{L_\mu C_1}} = F_{SW}\left[\pi + 2\sin^{-1}\left(\frac{1}{\widehat{V_{DSmax}} - 1}\right) + 2\sqrt{(\widehat{V_{DSmax}} - 1)^2 - 1}\right]$$

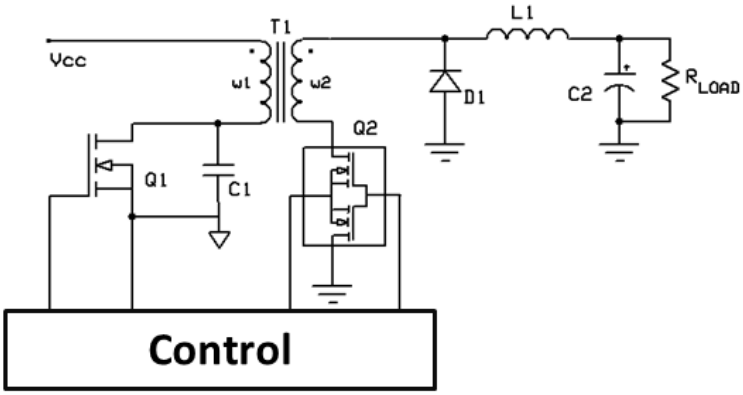
where F_{SW} is the switching frequency.

The maximum primary switch-on time duration $T_{p.max}$, at which $\widehat{V_{DSmax}}$ level will be achieved is

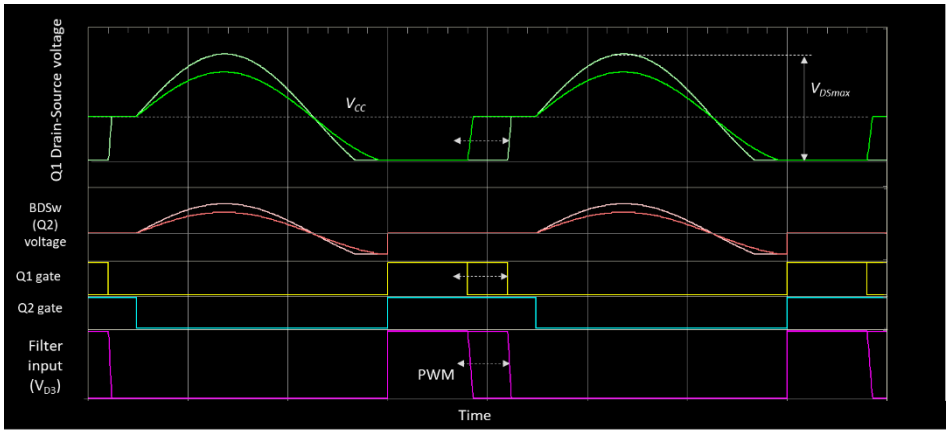
$$T_{p.max} = {2\sqrt{(\widehat{V_{DSmax}} - 1)^2 - 1}}\Big/{\omega_{res}}$$

As in the conventional forward topology, the ZVS forward converter generates a square wave at the input to the LC filter (V_{D3} in Fig. 3c), so the required power transformer turns ratio can be determined with methods similar to those used for standard hard-switching regulators. The only difference is that the pulse duty ratio used in the equations needs to represent a relative duration of the BDSw conduction state.

The bidirectional switch needs to be capable of withstanding the voltage level $V_{Q2+} = (V_{DS.max} - V_{CCmin})w_2/w_1$ of positive polarity and $V_{Q2-} = V_{CC.max}w_2/w_1$ of negative polarity. All other circuit parameters can be obtained using standard practices well developed for conventional forward converters.[5]



(a)



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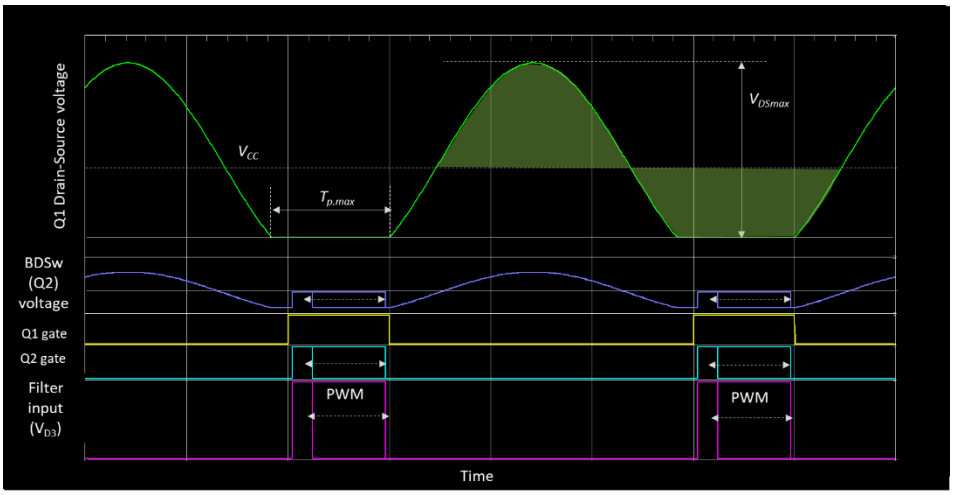


(c)

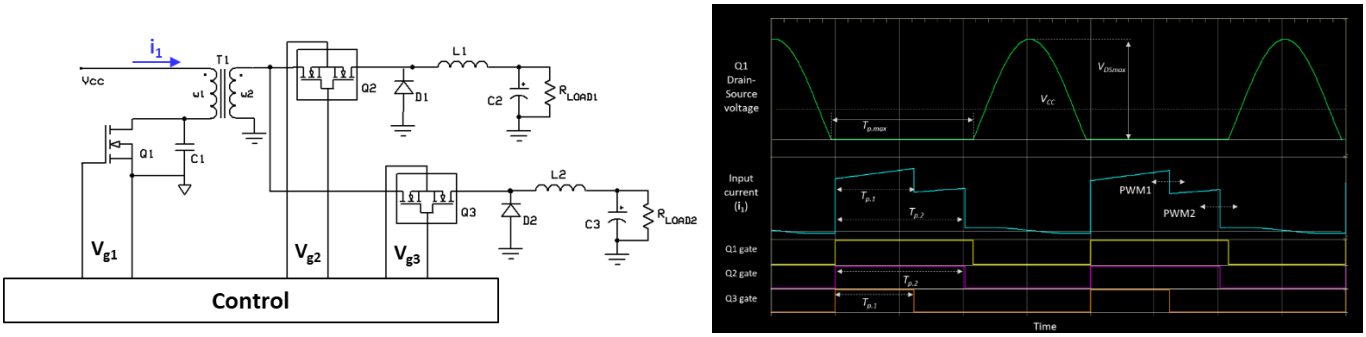
Fig. 3. A forward ZVS converter with bidirectional switch providing PWM control (a). Its component waveforms are shown in two control modes: where the primary-side switch Q1 on-time is shorter than the secondary-side switch Q2 on-time (b) and where the primary switch on-time is equal to or exceeds the secondary-side switch on-time (c).

Practical Applications Of This ZVS Converter

Multi-Output Arrangement

The proposed topology can be used for a single-output voltage regulator, but it can also be easily configured for multi-output applications. Placing BDSw in the secondary high-side current path (between the dot end of w2 and D2 cathode in Fig. 3a) enables usage of the secondary switch as a post-regulator component and forming additional regulated PSU outputs referenced to the same ground plane and using the same secondary winding.

This option is illustrated by a two-output arrangement in Fig. 4a. To get regulated voltages on each output, each channel needs to have a separate PWM controller. Currents from each of the loads will be summed in each of the transformer windings and constitute the resultant primary current waveform shown with the blue trace in Fig. 4b.



(a) (b)

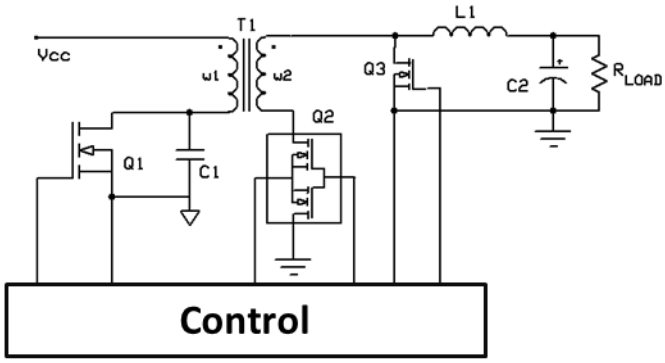
Fig. 4. A multi-output forward ZVS converter with bidirectional switch in the secondary, high-side current path (a) and its components' waveforms (b).

Synchronous Rectification Arrangement

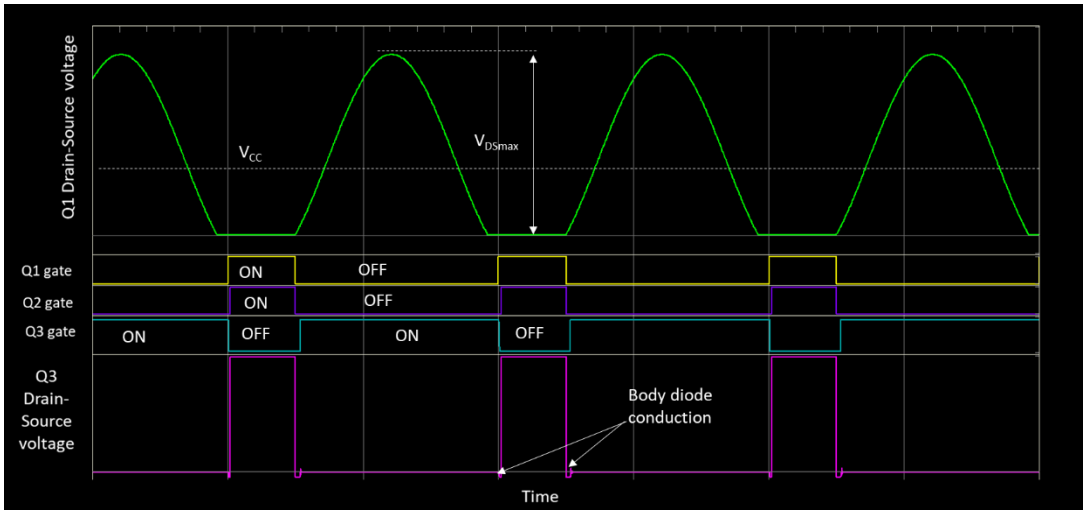
As would true for the hard-switching topology, replacing the freewheeling diode with an actively controlled switching element can help to further reduce power losses and to provide higher efficiency. To prevent cross-conduction between the two active components on the secondary side, the usual dead/blank time requirements need to be applied. As with synchronous buck converter implementations, the dead time value in this application must be just long enough to prevent "shoot through" on the secondary side—going beyond this value incurs additional deadtime losses.

A forward ZVS converter with a bidirectional switch and a freewheeling synchronous rectifier is shown in Fig. 5a. Its component waveforms and control signals are given in Fig. 5b for reference.

The performed analysis and presented implementation options were given for a single-switch forward converter but the same principle can be applied to the two-transistor (double-ended) forward topology, which could be used if a reduction is needed in the peak voltage of the primary switch.



(a)



(b)

Fig. 5. A forward PWM ZVS with freewheeling sync rectifier (a) and its component voltage waveforms (b).

Conclusions

The proposed technique provides a substantial reduction of power loss by essentially eliminating the switching losses in the primary-side switch. It simplifies power transformer design and makes the converter virtually immune to cross-conduction phenomena and the leakage inductance voltage spikes.

These advantages of the ZVS forward topology provide an opportunity for a significant increase in both the switching frequency and power density of the converter without impacting its efficiency. Using conventional pulse-width modulation in combination with only one primary-side MOSFET power switch provides a simple and cost-effective conversion solution for high-power applications of 1 kW and above.

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About The Author

Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

For more on forward converter design, see How2Power's Design Guide, locate the "Topology" category and select "Forward".