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Integrated GaN Power Stages Enable High-Performance 48-V To 12-V Power Converters

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GaN devices are finding use in an increasing number of applications. Examples are 48-V to 12-V power converters as well as Class D amplifiers. To address these applications, uPI is introducing a family of integrated GaN power stages that combine two 100-V GaN FETs in a half-bridge configuration with a dual-channel driver and protection features. These devices simplify the development of GaN-based designs by eliminating the difficulties associated with driving enhancement-mode GaN FETs, making it easier to obtain the higher efficiency or smaller size enabled by fast-switching GaN devices.

In this article, the application of a uPI GaN power stage is demonstrated in a 48-V to 12-V, 180-W synchronous buck converter. This design example showcases the efficiency, thermal and switching performance made possible by the GaN device, while discussing elements of the design, like cooling and inductor choice, that affect converter performance. A low-cost technique for measuring the GaN device's fast switching transitions is also described.

The nonisolated synchronous buck converter was chosen for the design example because it represents the simplest implementation of a 48-V to 12-V converter. However, the GaN power stages discussed in this article can also be applied in other topologies suitable for this voltage conversion, and these include both nonisolated and isolated topologies providing either unidirectional or bidirectional power conversion.

Power Stage Devices With Different Control Options

As noted above, uPI's GaN power stages combine two 100-V GaN FETs in a half-bridge configuration with a dual-channel driver. One driver channel is for the high-side GaN FET, while the other is for the low side, powered by a single 5-V rail. This power stage family comes in two different versions, the uP9801 with dual control inputs (Fig. 1) and the uP9802 with a single control input (Fig. 2). These devices are part of the uPI uGaN family.

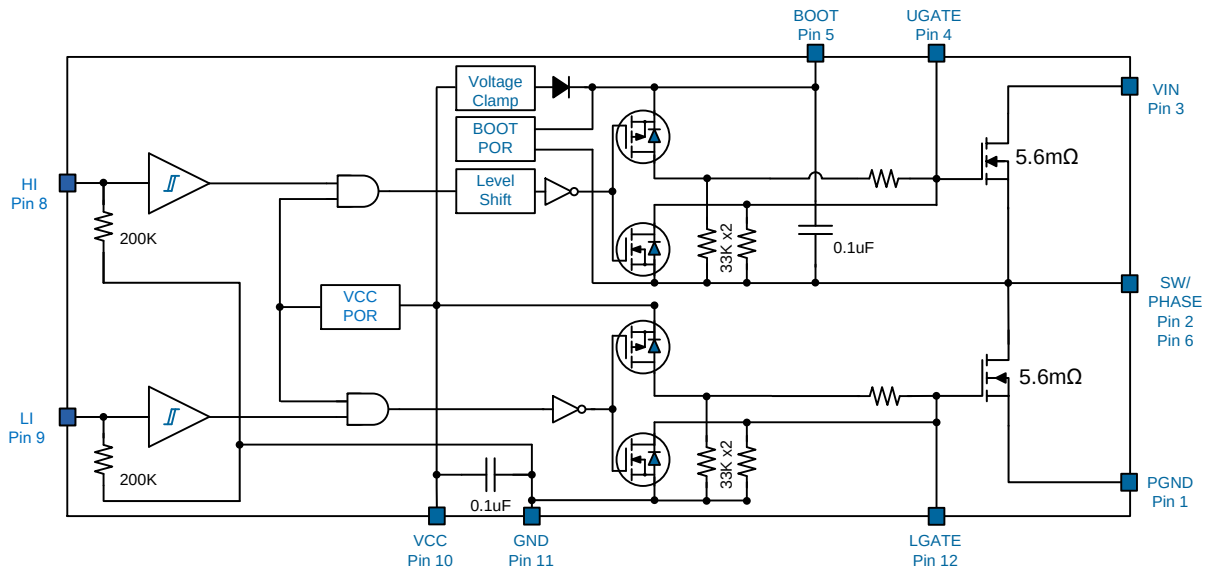

Fig. 1. uP9801Q block diagram.

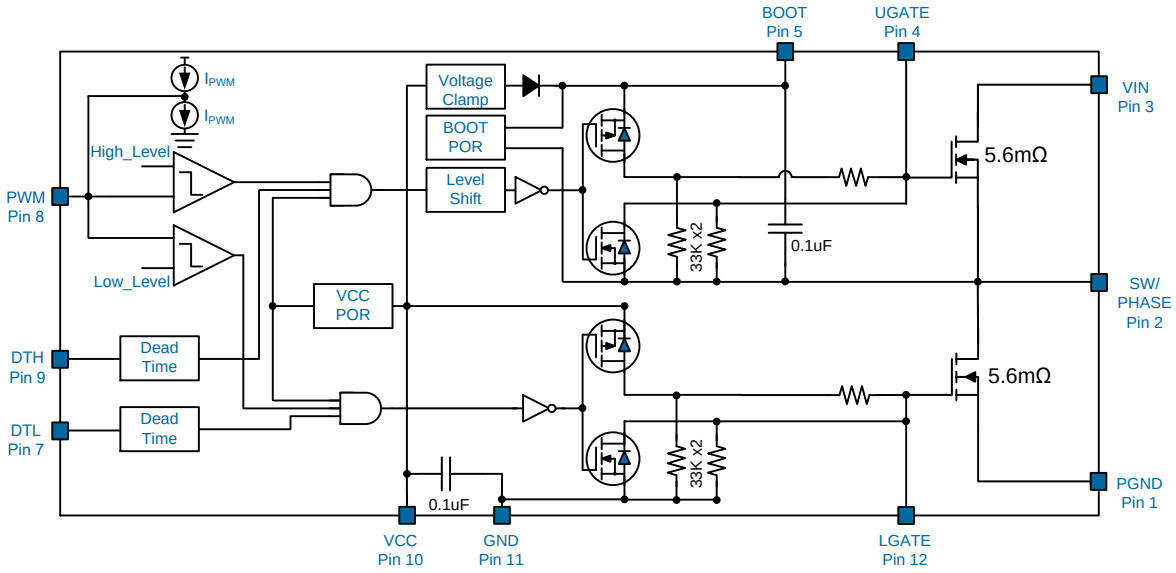

Fig. 2. uP9802Q block diagram.

Both versions include a UVLO for high-side and low-side drivers, short propagation delays, high side to low side matching propagation delays, integrated boot and V_{CC} decoupling capacitors, and low-C_{OSS} GaN FETs. A voltage clamp to prevent overvoltage damage to the GaN FET gates offers added protection. Gate "hold down" resistors are utilized to protect GaN FET gates from damage during start-up and assembly operations.

Packaging

Both devices come in an ultra-low profile of 0.625 mm (max) in a PLP5x6-12L package (Fig. 3).

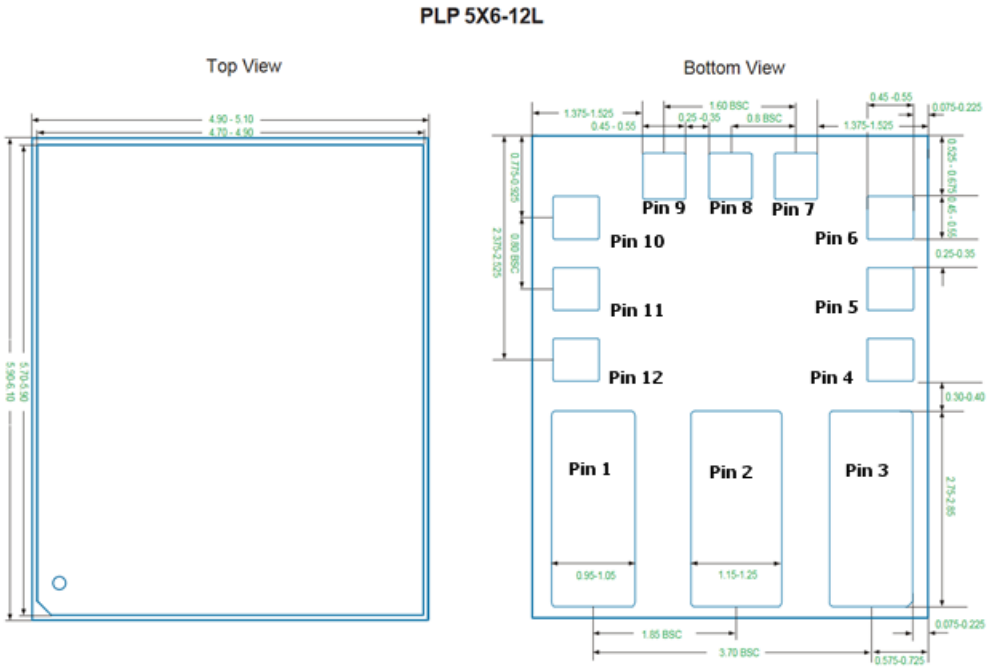

Fig. 3. Packaging drawing—top and bottom views.

In typical semiconductor packaging, bonding wires are used for interconnections from silicon to package pins and from silicon die to silicon die within the device's package, adding parasitic inductance and resistance. In contrast, interconnections within the uP98XX family are accomplished by "flat," low inductance paths; no bonding wires are used.

Additionally, the integration of many components that would typically be external such as boot capacitor, boot diode, and high-frequency V_{CC} bypass capacitors, helps save PCB space, lowers cost, increases robustness, and lessens layout criticality and PCB stack-up requirements.

The package has low thermal impedance allowing the heat to get out of the GaN devices to the PCB. Values of 5.1°C/W $\theta_{J\text{-}PCB}$ are guaranteed. Pads 1,2 and 3 are large in size both to accommodate large currents and as a thermal path to the PCB.

Single-Input Architecture

The uP9802Q has a single PWM input that is tri-state capable and is the only external signal required as dead times, both high-side and low-side turn-on delay, are adjustable via external resistors (see Fig. 2 again).

Dual-Input Architecture

The uP9801Q has dual inputs, one for the high-side and one for the low-side GaN FETs (see Fig. 1 again). The two inputs are generally used in Class D audio and digital power applications. The conduction timing of the two GaN FETs is to be controlled externally, usually through digital processing. It is possible to turn on both GaN devices simultaneously in the uP9802Q, so care must be taken to prevent this occurrence, or failure of the power stage may result unless current limiting techniques are used.

An Example Application: 48 V To 12V, 180 W

Accomplishing this conversion can be done through several different topologies. The following is not an exhaustive list, but identifies some of the popular topologies that may be applied at these voltage and power levels.

Nonisolated topologies:

- Bidirectional nonisolated
  - Full bridge, bidirectional buck-boost converter (four switches, one storage element)
  - SEPIC or ZETA converters (two switches, four storage elements)
- Unidirectional nonisolated
  - Synchronous buck converter (two switches, one storage element)

Isolated topologies:

- Full bridge (four switches, one storage element and a transformer)
- Half bridge (two switches, three storage elements and a transformer)
- LLC resonant topologies (four switches and a transformer).

As can be observed, the least-complex solution is the synchronous buck converter. All other solutions require more switches and additional storage components. This article will focus on the synchronous buck solution for which an example application circuit is shown below in Fig. 4. But please note that the new uPI GaN power stages can be used in all of the topologies listed above.

Example Application Circuit

The 48-V to 12-V synchronous buck converter described in this section is implemented using the uP9802Q integrated GaN power stage with a single input. The simplified schematic shown in Fig. 4.

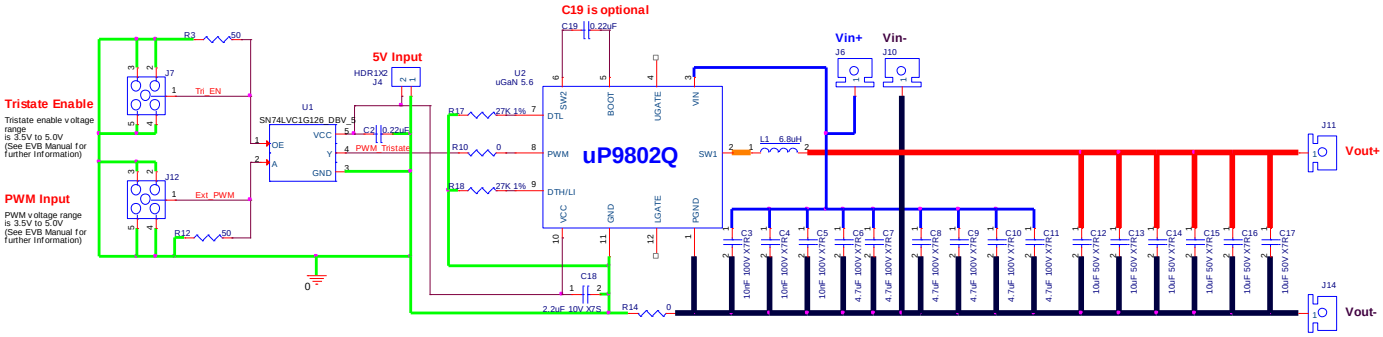

Fig. 4. Simplified schematic of a 48-V to 12-V, 180-W synchronous buck converter. (A complete schematic is available on request.)[1]

Our test PCB was a six-layer board with 1-oz copper on top and bottom, and 2-oz copper on all inner layers. Fig. 5 shows the layout of the topside of the board, while Fig. 6 shows the populated test board with test probes attached. The efficiency and power loss measurements obtained from the test board are presented in Figs. 7 and 8. An infrared image in Fig. 9 provides a visual of the thermal performance of the test board.

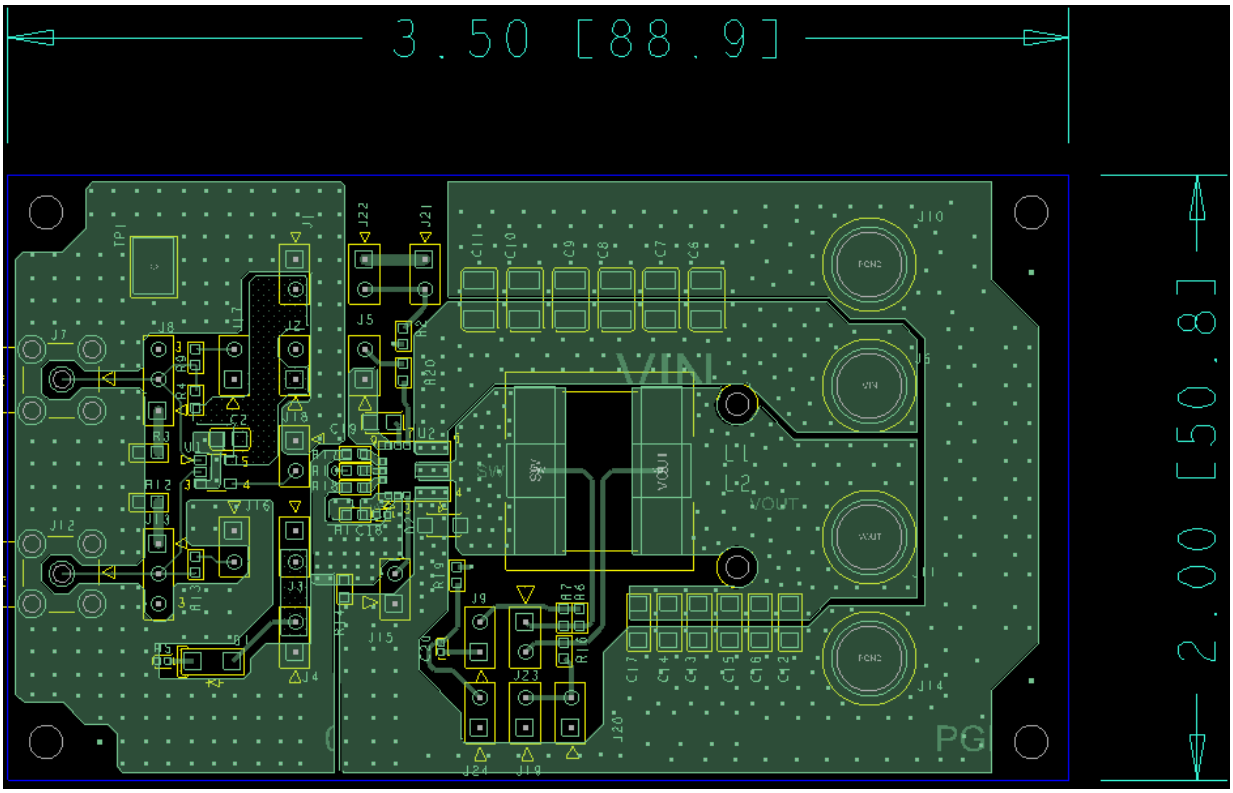

Fig. 5. Top layer of the test PCB featuring the uP9802Q GaN power stage.

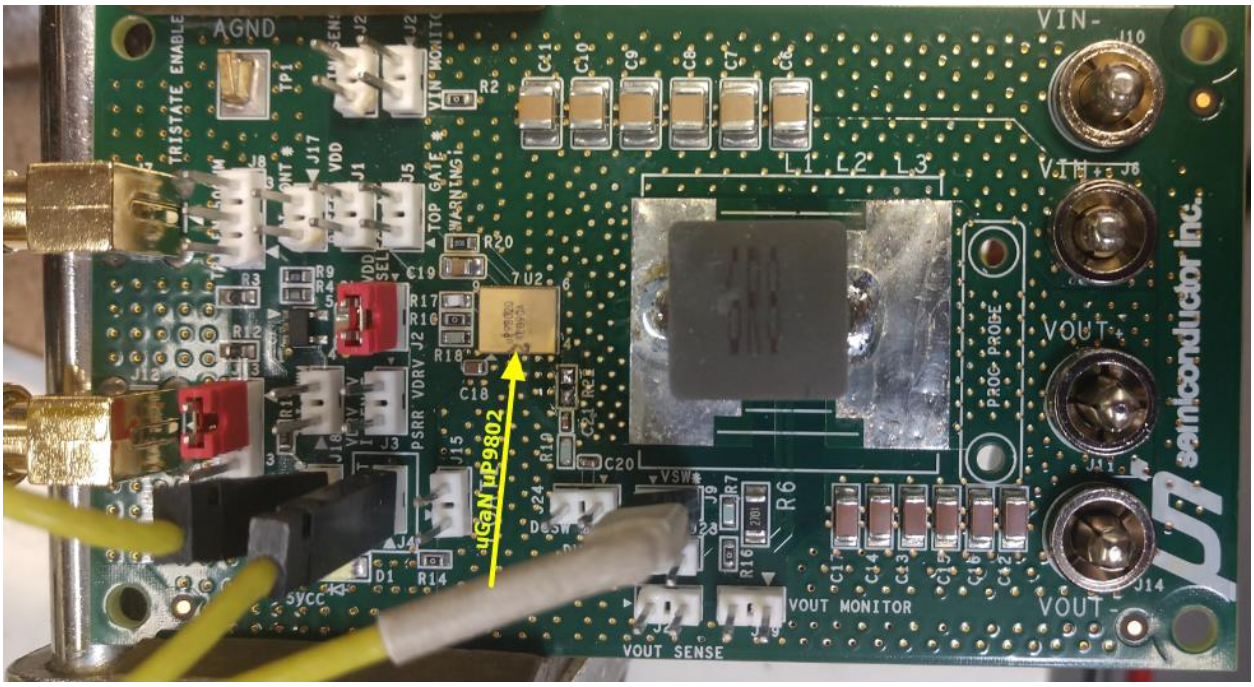

Fig. 6. Test set-up for the test PCB.

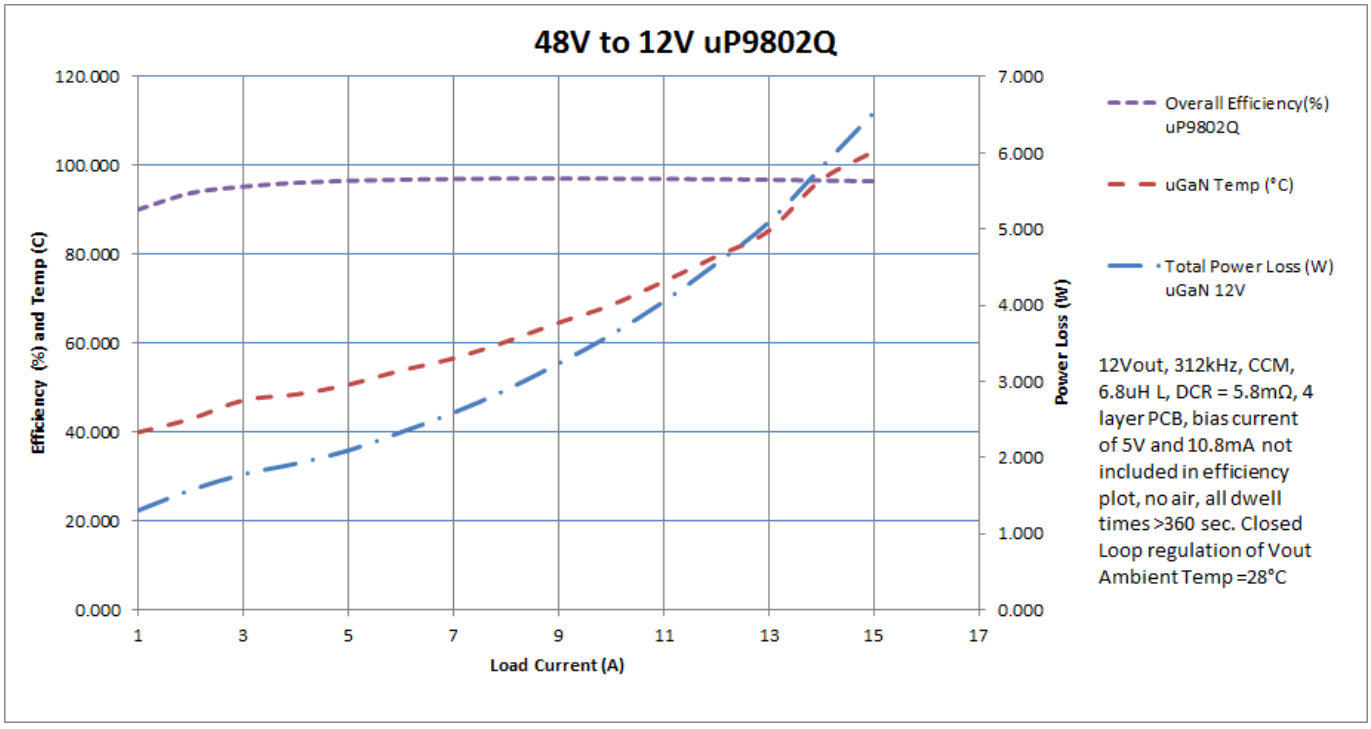

Fig. 7. Overall electrical and thermal performance for the example converter based on the uP9802Q.

The converter based on the uP9802Q has very high efficiency; greater than 96% from 30 W to 180 W with 97.3% peak efficiency at 108 W. The uP9802Q bias current is only 55 mW.

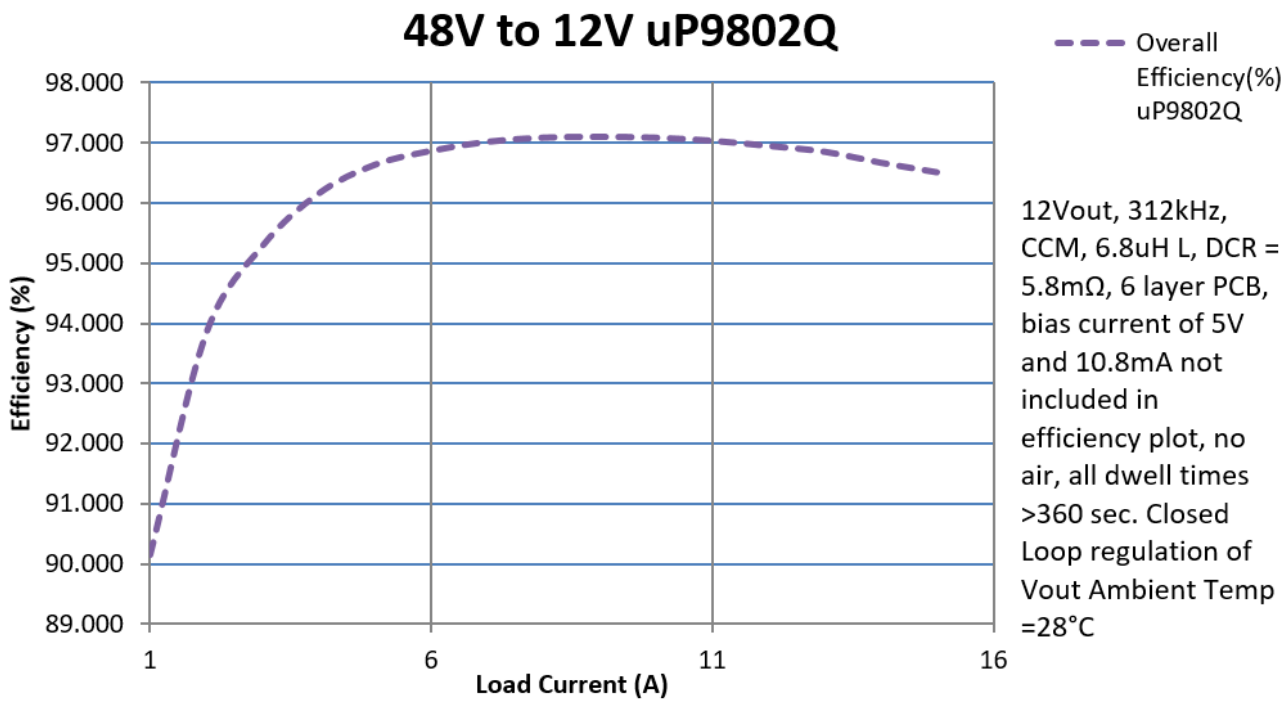

Fig. 8. Expanded efficiency plot.

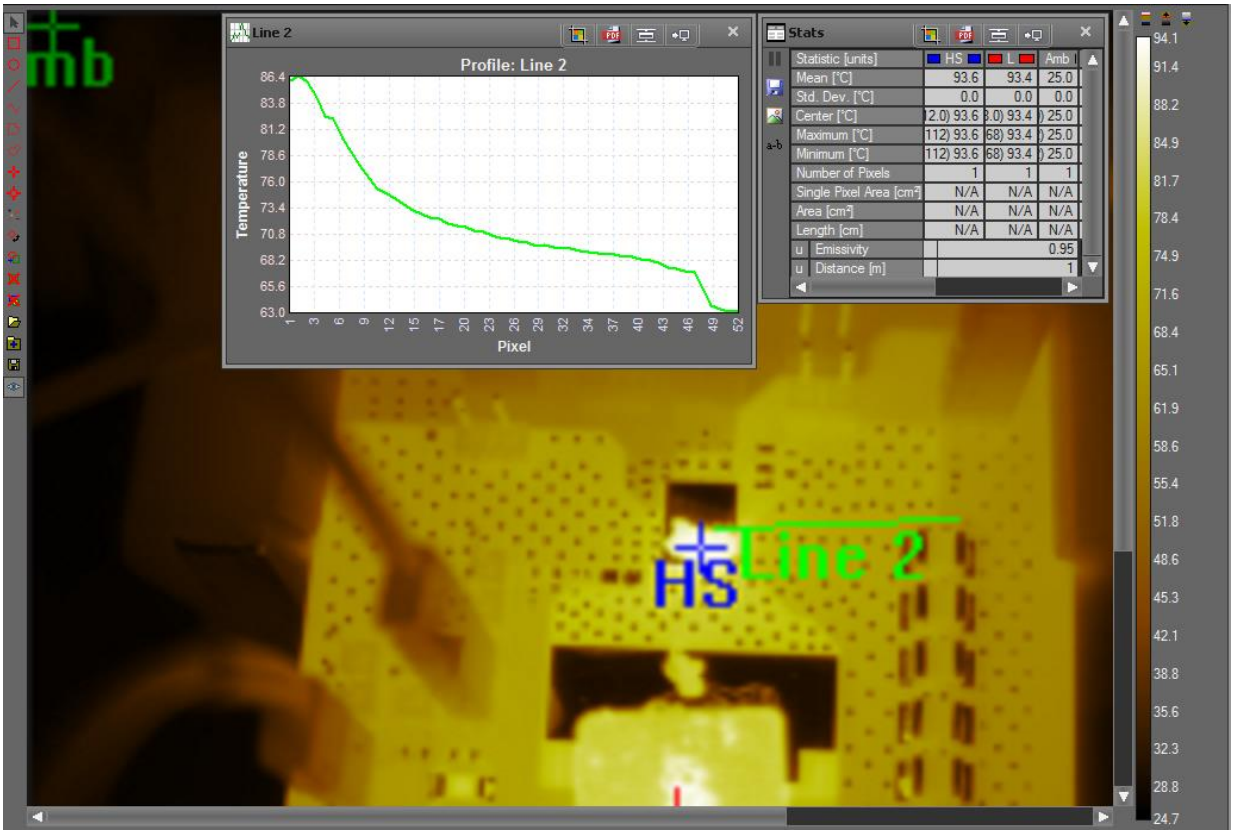

Fig. 9. IR image of test PCB.

In the thermal image in Fig. 9, HS (hot spot) is the hottest spot on the PCB as measured at the uP9802Q, L is the inductor temperature and Amb (upper left-hand corner) is the ambient temperature. The temperature plot in Line 2 shows excellent heat spreading, from which we conclude that the PCB layout is suitable thermally.

The thermal image above has been taken with only convection cooling of the test board. In this case the hot spot temperature, measured at the GaN power stage, is 93.6°C. Applying a modest amount of airflow can produce a notable impact on losses and efficiency at the high end of the load range.

When 1.7 m/s of airflow is applied (with 35% relative humidity and at 10-ft altitude), the maximum temperature of the test board falls to 72°C.

These temperature measurements were taken with the test board configured for 48-V input and 12-V output at up to 15-A max. out. The converter operates at a 320-kHz switching frequency. The inductor is a Mag Layers MMD-12HZI6R8M-M1-RI, which measures 13.2 x 12.9 x 8 mm, and has an inductance of 6.8 µH and a DCR of 5.8 mΩ. The single-phase converter is tested in a closed-loop configuration and the six-layer test board operates in a 27°C ambient. The required bias power was measured at 53 mW.

Fig. 10 illustrates the difference in efficiency and power loss at 1.7 m/s versus the case of convection cooling.

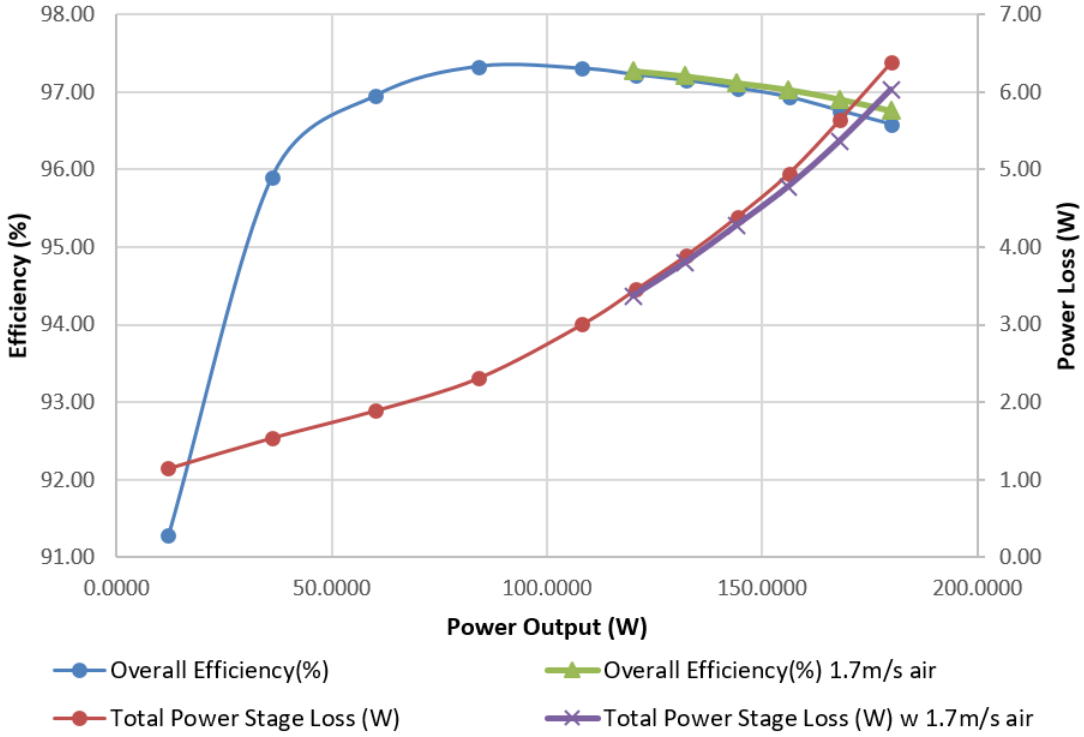

Fig 10. Efficiency and losses of converter test board measured with and without 1.7-m/s of airflow.

Switching Performance

Measurement of switching waveforms when using GaN can be difficult. The edges are very fast, and while this is good for efficiency, it is not as good for EMC and measurement. Our test board uses an RF technique to look into a 50-Ω input to our oscilloscope.

In effect, we create a 2.5-kΩ probe using a 2.7-kΩ 1% resistor in parallel with a 27-kΩ resistor on the PCB near the Lx switch node, which is then run into the 50-Ω input of the scope creating a 50-to-1 attenuator (Fig. 11).

The bandwidth is much higher than most scope probes (a network analyzer shows the 3-dB point is 700 MHz with the proper coaxial cable).

This technique results in a less expensive measurement method as a 1-GHz probe is more costly than the resistors. The downside is that it has a more significant effect on measurement accuracy than a high-frequency probe with a higher impedance. The resulting power loss can also affect efficiency measurements at lighter loads.

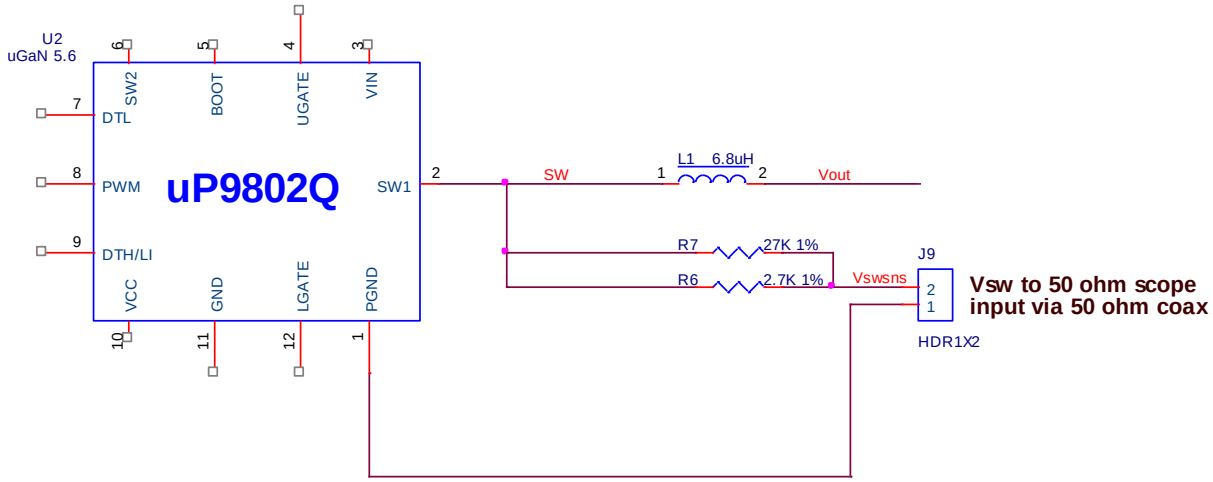

Fig. 11. 50-Ω measurement technique.

Fig. 12 offers examples of both the rise time on the Lx switch node and the dead time that can be expected.

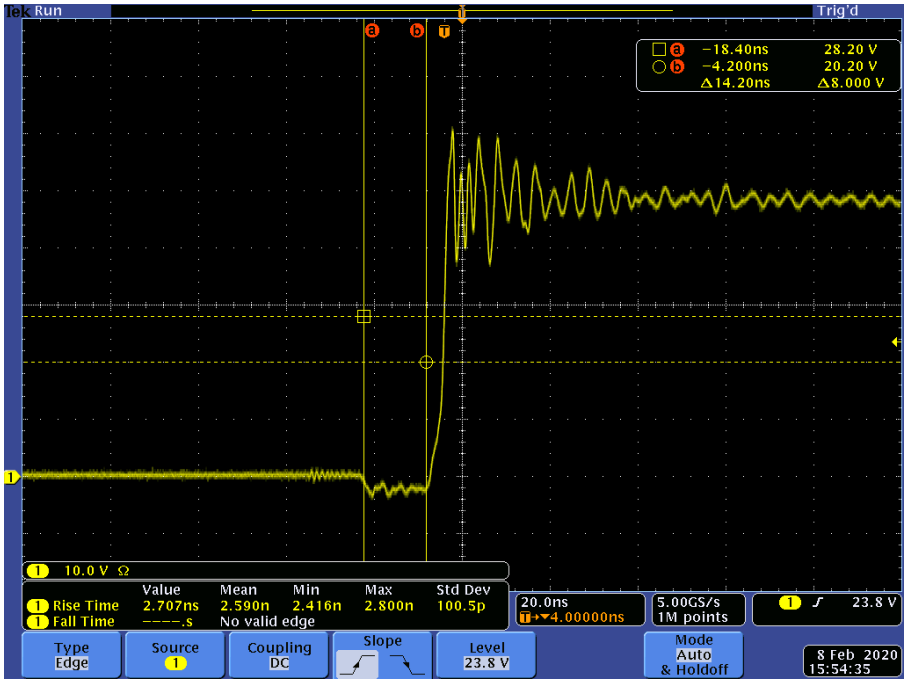

Fig. 12. Rise time and dead time measured for the uP9802Q on the test board.

Fall times are also in the 2-ns region when operating at 48 V as shown in Fig. 13.

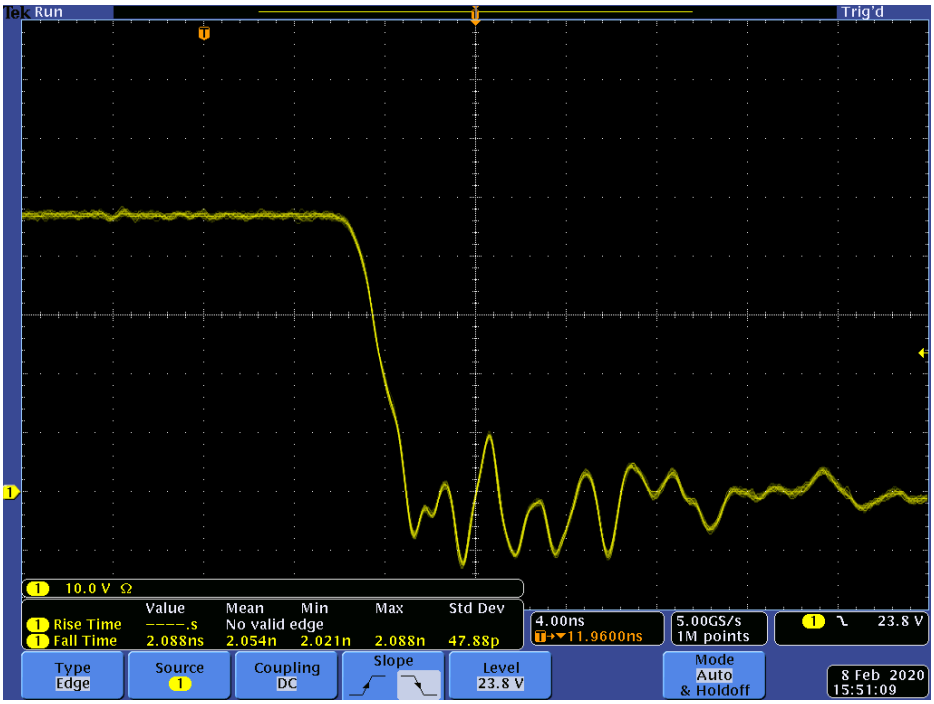

Fig. 13. Fall time measured for the uP9802Q on the test board.

Inductors

As the switching ability of semiconductors improves, their losses decline, and more focus is placed on the inductor as its loss term is a more significant percentage of the overall losses in the regulator. Fig. 14 compares overall inductor losses versus power stage losses and also provides a breakdown of the inductor losses into core and winding losses. This is an example of what the relative losses are in this regulator for a given inductor.

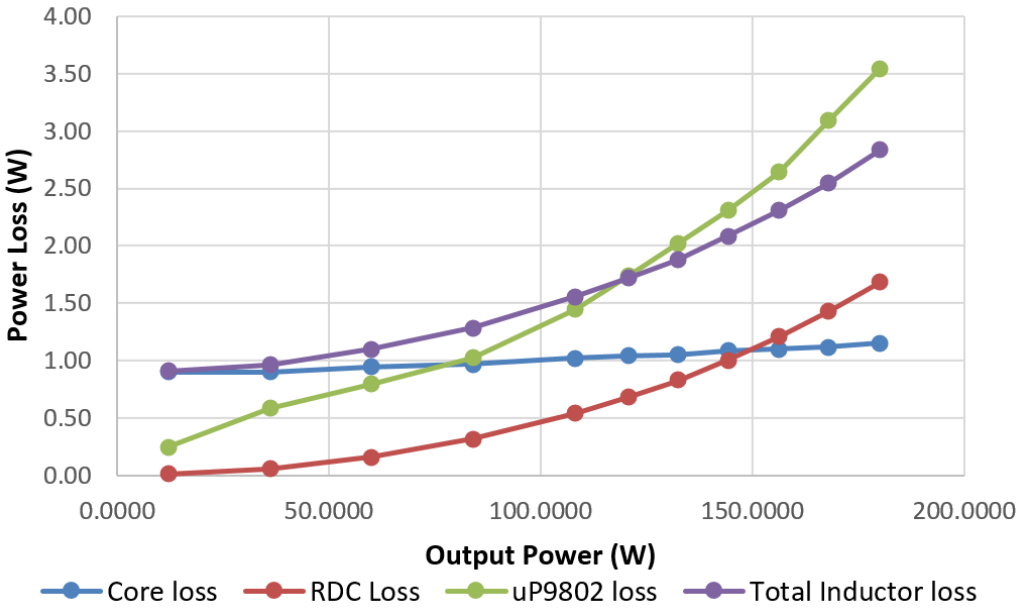

Fig. 14. Comparing the contributions of inductor and power stage losses.

Ferrite cores offer the lowest loss, allowing the operating frequency to be raised as high as 500 kHz with little effect on efficiency.

A video presentation that has further information about this example application is available online.[2]

Conclusion

The new family of uGaN devices will help improve performance in many applications where simplicity and efficiency are needed. The improved switching times decrease losses in applications of 48-V to 12-V regulators and make possible more integrated designs with enhanced ease of use.

References

1. For a complete schematic of the 48-V to 12-V, 180-W synchronous buck converter, email the author.
2. "An Introduction to uGaN, 80V Integrated Power Stage Family," video presentation by Ron Vinsant, uPI Semiconductor.

About The Author

Ron Vinsant is a senior member of Technical Staff at uPI Semiconductor. With more than 30 years of experience in analog and digital power systems design, he has demonstrated success in engineering and application engineering roles at technology companies both large and small, including Vishay Siliconix, Powervation, Fairchild, Zilker Labs, SOMA Networks, Linear Tech and Teledyne. Prior to joining the power industry, he studied physics at U.C. Berkeley, Calif.

For more on designing power converters using SiC and GaN devices and related product news, see How2Power's Special Section on Silicon Carbide and Gallium Nitride Power Technology.