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Developing A 25-kW SiC-Based Fast DC Charger (Part 6): Gate Drive System For Power Modules

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In parts 1 through 5 of this series[1-5] we've extensively described the development of a 25-kW EV charger from a hardware perspective and a control strategy. Fig. 1 represents the system discussed until now.

Here in part 6, we turn our attention to the gate-drive circuitry needed to drive SiC MOSFETs. These transistors are quickly proliferating in the power semiconductor market as they become more efficient and reliable. As more devices become available in the market, it is important for designers to understand both the commonalities and the differences between SiC MOSFETs and the silicon (Si) IGBTs and Si superjunction (SJ) MOSFETs so that the user can get the most out of each device.

This article is based on the lessons learned while building a 25-kW fast EV charger using new SiC modules from onsemi. Those modules use onsemi's M1 1200-V SiC MOSFETs. We will see how to design and tune the coupled gate driver-and-SiC MOSFET combination in a high-power application.

In this design, we will use IGBT galvanic-isolated gate drivers from onsemi as a starting point and introduce improvements with the new dedicated SiC galvanic isolated gate driver. All gate driver families presented in this article share the same isolation technique and output stage technology.

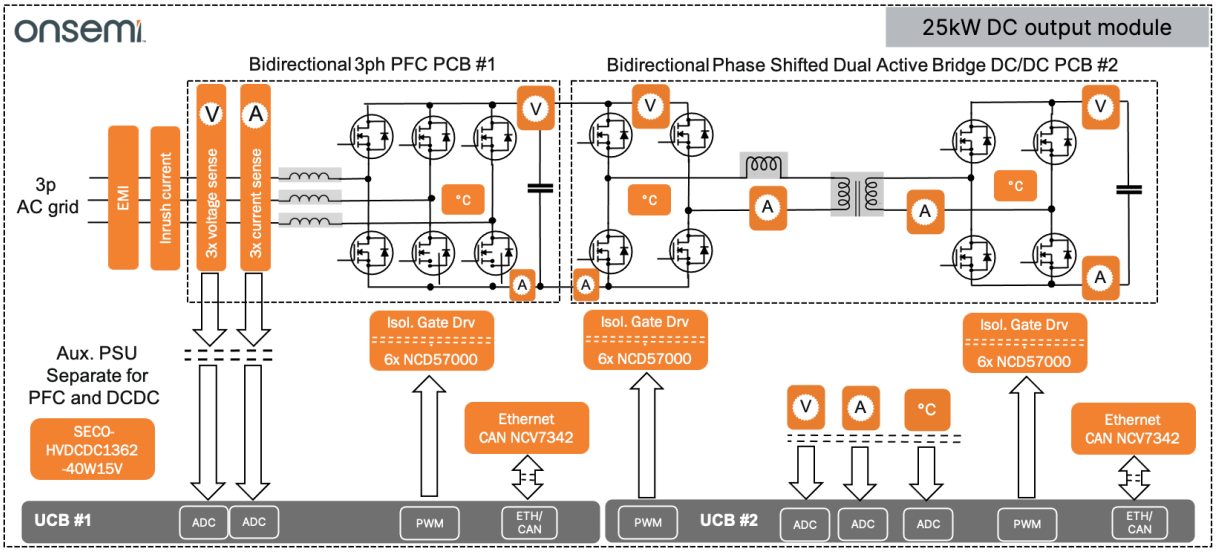

Fig. 1. A high-level block diagram of the 25-kW EV dc charger.

Gate-Drive Requirements: SiC MOSFET Vs. Si IGBTS Vs. SJ MOSFETs

For IGBTs and MOSFETs (Si and SiC), we must charge the gate to turn on the device and discharge the gate to turn it off. The current flow is somehow generic and can be seen in Fig. 2 for both cases.

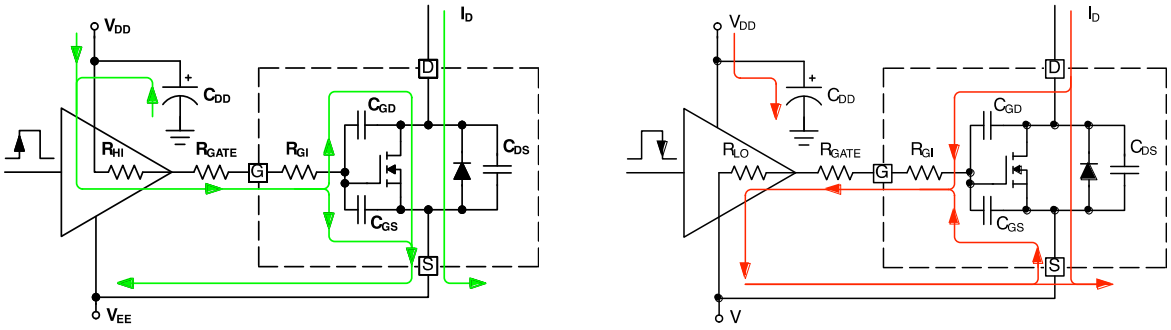

Fig. 2. The current paths in the gate-drive circuit are shown at turn-on (a) and turn-off (b) with green and red arrows, respectively.

However, the gate voltage ranges are different among those three devices (IGBT, Si SJ MOSFET and SiC MOSFET). For IGBTs, the on-voltage is around 15 V and the off-voltage is, generally, around -8 V. For SJ MOSFETs, the on-voltage is around 10 V and the off-voltage is typically 0 V. For SiC MOSFETs, as the $R_{DS(ON)}$ decreases when the gate voltage increases, maximum gate voltage can be applied for maximum efficiency. Therefore, the on-gate-voltage can vary from 15 V up to 20 V, depending on the technology or the generation.

Below an on-voltage of 15 V, the SiC MOSFET has a negative slope making it difficult to parallel devices. The off-voltage can be from 0 V down to -5 V. The onsemi SiC MOSFETs can be blocked with 0 V, -3 V or -5 V, depending on the compromise between the efficiency and complexity of the gate-driver circuitry, and, at some point, on the generation of SiC MOSFET used. The range of gate voltage (or the on-voltage) directly influences the undervoltage lockout (UVLO) needed for the gate driver.

As a first approach, IGBT gate-driver output voltage range is more similar to SiC MOSFET needs than to those of SJ MOSFETs. First, it is highly recommended to use a negative-bias gate drive with SiC MOSFETs (as for IGBTs) in switching applications to reduce ringing in the gate−source drive voltage of the power transistor during high di/dt and dV/dt switching due to the parasitic inductances introduced by non-ideal PCB layout. Also, as our SiC MOSFETs have a threshold voltage around 1.5 V, negative voltage blocking offers a larger margin for noise (induced by dV/dt and di/dt) to create an unwanted turn-on during the off-state.

Secondly, with negative blocking, the leakage current during off-state is lower. So, the static losses will be lower. Finally, turn-on and turn-off times are faster or shorter with negative blocking than with zero-voltage blocking.

To obtain fast turn-on and turn-off, or to maintain the output settle during drain/collector voltage transients, a very low output impedance is needed at the output driver stage. The maximum value for the drive current depends on the power rating of the applications and it is similar for all types of devices.

The maximum current required to charge the gate depends on

- the amount of gate charge needed
- the topology (hard switching or soft switching i.e., ZVS),
- the maximum dV/dt required to limit EMI with the (external plus internal) gate resistance.

Even if the (external plus internal) gate resistance limits the current value in the application, the driver should be able to source and sink current higher than the maximum current required. This will help to have a safe margin to maintain the needed maximum current at the maximum operating temperature and will prevent driver self-heating to reduce current capability.

As turn-on and turn-off speed increase dramatically with SiC MOSFETs versus IGBTs or SJ MOSFETs, SiC devices can operate at a much higher switching frequency compared to Si devices. As a consequence, in a half-bridge configuration, the switching node voltage can vary at a very fast rate. High dV/dt up to 100 V/ns can be achieved with SiC MOSFETs. The driver should be able to source and sink the required current induced by the

dV/dt applied to the gate by the Miller capacitor (or capacitor in-between drain/collector and gate). The gate-driver output signal should remain set to its value given by the input signal during this dV/dt transient.

Complementary to the sink current capability or to reenforce Miller effect current absorption, a gate clamp can be used. This clamp will reenforce the blocking voltage with a very low impedance and bypass the blocking or turn-off gate resistor. The clamp is used after the turn-off and until the early beginning of the turn-on. This technique is used for very high power when devices with large Miller capacitance are driven. This is our case here, in this 25-kW EV charger application.

Also, in the case of an isolated driver or a floating driver, the common mode transient immunity (CMTI) between driver input and output stages should be stronger for SiC device drivers than for silicon device drivers. The gate drive voltage applied should remain stable.

To conclude, no glitch should be seen at the driver output during dV/dt on the switching node, on drain/collector or between driver input and output stages for all types of switches. But, as SiC MOSFETs are much faster, the SiC MOSFET driver should be much stronger on those requirements (higher CMTI and dV/dt immunity levels, higher current rating and lower output impedance).

As we have a half-bridge architecture with high switching speed, timing is an important point to look at. We need to consider two timing parameters when devices operate in half-bridges: Propagation delay from input to output and the delay-mismatch between two drivers or two outputs.

For SiC, as the switching frequency can be above 100 kHz, the propagation delay could affect duty cycle accuracy. A mismatch will affect deadtime between switches. For a SiC driver, propagation delay below 50 ns and delay mismatch below 10 ns are suitable.

For high-speed applications, SiC MOSFETs can be driven by a Si or SJ MOSFET gate driver, which are normally faster than IGBT drivers. But, they may not be able to provide the required output voltage range. The on-voltage on these drivers (or the output voltage swing) is often limited to 15 V. This is too low for SiC MOSFETs. Also, most of the Si MOSFET drivers do not provide negative blocking.

Specific Requirements For A 25-kW Application

Desired Rise/Fall Times And Required Source/Sink

As we want to control EMI, we will limit the dV/dt but not too much in order to have small dead time (or fast turn-on/-off time) and high efficiency. As stated in AND90103/D,[6] with a gate resistor in the range of 2 to 5 Ω, SiC MOSFET dV/dt could be in the range of 20 to 40 V/ns. So, the gate resistor was selected with this range in mind. The gate resistor value selection was tuned and verified with SPICE simulation by evaluating dV/dt during turn-on/-off times.

Isolation Level

During hardware development, we follow the IEC-61851 standard which requires us to follow IEC-60664-1 rules. We assume the working voltage is close to 1000 V maximum. Those requirements guide us to use the NCD57000[7] gate driver. This driver has a dielectric strength isolation voltage of more than 5 kVrms, a working voltage V_{IORM} capability of more than 1200 V and complies with UL 1577. The wide-body 8-mm creepage helps to fulfill creepage/clearance requirements.

Features And Protections

The following gate-driver features increase the robustness of a SiC MOSFET power implementation, raising the efficiency and reliability of the application. These key features are:

- Common-mode transient immunity is a critical parameter for SiC applications. The NCD57000 offers 100 kV/µs.
- Active Miller clamp
- DESAT protection

- Soft turn-off at DESAT.

All these features are included in the NCD5700 IGBT driver. It also includes negative drive or negative turn-off voltage.

Gate Driver Supply For SiC MOSFETs

Using the SECO-LVDCDC3064-SIC-GEVB[8] isolated power supply for SiC driving circuits provides the necessary stable voltage rails of −5 V and 20 V for driving a SiC transistor efficiently. The transformer safety specification complies to IEC 62368-1 and IEC 61558-2-16, with 4-kVac dielectric insulation.

Implementing The SiC Gate Driver

DESAT Protection Calculation

The desaturation current of SiC transistors was calculated based on AND9949/D.[9] DESAT current was set to trigger in the range of 85 to 115 A with the 14.3-kΩ resistor (Fig. 3). The DESAT current will be evaluated and fine-tuned in the prototype stage.

The following considerations have been taken into account:

V_{TH} = 9.0 V, $R_{DS(ON)}$ = 11 mΩ at 100 A, US1MFA with V_F =309.5 mV at 500 µA (simulated).

A 22-pF capacitor placed on the DESAT pin increases blanking time by 430 ns to obtain a total blanking time equal to 880 ns. As the internal filtering time of 320 ns is given in the datasheet, the total reaction time to a desaturation event is then equal to 1.2 µs. When you add in the time required to turn off the SiC transistor, the total time required for DESAT action is lower than 2.0 µs.

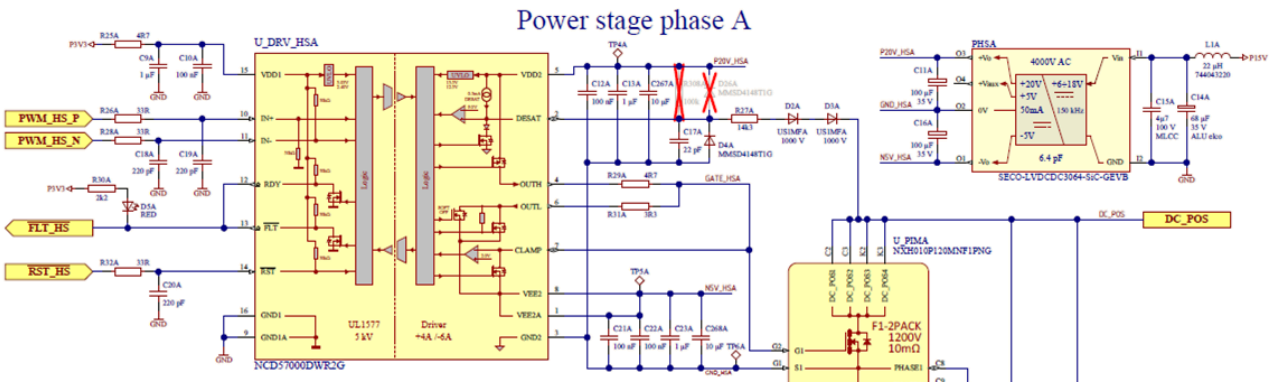

Fig. 3. Gate driver NCD57000 connection with calculated DESAT function component values.

Verifying SiC MOSFET Switching With Simulations

The PFC as well as the dc-dc power stage simulation models included a gate-driver model in order to evaluate switching performance with gate-source resistors R_{G1} = 1.8 Ω and R_{G2} = 100 kΩ (See Fig. 4 for R_{G1} and R_{G2} definitions or locations).

In this case, only R_{G1} plays a role in discharging the SiC MOSFET gate capacitor. The PFC model incorporates the three half-bridge SiC-modules as well as the gate drivers. But only one half-bridge connection is shown in Fig. 4. The SiC module SPICE model was discussed in part three of this series.[3]

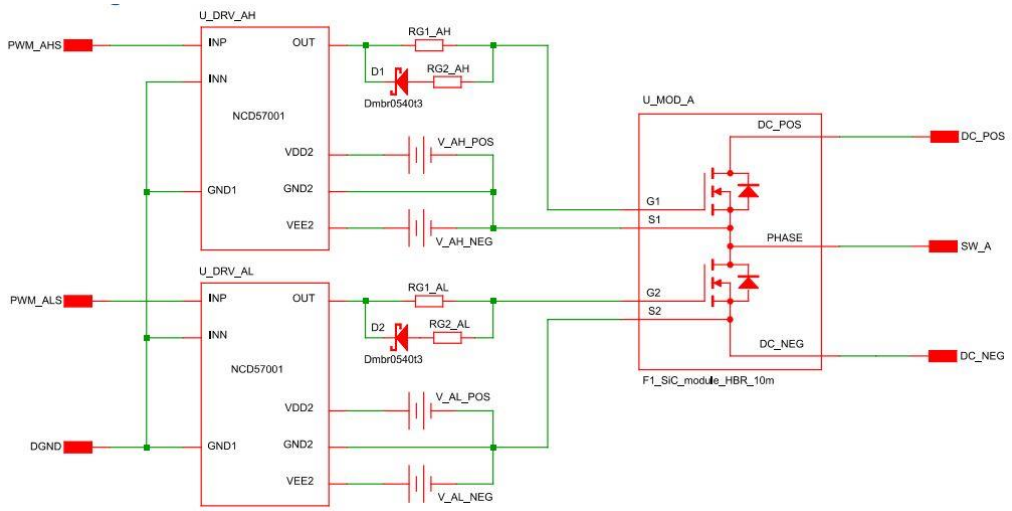

Fig. 4. Power stage with gate driver model for PFC phase A.

The driver stage will significantly impact the performance of the system (even moreso for SiC-based systems). Therefore, it is highly recommended to include it in the simulation—at least to some extent.

One challenge is that existing gate-driver models are often very complex, they slow down simulation and increase simulation runtime because they include all features of the driver (like UVLO, clamp, DESAT, etc.). In general, for power stage simulation and, more specifically, for the goals of this project, a simplified gate-driver model is sufficient. One was built including only the propagation delay and the output stage characteristics or performances.

Even though detailed I-V characteristics are usually not readily available in various drivers' datasheets, using the specified driver output capability (sink $I_{PK-SNK1}$ and source $I_{PK-SRC1}$ peak currents, see NCD57001 datasheet [10]) for certain given points, in combination with propagation delay information, results in an approximation of the output characteristics. This approximation improves the simulation accuracy while still providing acceptable simulation time. Fig. 5 shows the NCD57001 gate-driver SPICE model that was created based on datasheet values.

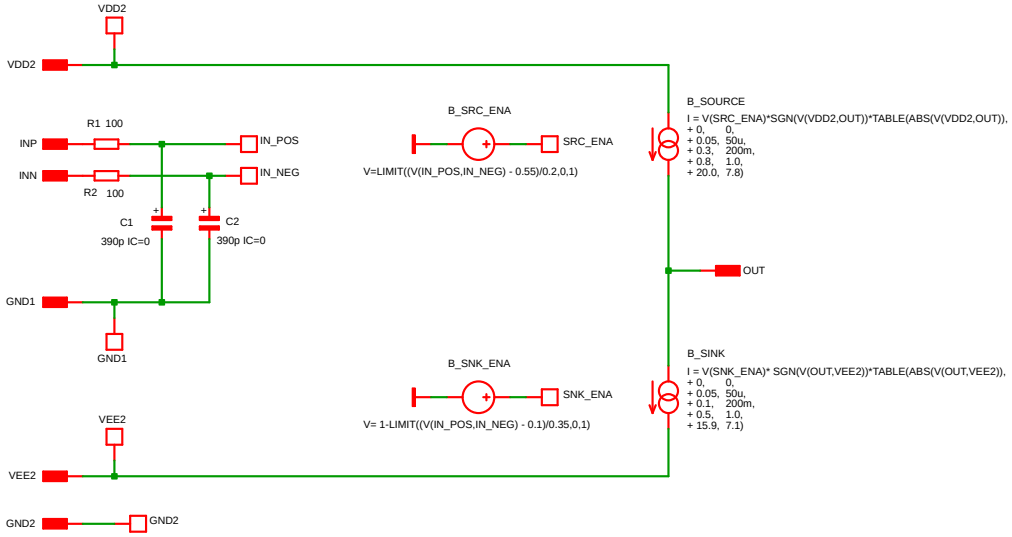

Fig. 5. A streamlined NCD57001 SPICE model based on datasheet values.

Simulations Of Switching Transitions: Turn-On And Turn-Off

One of the key parameters in evaluating the switching performance of the PFC stage is the speed of the switching transitions (see Fig. 6), or in other words, the dV/dt of the MOSFETs. In theory, the faster the switching transitions, the lower the exhibited switching losses and the better the efficiency.

However, there are other limitations on the switching speed. For example, the capability of the transistor itself to sustain such high gradients, and EMI or other common-mode (CM) noise generated by fast transitions. Layout itself and the parasitic inductances and capacitances also add to the limitations.

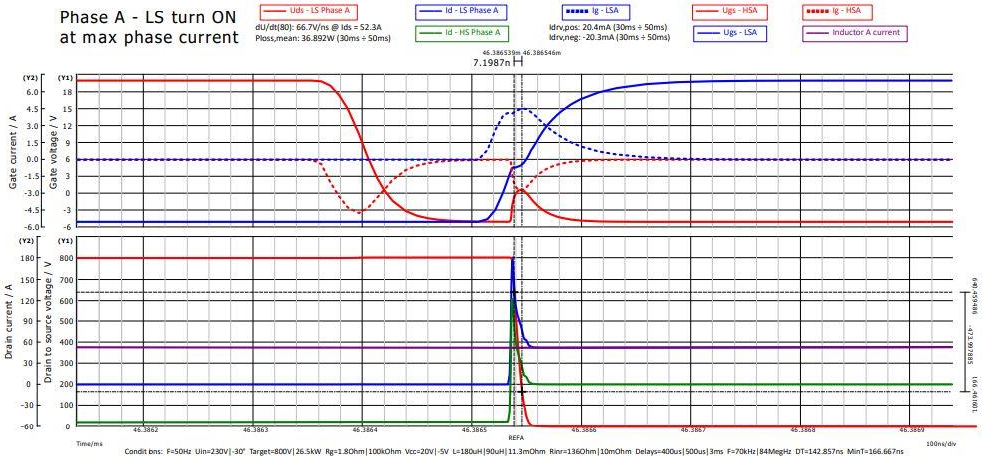

Fig. 6. Typical turn-on waveforms for the PFC stage MOSFETs.

Fig. 7 shows dV/dt values in excess of 66 V/ns with the configuration given for this simulation. Such values represent really fast transients indeed, only enabled by wide-bandgap technologies. Actually, such high dV/dt values could become harmful (even for SiC modules) and high overvoltage spikes could be generated by the parasitic inductances in the actual application, easily surpassing the maximum V_{DS} rating of the component.

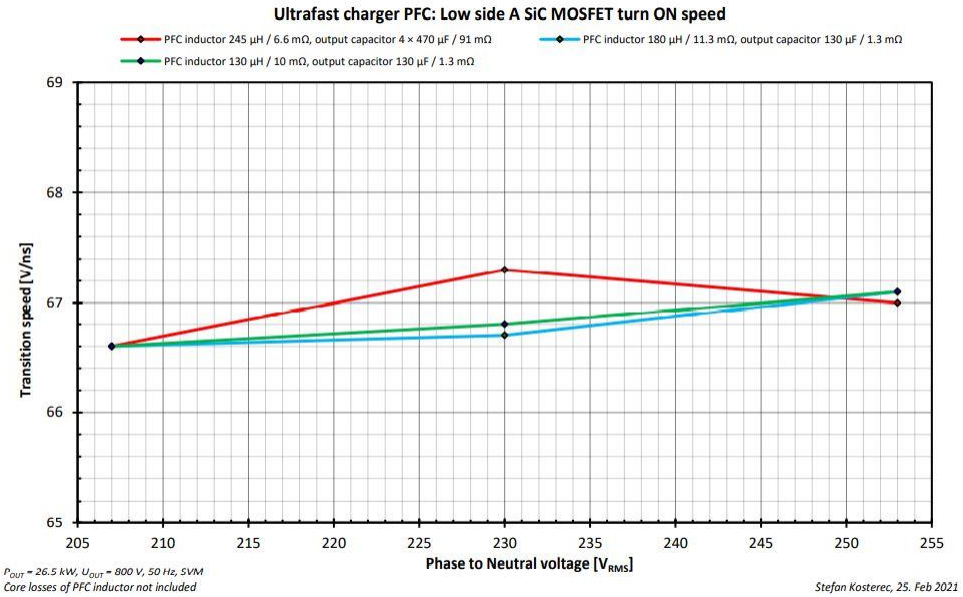

Fig. 7. Low-side phase A SiC MOSFET turn-on speed as a function of input voltage and inductor and output capacitor values.

Modifying the value of the gate-source resistor (for the turn-on) is the simplest way to reduce the dV/dt. A higher gate resistor value will result in slower transitions, and bring the application on the safer-side, with the tradeoff of a small additional power loss (as the transition will be longer).

Based on the results of this simulation, it was decided to increase the original 1.8-Ω gate source-resistor value to a value in the range of 2.5 to 4.7 Ω. With this value, we keep the turn-on transition speed around 25 V/ns, which serves as a good compromise. This will be the starting value used to evaluate the actual hardware.

Regarding the turn-off transitions, a similar approach has been followed. Figs. 8 and 9 show the results of these simulations. The off-transitions are also fast (up to 40 V/ns) with 1.8-Ω gate sink-resistor (the same value as was used in turn-on simulation). The sink resistor value will be increased to 3.3 Ω in the prototypes to tune the off-transition to around 25 V/ns.

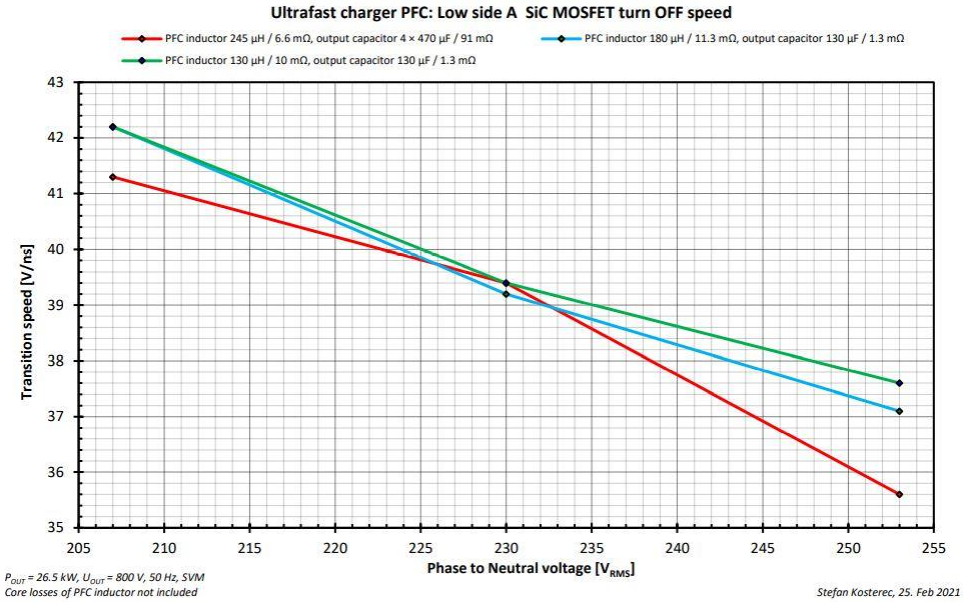

Fig. 8. Low-side phase A SiC MOSFET turn-off speed as a function of input voltage and inductor and output capacitor values.

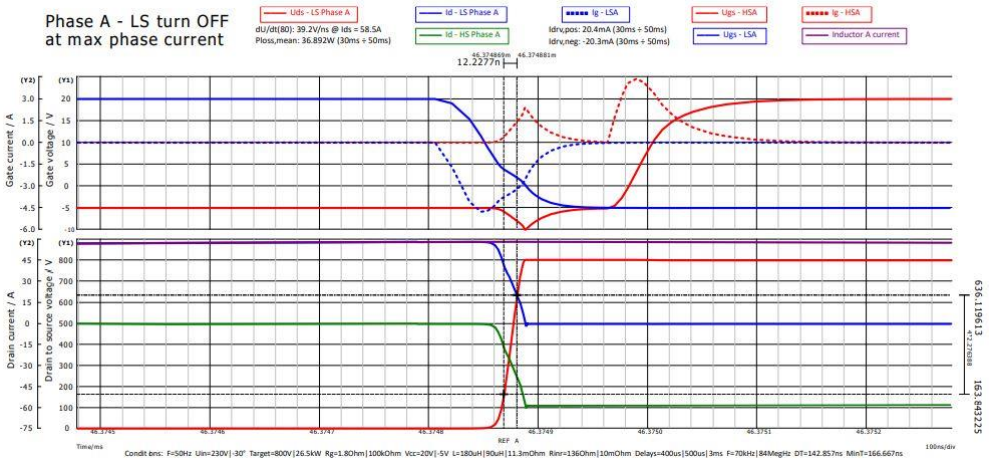

Fig. 9. Typical turn-off waveforms of the PFC stage MOSFETs.

PCB Layout And Recommendations

SiC drive circuitry layout is critical in SiC power design in order to eliminate or minimize PCB parasitics. Here are some recommendations and examples of good layout arrangement in Figs. 10 and 11. Source, sink and clamp tracks (see Fig. 10) should be as short as possible. The sink/source path is closed by V_{DD} and V_{EE} decoupling capacitors (as shown in Fig. 102). They have to be placed as close as possible to V_{DD} and V_{EE} gate driver pins as shown in Fig. 11.

Capacitors should have a value large enough to feed the sink and source current peaks while maintaining the V_{DD} and V_{EE} level. Those decoupling capacitors should also have very small parasitics and be the high-frequency type.

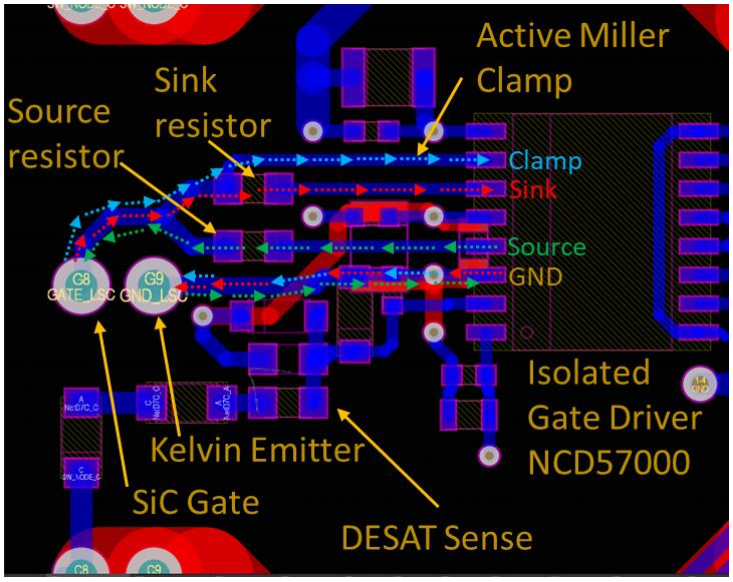

Fig. 10. SiC gate-driving circuitry PCB layout. Arrows show source, sink and clamp current paths in green, red and light blue, respectively.

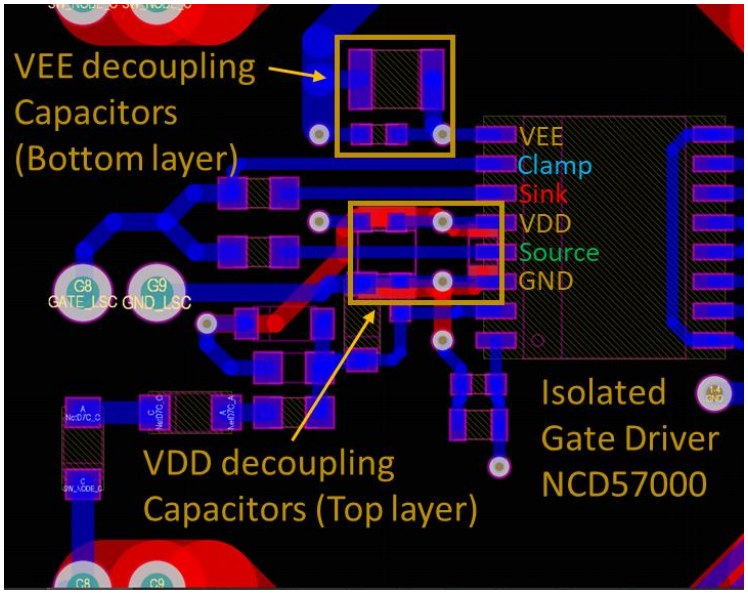

Fig. 11. Recommended placement for V_{EE} and V_{DD} decoupling capacitors.

Future Enhancements For SiC Gate Drive

The NCD570xx IGBT gate driver family discussed above is adequate for the SiC MOSFET gate driver requirements in high-power applications. However, with an advanced version of the galvanic isolation transformer, faster transmission times and less delay mismatch can be obtained.

Incorporating this improvement, the newer NCP5156x[11] gate driver family, can also be used to drive SiC MOSFETs. Gate voltage range has been tuned to comply with SiC MOSFET gate on/off voltages for all generations. The UVLO has also been adapted to the gate voltage range values.

The major features of the NCP5156x family include a propagation delay of 36 ns typ. with 8-ns maximum delay matching per channel; an output supply voltage from 6.5 V to 30 V with 5-V, 8-V, and 17-V UVLO threshold, a CMTI >200 V/ns; 5 kVrms (UL 1577 rating) of galvanic isolation from input to each output and 1200-V peak differential voltage between output channels; user programmable dead-time and 4.5-A/9-A source and sink peak current (Fig. 12).

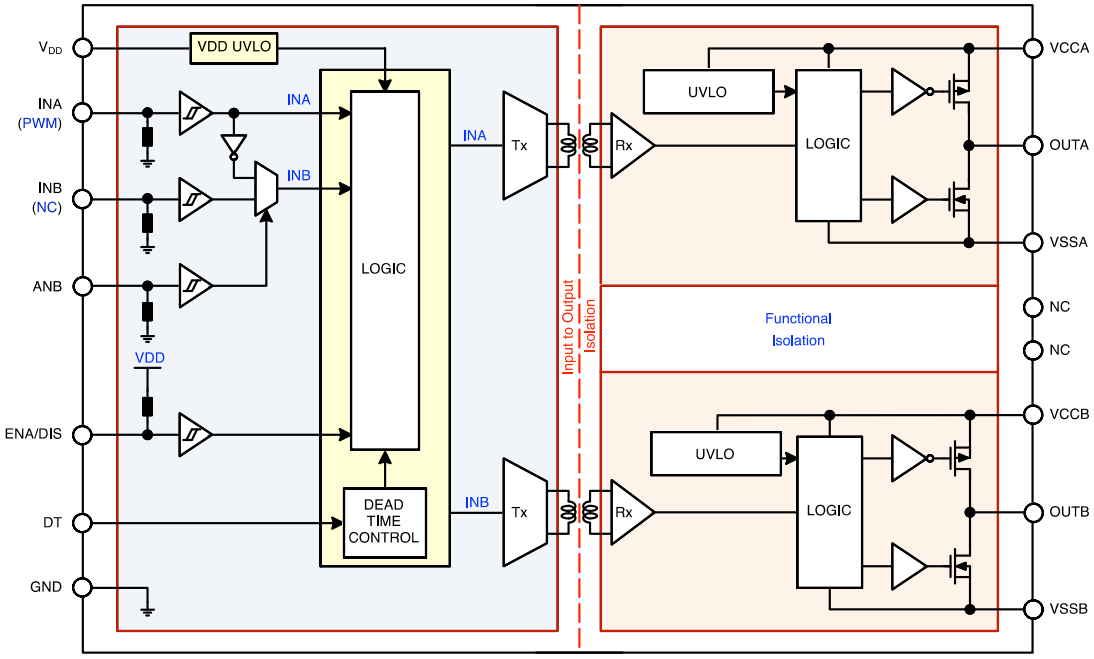

Fig. 12. NCP51561 block diagram.

When only one power supply (or unipolar) rail is available for the output stage, the following schematic with a Zener diode can be used to obtain a positive and negative supply (or bipolar) voltage (see Fig. 13).

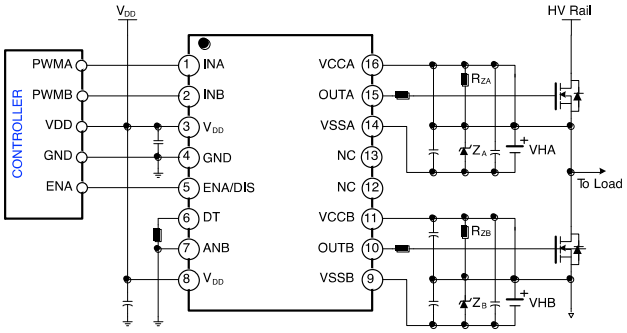

Fig. 13. Negative bias with Zener diode on a single isolated-bias power supply.

Fig. 14 shows the experimental results of the negative bias with Zener diode on a single isolated power supply of the NCP51561 for a SiC MOSFET gate-drive application. The example was designed to have a +15-V and −5.1-V drive power supply referenced to the device source by using the 20-V isolated power supply.

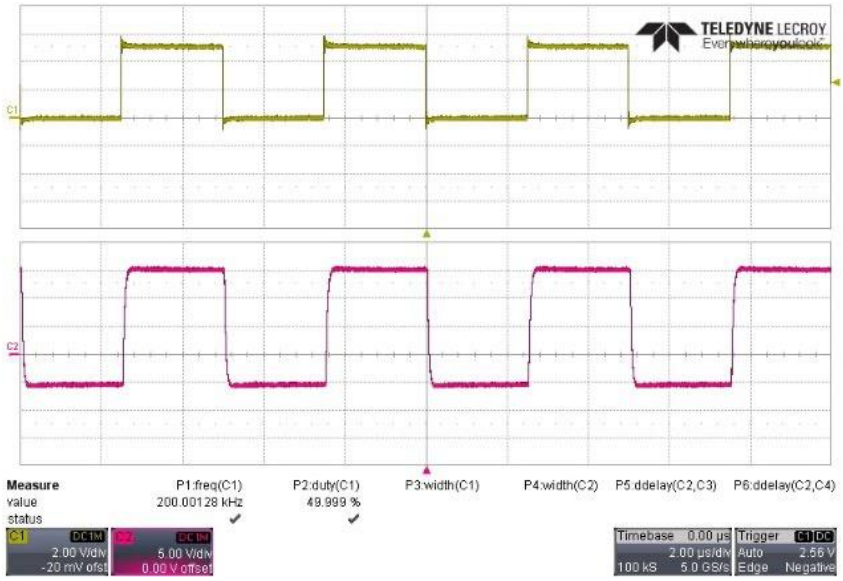

Fig. 14. Experimental waveforms of negative bias with Zener diode on single isolated power supply (with CH1: input [2 V/div], and CH2: output [5 V/div]).

As the NCP5156x ICs do not have a Miller clamp, they are recommended more for low-power SiC MOSFET applications. For power above tens of kilowatts, a Miller clamp is recommended as we saw in this article. To this end, a new NCD57100 and NCD57101 (pin-to-pin compatible with the NCD57000 and NCD57001, respectively) will be available with an extended gate-voltage range.

This new extended gate voltage range will be better suited to drive SiC MOSFETs. This range goes up to 36 V maximum in the new NCD571xx compared to 25 V with the NCD570xx used here in this 25-kW EV charger application.

Conclusion

The article detailed the necessary considerations in designing and tuning the gate drivers for the SiC MOSFETs in 25-kW power applications. Starting with the existing NCD57001 IGBT galvanic-isolated gate drivers, it went on to explain the improvements being made in dedicated SiC galvanic isolated gate drivers and introduced a new device family, the NCP5156x and NCD571xx, to drive the SiC MOSFETs.

SiC MOSFETs are much faster than existing Si MOSFETs and IGBTs. Therefore, the SiC MOSFET driver requires higher common-mode transient immunity and dV/dt immunity, higher current rating, and lower output impedance. Using the devices, tips and tricks mentioned in this article, designers can achieve the performance needed from SiC MOSFET drivers for their applications.

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About The Authors

Karol Rendek is an applications manager at the Systems Engineering Center at onsemi. Karol joined onsemi in 2020. Previously, he spent nine years working as hardware engineer, system engineer and project manager in development of embedded systems, Class D amplifiers, rolling stock control and safety systems and industrial electric vehicle chargers. Karol has Master's degree and Ph.D. in Microelectronics from Slovak University of Technology in Bratislava. He spent three years during his Ph.D. study focusing on low frequency noise analysis of GaN HEMT transistors.

Stefan Kosterec is an application engineer at the Systems Engineering Center onsemi. Stefan joined the company in 2013. Previously, he spent eight years at Siemens PSE as ASIC/FPGA designer where he developed digital solutions targeted for various areas, among others communications, power conversion and motor control. He spent also two years at Vacuumschmelze acting as inductive components designer and also took a role of product integrity engineer at Emerson Energy Systems responsible for verification of telecom power systems. Stefan has a master's degree in Applied informatics from the Faculty of Materials Science and Technology of Slovak Technical University Trnava.

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Didier Balocco currently serves as the business marketing engineer for Europe at onsemi. He came to onsemi through the company's acquisition of Fairchild Semiconductor, which he joined in 2014 as a field application engineer (FAE) supporting the south of France, Spain and Portugal. Previously, Didier worked at AEG Power Solutions, formerly Alcatel Converters, as a research engineer for dc-dc and ac-dc converter design in a range of 1 W to 1 kW, mainly for telecom equipment. While at this company, he also managed the research activities. Among his projects, Didier worked on a 15-kW solar inverter module for a 150-kW cabinet in Dallas, Texas, USA. His main interests during this period were switched-mode power supplies, converter stability and modeling as well as high power factor rectifiers.

Didier has published more than 10 papers on power electronics and holds one patent. He received an engineering degree from the "École Nationale Supérieure d'Électronique et de RadioÉlectricité de Bordeaux", France and a Ph. D. degree in Power Electronics from the University of Bordeaux.

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Parthiv Pandya is responsible for industrial IoT and industrial automation applications and systems product marketing at onsemi. He has over 15 years of experience in semiconductor industry working as an application engineer for Wi-Fi, Bluetooth and Ethernet PHY and switch hardware development. His background also includes programming microcontrollers-based TCP/IP and Bluetooth software stacks. Parthiv has a masters in electrical engineering and an MBA from Arizona State University.

Will Abdeh is part of the Applications Engineering team at onsemi. In this role, he's responsible for the marketing strategy of EV charging and factory automation, which involves launching new hardware platforms and driving new development opportunities. Will has launched several application-based hardware reference designs like Motor Development Kits and the Strata enabled H-Bridge Motor Driver kit. Will holds an MSE from the Ira A. Fulton Schools of Engineering at Arizona State University.

For further reading on designing EV chargers, see the How2Power Design Guide, locate the Application category and select "Automotive".