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Compendium Untangles The Complexities Of PDNs

Power Distribution Network Design Methodologies, István Novák, Faraday Press edition, an imprint of Stairway Press, Apache Junction, Ariz., ISBN 978-1-949267-67-9, glossy hardback, 402 pages, 2021.

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Experienced engineers know that the first 90% of a design project is relatively easy. This book addresses one of the topics in the last 10%, how to successfully distribute power on circuit boards. Run a few traces from the power connector to the loads and you're done, right?

István Novák, the author assembling the compendium of articles comprising this book, is an IEEE Fellow recognized for his contributions to the understanding of how to preserve waveforms in a noisy environment ("signal integrity"). This book, which has 22 chapters contributed by authors throughout the electronics industry, deals with the closely related field of power integrity. An earlier edition of this work was published in 2008. Some of the chapters here are adapted from previously presented papers.

But first there is copious material up front: a forward by Steve Sandler, to whom Novák has been a mentor; a publisher's note (from Ken Coffman, with the motto, "The Relentless Power of Reason"); a five-page preface from the author; references; an About the Executive Editor page (the author); acknowledgements and finally the book's table of contents.

Chapter 1 is from a DesignCon 2007 talk, and eases into the timely topic, "Power Supply Compensation for Capacitive Loads" with some basic feedback theory presented in a bench-oriented style. Waveforms with graticules appear, with block diagrams of test setups and measured frequency-response plots. Feedback stability conditions are described. A few very simple equations are sprinkled into the text. Compensation is lightly touched upon—hardly the full story but enough to give the flavor of what is involved.

Because the chapter is based on linear, continuous control theory, I was hoping that something about feedback amplifier output impedance, gyrating above bandwidth, would appear. As loop gain decreases with frequency, closed-loop output resistance rises, like an inductance, and can resonate within the high-frequency range between loop bandwidth and f_T (unity-gain bandwidth) with load capacitance, and often does, leaving engineers mystified as to the cause. However, that can require a long chapter in itself and chapter 1 is intended to orient the reader for chapter 2: what is wrong with resistance (dc-dc) converters.

Chapter 2 introduces converters as loads on *power distribution networks* (PDNs). While noting that feedback loop nonlinearity (such as loops having digital control) complicates design, most of the chapter involves observational comments about impedance plots, $Z(f)$, and resonances in them. Why the resonances occur is not addressed. I was hoping that instability caused by constant-power inputs of converters, and how they can present a negative incremental resistance to the power source, undamping parasitic resistance, would be discussed, but this too was a short chapter, introducing and identifying the problems from what instruments show on the bench.

Chapter 3 extols the benefits for supply bypassing of organic polymer capacitors (Cs) and their low series resistance. Capacitor structure is shown, with a table showing how the resistance of polypyrrole Cs are two decades lower than TCNQ Cs which are a decade lower than Ta (tantalum) Cs and two decades lower than aluminum (Al) electrolytic Cs.

Then one of the important topics in power distribution appears—that of wideband bypassing of a load with capacitors. Al electrolytic capacitors are notorious for high series resistance, forming a series RC branch across the supply lines. Including lead inductance, they typically reach minimum impedance around 1 MHz, then become inductive.

To maintain low bypass impedance to higher frequencies, a smaller capacitor of a different type such as a *multilayer ceramic capacitor* (MLCC) is placed in parallel. This maintains low impedance above the electrolytic resonant frequency despite the higher reactance of the smaller C at lower frequencies where the electrolytic C has low impedance. The chapter shows some Z plots of this, with a section on good capacitor combinations. Ta Cs have a history of failure without series R for current limiting (not mentioned) and appear for bypassing as polymer Ta Cs.

In the opening of chapter 3 it is stated (by author Hideki Ishida) that "a too-low ESR value capacitor sometimes causes problems." Chapter 4 continues this topic. Low series R of Cs can underdamp series resonance formed by bypass Cs and the inductance of traces of the power distribution network (PDN). Parallel resonant Zs are reduced by increasing C. *Decoupling* is apparently not distinguished from *bypassing*. For that, Laudie Doubrava of Tektronix in the 1970s made an important distinction.[1] Decoupling is what LC or RC filters do to keep PDN noise from entering sensitive circuits, while bypassing reduces voltage noise from travelling on PDNs by shorting current transients locally at the loads where they occur.

The authors of this chapter (both from TDK, an MLCC manufacturer) propose to solve the problem by adding more MLCCs. The series R is controlled by choosing MLCCs with the optimal resistance based on how they are constructed—on how many of the stacked series Cs have their electrodes brought out to the terminals. Both capacitance and case size remain the same, and two "no connect" (NC) terminals appear on the sides of the MLCCs for internal connection to the alternating connections to the internal series-C string, shown in Fig. 4.9 of the book (from page 50 and repeated below in the figure.)

By selecting the MLCC with a controlled series R, the bypassing (or decoupling) circuit (network) can have a reduced tolerance on what are otherwise parasitic resistance values—an advance in controlling what are typically wide-tolerance values.

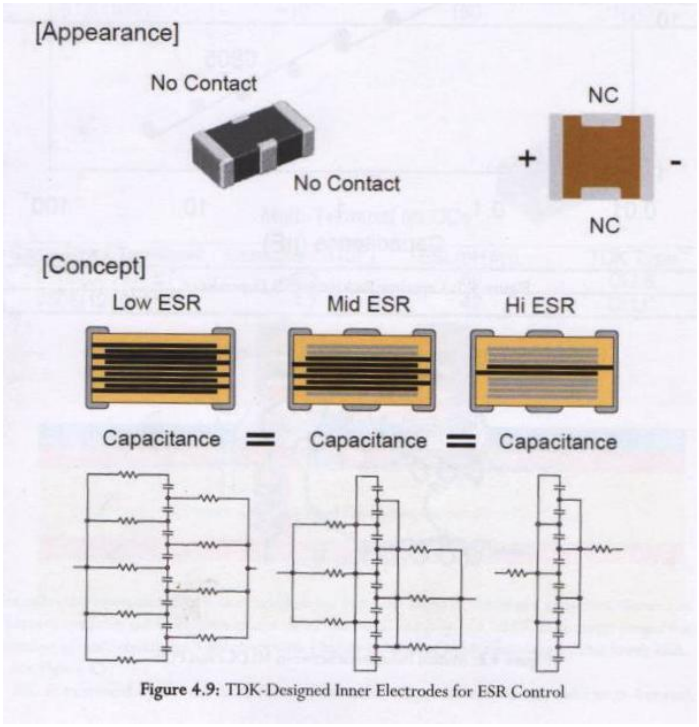

Figure. As discussed in chapter 4, for a given value of decoupling capacitance, designers of power distribution networks can select from among different MLCC constructions to achieve optimal levels of ESR.

Related to parasitic element values of Cs are both series R and L. A section in chapter 4 expounds on measurement methods, an instrumentation topic. By measuring parasitics with an impedance analyzer from Agilent (now Keysight Technologies) and probes from Cascade Microtech—spun off from Tek Labs in the 1980s by Erik Strid and Reed Gleason (who once hang-glided from the summit of Mt. Hood)—these element values allow SPICE circuit simulation.

Simulated waveforms are shown in this chapter but no acquired waveforms are presented as data for comparison. Nevertheless, parasitic values with useful tolerances provide some of the circuit model for accurate PDN circuit simulation.

Chapter 5: As K. Barry A. Williams, principal engineer at Hewlett-Packard states, "The goal of a power distribution system is to have an impedance that is flat over frequency." PDN modeling follows, and then load characterization, with a load current of 20-A amplitude and 938-ps pulse width, to frame the speed at which computer-board PDNs must operate nowadays. A few simple resonance equations appear to calculate *Z*, and

using *Q* from communications theory. Multiple stages of bypass circuits result in multiple resonances, spatially distributed on the circuit-board. Design is summarized by some Z plots and some judicious choices of bypassing components—an art more than analytically-optimized engineering.

Chapter 6 shifts gears and becomes oriented to converter control circuits for VRMs—voltage regulation modules, voltage regulators placed near the load. Pentium II µP power specifications are tabulated; 2.8 V ±0.1 V for the µP core, and at 300 MHz, 14.2 A. This takes us into the territory of low-resistance converter design;

$$R_{out} = 2.8\ \text{V}/14.2\ \text{A} = 20\ \text{m}\Omega$$

The load can change at up to 30 A/µs and the voltage must remain in tolerance. Optimal load transient response rules out voltage control of common-passive (buck) converters because of lack of direct control of inductor current. Another reviewed ("V^2") control scheme combines constant-off-time current control with feedback of the output capacitor current, but this also falls short in performance. The proposed scheme reverts back to current control (specifically, constant-off-time peak current control) and "suitable compensation of the voltage-error amplifier" (p. 86).

The rest of the chapter contains some *s*-domain equations (not derived in the text) and an example design. Simulated and measured results are compared. The emphasis in the design is on choosing a control scheme (and power-transfer circuit) that will achieve the right Z_{out}.

In the subsequent chapters, additional topics involve more on bypass capacitors and filters, voltage positioning, PDN design strategies, and particular power-system analysis, for DDR2 RAMs, Gbit I/O interfaces, FPGA serDes jitter performance, and circuit-board power planes. The last chapter, 22, concludes with a transmission-line model of MLCCs.

Chapter 17 emphasizes capacitor types for bypassing, and includes the use of Ta capacitors. No mention is made of the failure mode in solid electrolyte Ta Cs with transient overcurrent. My experience with these parts left a lasting impression.

Decades ago, at Tektronix, the FG502 function generator made liberal use of Ta bypass Cs. I was in TM500 final test and calibration, powering on FG502s for the first time. About 20% of them had power bus shorts traced to shorted Ta capacitors. I remember replacing large numbers of them. Since then, I have avoided using Ta Cs.

Tek component engineering issued a "Component News" description of the failure mode, with the sentence: "To assist the self-healing process [of the dielectric recovering from point shorts], manufacturers specify a [0].3 A surge-current limit, which is equivalent to 3 ohms/volt circuit impedance." Vishay-Sprague authors[2] express these limitations as power dissipation limits. Overrating the voltage can alleviate failure, but the mechanism still exists.

In this review, I have expressed here and there what is missing from the book, but this should not detract from its value. The topic cannot be covered exhaustively in one book, though the author and publisher have made a good attempt to include the major concepts and should be applauded for compiling an entire book on what is too easily regarded as a trivial topic amidst the maelstrom of more obvious project design considerations. More books on the problems of the final 10% of electronic design of a product would enhance the literature, and this book contributes to that end.

References

1. *High-Performance Amplifiers*, Dennis Feucht, Innovatia.com, p. 115.
2. "AC Ripple Current of Solid Tantalum Capacitors" by Dave Toomey and Jean Racine, *PCIM*, June 1995, pp. 37 - 43.

About The Author

Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

To read Dennis' reviews of other texts on power supply design, magnetics design and related topics, see How2Power's Power Electronics Book Reviews.