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Why EM Is Replacing SPICE For Simulation Of Board-Level Power Delivery

by Heidi Barnes, Keysight Technologies, Santa Rosa, Calif. and Steve Sandler, Picotest, Phoenix, Ariz.

There is nothing magical about power delivery for high-speed digital loads. It follows the laws of physics and travels in waves according to Maxwell's equations. Now, if you have ever tried to solve Maxwell's equations by hand, you will completely understand why electronics engineers spend so much time with lumped-element circuit theory.

Lumped-element circuit theory makes use of the much simpler Ohm's law and Kirchoff's laws for nodal analysis and is the basis for SPICE-based simulators. The question that is left unanswered is "When do the assumptions that the circuit is the lumped equivalent of a schematic break down and drive the need to include a higher fidelity electromagnetic (EM) model of the physical interconnects between the components in a schematic?"

In the power electronics world of voltage regulators there is such an entrenched history of SPICE models that few engineers look further than running a freeware LTspice simulation with vendor-supplied models to predict behavior. This "lumped-SPICE" type simulation assumes perfect conductors connecting between the bill-of-material components in the schematic.

However, signal integrity engineers designing power delivery to high-speed digital loads are finding out the hard way that lumped-SPICE simulations are leaving out critical time delays and parasitic behaviors that only an EM simulated model of the printed circuit board (PCB) interconnect can get right. Getting it wrong can result in incorrect prediction of power rail resonances and lead to voltage regulator designs that are on the edge of instability. Ultimately, it can lead to a complete failure of the high-speed circuitry.

In this article, we will discuss and demonstrate the differences in simulation results obtained with lumped-SPICE modeling of circuits lacking PCB parasitics versus simulation results obtained with EM modeling that includes the board effects. We'll illustrate these differences through simulations of voltage regulator output impedance and capacitor network impedance, noting the implications of the discrepancies.

Hopefully, these examples will drive home the need for EM modeling of both the voltage regulator and the power distribution networks (PDNs) in which they are used. However, in the last section we'll explore how the lack of clarity surrounding vendor-supplied models of decoupling capacitors presents a barrier to accurate power delivery simulations with EM models.

Simulating Voltage Regulators

For example, as regulators increase in switching frequency and deliver power to low-impedance PCB power distribution networks, their internal parasitics start to be comparable to those of the printed circuit board. Fig. 1 shows the capacitive output load impedance magnitude and phase of a switching regulator in the off state simulated in lumped SPICE without the PCB parasitics (blue trace), and then simulated again with the EM model of the PCB included (red trace).

The lumped-SPICE simulated ESL of the power delivery path is lower by a factor of 25 and completely underestimates the decoupling capacitor requirements to satisfy the load at higher frequencies. A closer look at the phase plot shows that the inaccuracies of the lumped-SPICE simulation also extend to the lower frequencies by eating away at the stability margins for the voltage regulator control loop.

Fig. 1 shows that the SPICE simulated phase can be off by as much as 6 degrees at frequencies as low as 100 kHz. This error can be a significant portion of a typical design requirement for better than 30 degrees worst-case phase margin. This is a good example of how PCB parasitics matter at frequencies even as low as 100 kHz.

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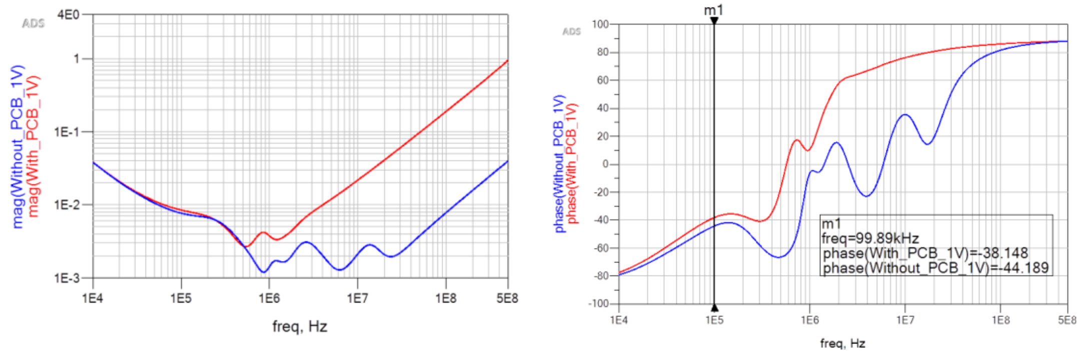

Fig. 1. Comparison of the switching regulator off-state output impedance vs. frequency for a lumped-SPICE simulation (blue) vs. simulation including a full 3D EM model of the PCB interconnect parasitics (red). The plot on the left is impedance magnitude and the plot on the right is phase. The lumped-SPICE simulation and the simulation with the PCB EM model were carried out in Keysight's PathWave ADS EDA tool.

Simulating Decoupling Capacitors

Power delivery for a high-speed digital load extends way beyond the kilohertz bandwidth of the typical voltage regulator. At these higher frequencies, the decoupling capacitors become the source of power and if not selected correctly can easily lead to high-impedance resonances. A very simple experiment of five parallel capacitors shows just how wrong a lumped-SPICE simulation can be when PCB parasitics of the path are ignored. Fig. 2 shows a small connectorized PCB that was used for this experiment. The board was both measured and simulated to show the impact of the PCB parasitics on the impedance of five parallel capacitors.

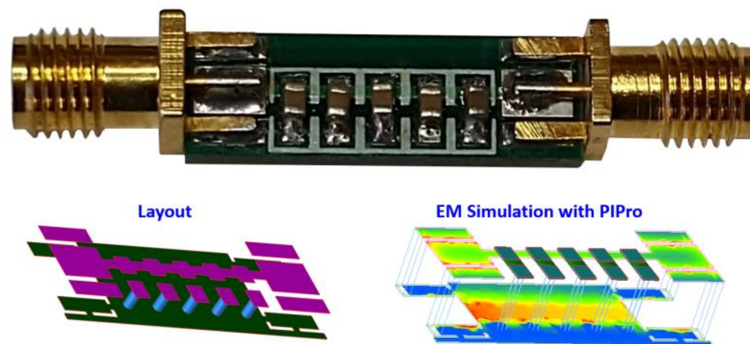

Fig. 2. Simple experiment of five decoupling capacitors in parallel to show how lumped SPICE gets it wrong when calculating the PDN impedance. A test board is shown here (top image) along with a corresponding layout drawing (lower left) and an EM simulation of the test board (lower right) produced in Keysight's PIPro 3D EM tool for Power Integrity.

In the first experiment, all five capacitors have the same value. The impedance of these capacitors was simulated using a lumped-SPICE model and a distributed-EM model. The results presented in Fig. 3 show just how wrong lumped SPICE can be for low-impedance power delivery networks that are trying to extend power delivery to tens of megahertz. The lumped-SPICE model calculates 5x the capacitance (of the single capacitor value), one-fifth the ESR, and one-fifth the ESL and is shown as the large dashed black trace in Fig. 3.

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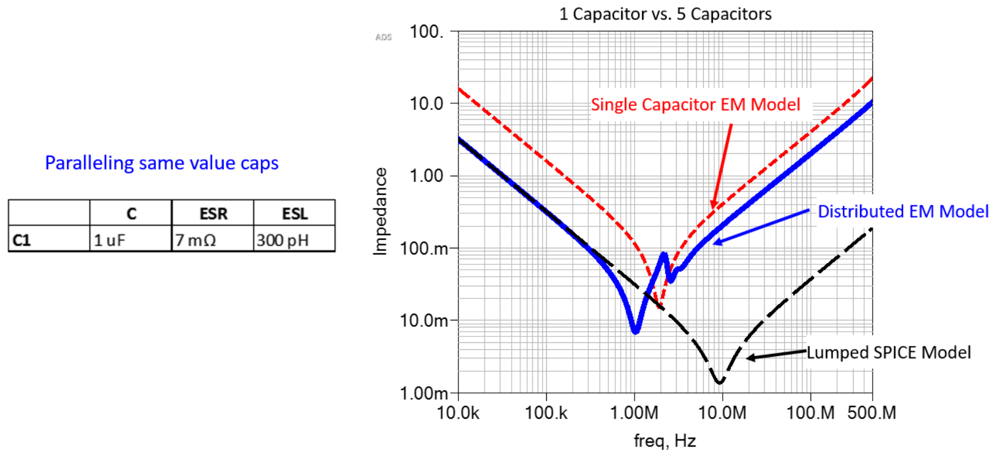
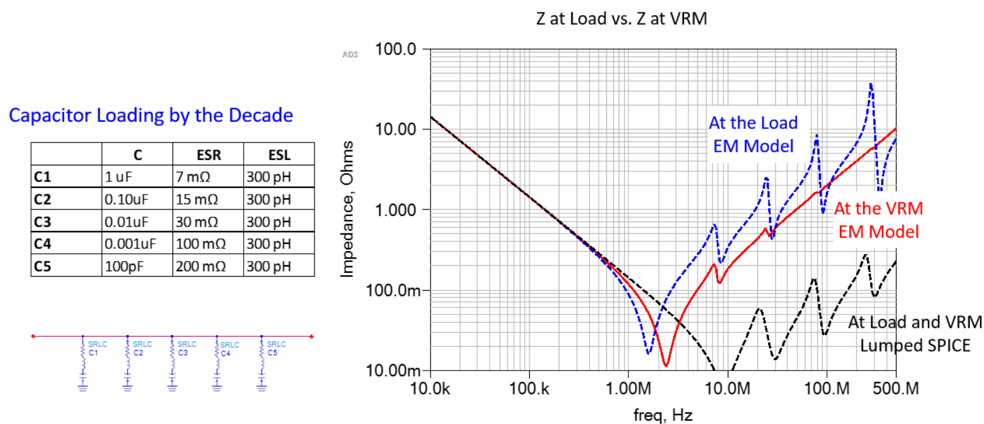


	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH

Fig. 3. Impedance of five parallel capacitors simulated with lumped SPICE (black dashed trace) vs. their impedance simulated with the PCB EM model (blue solid trace). The single capacitor impedance is included as a reference (red dashed trace) to show that one-fifth the ESL calculated by lumped SPICE is underestimating the true path inductance, while EM simulators obtain the correct distributed path inductance.

The simulated result that includes the PCB EM model also shows the expected 5x capacitance, but that is where the similarity with the lumped-SPICE model ends. Simulation and measurement confirm that the ESR and the ESL are significantly higher when the PCB parasitics are included. This results in impedances that can be orders of magnitude off at the higher frequencies for the lumped-SPICE model.

Using this same PCB example, a second experiment with five different capacitor values shows how a lumped-SPICE model fails to predict the location-dependent behavior of the PDN impedance. If path-dependent parasitics between the five different capacitors are not included, then the lumped-SPICE model gives the same impedance at each end of the PCB. However, both in measurement and in simulation it can be shown that there is a significant difference in impedance seen when measuring at the bulk capacitors next to the VRM vs. at the load next to the smaller decoupling capacitors (Fig. 4).



	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH
C2	0.10uF	15 mΩ	300 pH
C3	0.01uF	30 mΩ	300 pH
C4	0.001uF	100 mΩ	300 pH
C5	100pF	200 mΩ	300 pH

Fig. 4. Impedance vs. frequency for five different values of capacitors in parallel. Again, the lumped-SPICE data (black dashed curve) underestimates the inductance, and incorrectly assumes the same impedance at each end of the network. Simulation with a PCB EM model in ADS correctly predicts the parasitics and shows a large difference in resonances at the load (blue) vs. the VRM (red).

This clearly shows that when measuring a power rail, it matters where it is measured. The impedance will depend on the measurement location.

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If you are still in doubt, just look at a traditional transient simulation shown in Fig. 5 of the voltage ripple at the voltage regulator module (VRM) vs. at the load when the PCB EM model is included. The regulator's large-signal switching ripple is filtered by the PDN path transfer impedance. This results in a smaller peak-to-peak magnitude in regulator switching noise at the load.

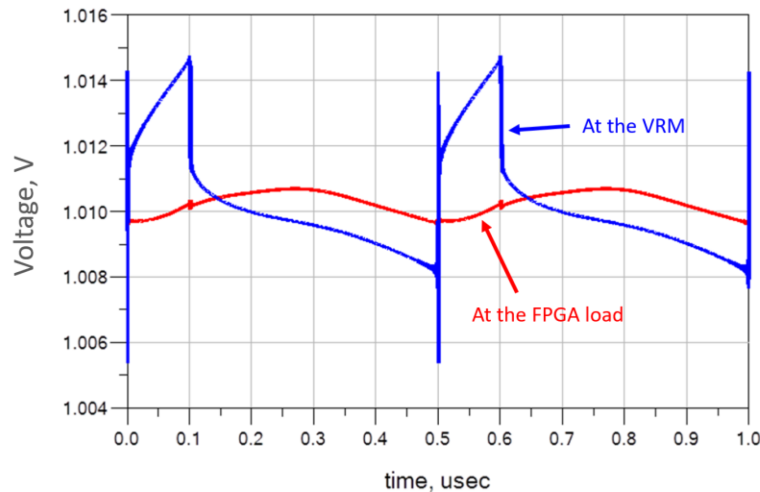

Fig. 5. Voltage ripple on a 1-V power rail measured at the VRM in blue and at the FPGA load in red. Power rail ripple depends on the measurement location. (Data provided by AEi Systems.)

Poorly Defined Capacitor Models

These few examples above show the importance of including the PCB EM model when doing power integrity simulations. Luckily the cost of EM simulators continues to decrease when one considers the significant increase in simulation speed and improvements in net-based automation of the simulation setups.

However, there is one challenge that the industry faces in the rush to demand EM model accuracy. How accurate are the capacitor models that attach to the PCB EM model, and does the model indicate if the mounting inductance is included?

To explore the significance of the mounting inductance an example *islands PCB* compares the difference in mounting inductance for a capacitor return path with 2 ground vias vs. one with 12 ground vias, as shown in Fig. 6. The board is constructed with two different PCB stack-ups to see how the mounting inductance changes when the power-to-ground layer distance decreases from 63 mils to 8 mils.

The results in Fig. 7 show that the additional ground vias do reduce the mounting inductance but reducing the distance between the power and ground layers has a bigger impact. The 63-mil board with 1 via has 620 pH of inductance and even with 12 ground vias added it only drops to 450 pH. Reducing the dielectric thickness between power and ground to 8 mils drops the inductance to 425 pH.

Obviously, the EM model shows that the capacitor footprint and PCB construction can have a significant impact on the mounting inductance of the capacitor. If this is the case, then how can one use the same capacitor model in a lumped-SPICE simulation as that used when connecting to an EM model of the PCB PDN? Did the vendor model of the capacitor remove all the mounting inductance? Or will it be double counted when attaching to an EM model of the PCB PDN?

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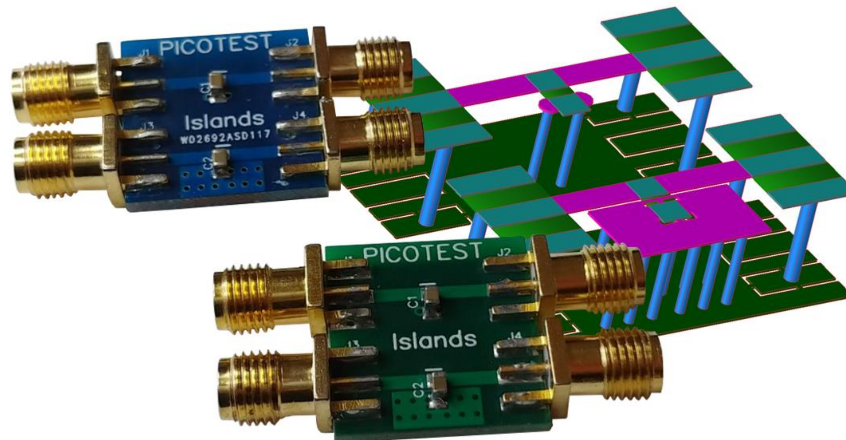

Fig. 6. Capacitor mounting experiment to demonstrate the impact of mounting parasitics and the need for separating internal capacitor parasitics from the mounting parasitics when connecting to a PCB EM model that already includes the mounting parasitics. The PCB at the top left has 63 mils between power and ground while the PCB at the lower right has only 8 mils. Both boards have a capacitor with two vias to ground and a capacitor with 12 vias to ground as shown in the PathWave ADS PIPro model of the PCB.

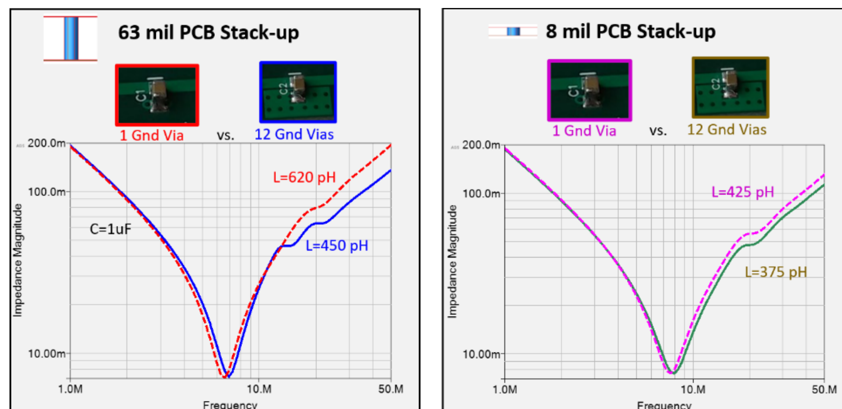

Fig. 7. The design of the PCB stack-up and the PCB footprint have a significant impact on the mounting inductance of a capacitor. Adding additional ground vias helps reduce the mounting inductance of the capacitor (plot on the left), but the larger drop in mounting inductance happens when a thinner 8-mil dielectric instead of 63 mils is used between the power and ground (plot on the right).

The best way to ensure the accuracy of the PI simulation with an EM model is to verify the capacitor models with measurement. Mounting inductance can easily be measured or simulated by shorting the pads of the capacitor's PCB footprint together to determine the impedance including loop inductance of the mount. This impedance in the form of an S-parameter can then be de-embedded from the measurement of the capacitor with the mount.

Fig. 8 shows how this simple definition of the mounting inductance by shorting the capacitor pads results in a much more repeatable model. Three 0805 1-µF capacitor vendor models were selected, and according to the data sheets the worst one had more than double the inductance. However, after measuring the capacitors and removing the mounting inductance of the fixture it was discovered that all the capacitors had a similar internal parasitic inductance due to the 0805 package size. Ironically the capacitor with the highest inductance according to the data sheets had the lowest internal parasitic inductance.

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3 Different 0805 1uF/25V Capacitors

Vendor Data for Inductance:

- 709 pH **08053C105JAT2A**
- 400 pH for the **GCJ21BR71W105KA12L**
- 340 pH for the **GRM216R61E105KA12D**

Vendor data has wildly different inductance values, while the measured data shows that the 0805 package is consistent with ~155 pH.

Measured Data with Mounting Inductance Removed:

AVX 08053C10...	Murata GCJ21...	GRM216R61E10...
140.119 pH	148.087 pH	174.123 pH

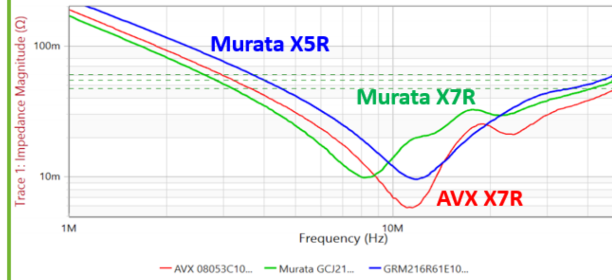

Fig. 8. Capacitor data (inductance) supplied by the two vendors compared to capacitor measured data with the mounting inductance removed. All capacitors are 1 µF in an 0805 package, and as expected the measured data with mounting inductance removed shows similar internal parasitic inductance. Sadly, the vendor data is significantly higher in inductance with large variations in value.

Conclusion

In this article, we've examined just a few of the things that lumped SPICE gets wrong and why it's worth spending the time to run the PCB 3D-EM simulation to get it right for power delivery to a high-speed digital load. Even at frequencies as low as 100 kHz the parasitic inductances can significantly impact the output impedance at the VRM. This can lead to underestimating the amount of bulk capacitance required, and lead to decreased phase margins for regulator stability.

At higher frequencies, the power delivery is provided by the decoupling capacitors and here again, lumped SPICE gets it wrong. The simple experiments with five parallel capacitors of the same value and of different values clearly show the importance of including an EM model of the distributed nature to account for PCB parasitics. The inductance is not a simple one-fifth the single capacitor value when paralleling same-value capacitors, and measurements of either impedance or voltage ripple at the VRM are not the same as measurements at the load.

Finally, the industry does a disservice by supplying capacitor models that do not specify whether the mounting inductance is included or removed. Clearly EM models can add significant fidelity to the EM simulation, but only if the capacitor model fidelity is also improved by ensuring that the mounting inductance is not double counted.

The future demand for increased digital bandwidth with multi-level signaling, coupled with higher currents and lower voltages to meet low power requirements will only make it harder for lumped-SPICE simulations to keep up. Only with end-to-end VRM + PCB + load simulations that include 3D-EM models of the PCB parasitics will simulation be able to accurately predict power delivery performance for this new generation of designs.

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About the Authors

Heidi Barnes is a senior application engineer and Power Integrity Product Owner for High Speed Digital applications in the Design Engineering Software Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and channel simulators to solve signal and power integrity challenges. Heidi is the author of over 20 papers on SI and PI, active member in developing the new IEEE P370 Standard involving interconnect S-parameter quality after fixture removal, and recipient of the DesignCon 2017 Engineer of the Year.

Prior experience includes seven years in signal integrity for ATE test fixtures for Verigy, an Advantest Group, eight years in RF/Microwave microcircuit packaging for Agilent Technologies, 10 years with NASA in the aerospace industry, and one year with Arco Solar in the solar cell industry. She has been with Keysight EDA software since 2012. Heidi holds five patents, and was awarded the NASA Silver Snoopy for her work on hydrogen fire and gas detection. Heidi holds a bachelor’s degree in electrical engineering from California Institute of Technology.

Steven Sandler is the managing director of Picotest, a company specializing in precision test and measurement equipment. Sandler is also the founder and chief engineer of AEi Systems, where he leads development of high-fidelity simulation models for all types of simulators as well as the design and analysis of both power and RF systems.

Sandler has over 30 years of experience in engineering and is a recognized author, educator and entrepreneur in the areas of power, RF and instrumentation. His book, “Power Integrity: Measuring, Optimizing and Troubleshooting Power Related Parameters in Electronics Systems,” was published by McGraw-Hill Education.

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