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Ruggedizing Buck Converters For Space And Other High Radiation Environments

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Space missions, riding on a wave of exciting new government and private initiatives, are multiplying and capturing the imagination of entrepreneurs as well as the public at large (Fig. 1). Every space device, from a spacesuit to a satellite, is a complex system not unlike other modern electronic appliances, needing microprocessors for computing power, sensors, energy to operate, energy storage to function untethered, and power management to minimize energy waste and extend operation on battery. However, in contrast with common electronics, space devices operate in a uniquely unforgiving environment, exposed to high radiation bombardment, which if not neutralized or mitigated, interferes with the electronics down to the level of a single transistor, causing disruption or even catastrophic failure.

Although space and commercial systems have a lot of electronics in common, space technology cannot draw directly from the wealth of electronics produced with great economies of scale by the commercial industry. Any off-the-shelf component utilized in a space application will likely degrade and fail prematurely once exposed to the severity of the space environment, endangering the mission. But not all is lost, as a wealth of ruggedization techniques are able to meet the challenges of this unforgiving environment.

In this article, we review first the effect of radiation on passive and active electronic components and the technologies, processes and device techniques that make them radiation-tolerant or radiation-hard. Subsequently we discuss Alphacore's design of a radiation-hardened dc-dc converter at the heart of a space power management and distribution system. Able to properly function at up to 200 Mrad of TID, the converter can operate within the large hadron collider at CERN, and in space satellite and probe missions.

Fig. 1. Space electronic equipment, including that worn by astronauts, is continuously exposed to high levels of radiation.

Weak Points Of CMOS Microelectronics

In semiconductor circuits, the weak points are known to be the bipolar parasitic transistors formed between the various CMOS p- and n-diffusions: the CMOS cross section in Fig. 2 shows two such parasitic transistors (npn and pnp in brown) forming a silicon-controlled rectifier (SCR).

These parasitics, normally dormant, can be excited or turned-on by stray charge injections. In commercial electronics this happens when driving inductive loads, whose kick may force an n-doped region below ground, hence turning on a parasitic npn between that n region, the p substrate, and a contiguous n region. This type of "attack" coming from the ground is well understood and is fought with processes like silicon-on-insulator (SOI), which eliminates the p substrate, and if that is not an option, with "moats" that surround the exposed diffusion in contact with the inductor, and collect the injected charges, dumping them directly to the positive node (V_{dd}).

In space applications in addition to such ground attacks we have aerial attacks. Here the parasitic injection is caused by high-energy particles coming from deep space and penetrating the silicon with the same destabilizing or destructive effects.

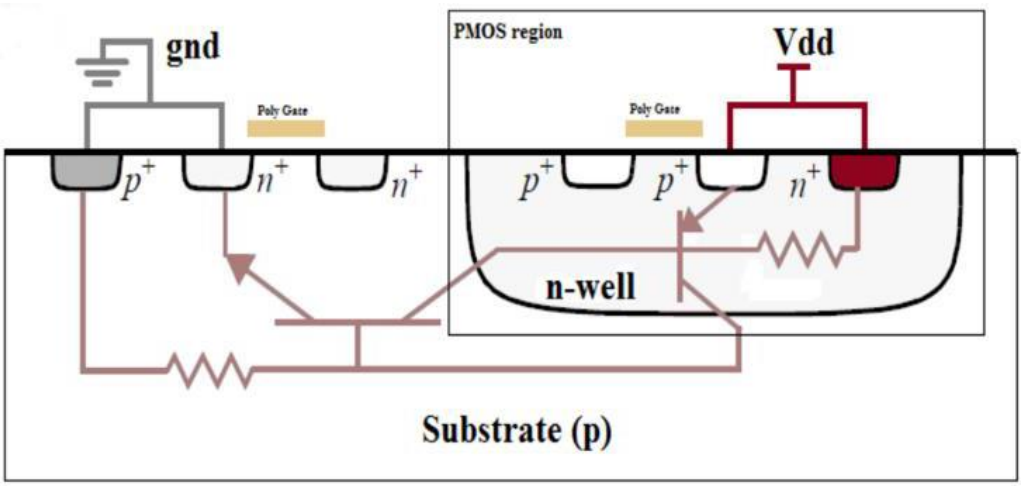

Fig. 2. Parasitic bipolar transistors in a CMOS process.

Radiation Effects On Electronics

When gamma rays or X-rays hit the silicon, the electrons in the valence band get enough excitation to enter the conduction band. This ionization process causes energy to be trapped in the materials and is called "total ionizing dose (TID)," measured in "rads" or "Grays". This energy generates electron-hole pairs in the particles' path.

In the oxide most of the generated electron-hole pairs remain trapped, causing threshold voltage shifts.
When a heavy ion hits an electronic device (Fig. 3) and passes through a sensitive node, it can generate a transient voltage pulse at that node inducing state changes in the logic. This is called a single-event transient (SET). When the ion hits a pnpn structure (the parasitic SCR in Fig. 2) it can induce a latch-up. This is called a single-event latch-up (SEL). Both events are referred to as single-event effects (SEEs).

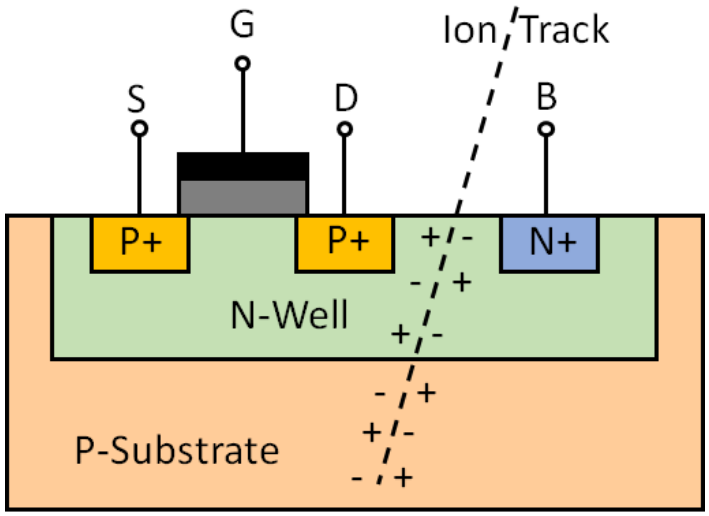

Fig. 3. Ionizing path in a PMOS transistor hit by an ion.

Radiation Hardened Processes

Compared to traditional bulk silicon technologies, a CMOS SOI process reduces the radiation-sensitive volume by isolating the entire device from the bulk substrate with the help of the buried oxide layer (Fig. 4). This makes SOI highly resistant to SEEs while remaining sensitive to TID, as charge induced by gamma rays or X-rays gets trapped in the buried oxide, creating a shift of the threshold voltage in MOS structures. Fortunately, circuit and layout techniques can be utilized to achieve radiation hardness to SEE and TID.

Gallium nitride (GaN) is used to form high electron-mobility transistors with a low temperature coefficient and a lateral structure, offering very low $R_{DS(ON)}$ and lower total gate charge than silicon MOSFETs. This makes them very attractive for use in high-power, high-frequency switching applications. GaN has also demonstrated low susceptibility and inherent robustness to radiation-induced material and performance degradation and is emerging as a workhorse in the space electronics industry.

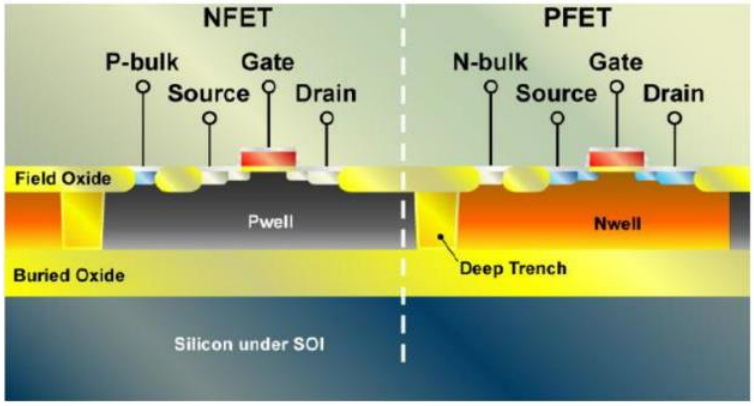

Fig. 4. SOI process cross section.

Circuit And Layout Techniques

Annular Gate Transistor

In submicron processes, the shallow trench isolation (STI) contiguous to drain and source of a CMOS transistor, thicker than the gate oxide, collects charges under TID, which can invert the active area abutting the STI, causing a leakage current from source to drain. An annular gate transistor, or enclosed-layout transistor (ELT), is one of the most effective ways to mitigate this TID-induced leakage.

Fig. 5 shows the schematic and layout of an NMOS ELT transistor in a 180-nm process. The drain is entirely enclosed by the gate, and the source is at the other side of the annular gate, thereby eliminating contiguity to the STI. The whole transistor is further enclosed by its body connection, to increase the robustness to SEEs, such as SELs caused by heavy ions or neutrons.

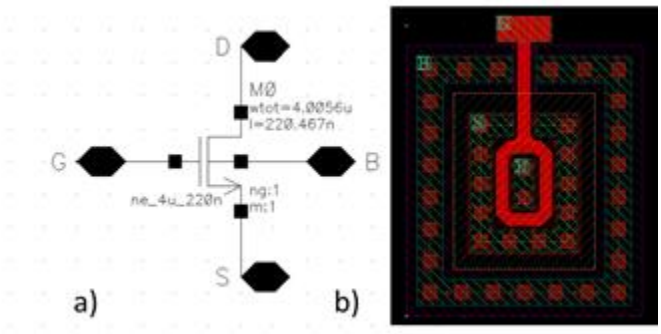

Fig. 5. Schematic (a) and layout (b) of an ELT transistor.

Superjunction Transistor

The high-voltage superjunction double-diffused MOS, or SJDMOS, transistor (Fig. 6) is critical for power management applications. Compared with conventional lateral diffused MOS (LDMOS), where the high breakdown voltage is completely supported by a lightly diffused drain channel with a single type of material, the superjunction DMOS uses lightly diffused p-type and n-type channels next to each other. This structure gives a higher breakdown voltage for a given lateral channel length, along with better radiation tolerance, especially SEE robustness.

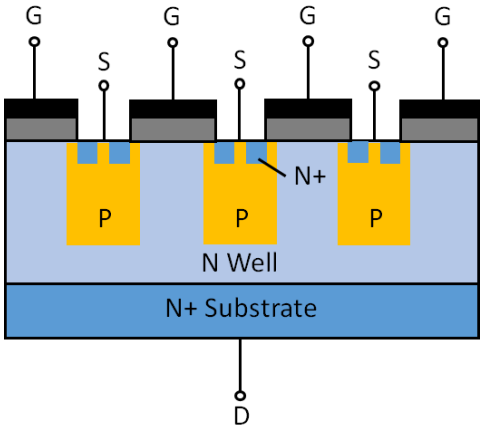

Fig. 6. Cross section of a superjunction DMOS transistor.

ELT/SJDMOS Cascode Structure

SJDMOS transistors make excellent power drivers; however, with their 5-V gate drive, they are prone to TID-induced leakage. To address this problem, a low-voltage enclosed-layout transistor (ELT) cascoded with the SJDMOS (Fig. 7) will block the leakage path.

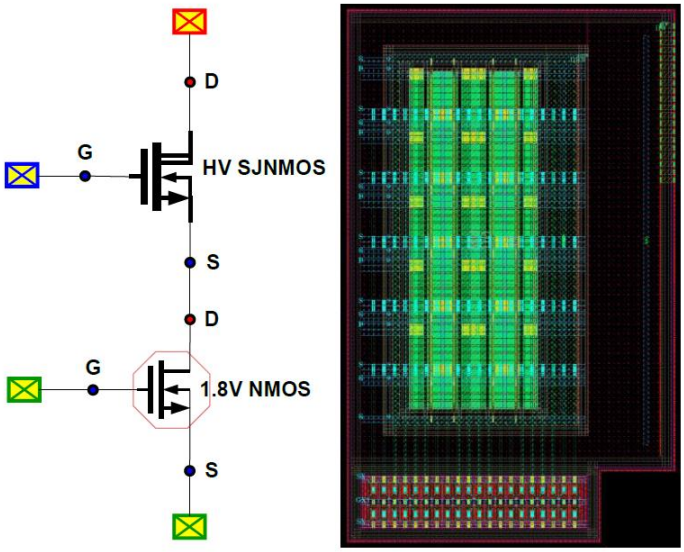

Fig. 7. Circuit schematic and layout of an ELT/SJDMOS cascode.

Even if the TID effect changes the threshold voltage of SJDMOS, it does not significantly degrade the switching mode operation of the power stage. Hence the cascode structure protects from the TID leakage of the power

stage even if the TID changes the electrical parameters of the individual SJDMOS device. Combining the improved SEE rad-hard performance of SJ devices and TID-robust ELT devices, the cascode structure has both improved radiation tolerance performance and high breakdown voltage.

Bandgap Reference For Space Applications

The diode p-n junction is the basis of any bandgap voltage reference (BGR). In conventional CMOS BGRs, the p diffusion is surrounded by an STI (shallow trench isolation as previously noted) field oxide layer, which tends to trap irradiation-induced holes.

However, if we surround the source of a PMOS with an annular gate we can isolate it from the STI. In this structure the drain and n-well are grounded and the diode is formed at the junction between the source and the n-well diffusions (Fig. 8). Such a layout is implemented in a device called a dynamic-threshold MOS transistor (DTMOST), a radiation-hardened diode with a V_{be} of about 0.1 V versus the 0.6 V of the conventional diode.

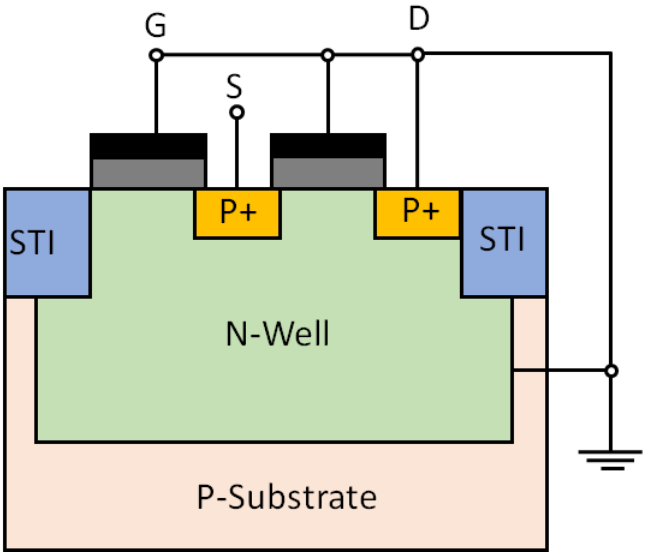

Fig. 8. Cross section of a DTMOS transistor.

Inductors For High Magnetic Field Applications

Although not relevant to space applications, in high energy physics experiments, such as the Large Hadron Collider (LHC), in addition to dealing with radiation, components must also withstand the effects of strong magnetic fields. This requirement precludes the use of ferromagnetic-core-based inductors, since in the presence of high flux the magnetic core saturates and the inductance collapses. In contrast, air-core inductors are free from saturation and core loss and are linear vs. current, exhibiting higher Q and lower distortion.

Nevertheless, their superior electrical performance comes at the cost of a larger size compared to core-based inductors. While planar, solenoidal and toroid coreless inductors are available, the toroid is preferred for its ability to contain the flux inside its enclosed volume, minimizing disturbances due to its magnetic emissions.

A Rad-Hard Buck Converter Architecture

The process and circuit techniques described in the preceding sections lay the groundwork for development of a power supply controller and driver IC that can be applied in a rad hard dc-dc converter. Alphacore develops such ICs, enabling critical systems for research, aerospace, defense, medical imaging, and homeland security.

As an example, Fig. 9 shows a 10-A, 8-V to 18-V input, 1-V to 1.5-V output dc-dc converter comprising a GaN power stage IC and a CMOS SOI controller/driver IC with high-voltage superjunction transistors for the driver

section. Capable of robust operation up to 200 Mrad of TID, the converter can operate within the large hadron collider at CERN as well as in space vehicle missions.

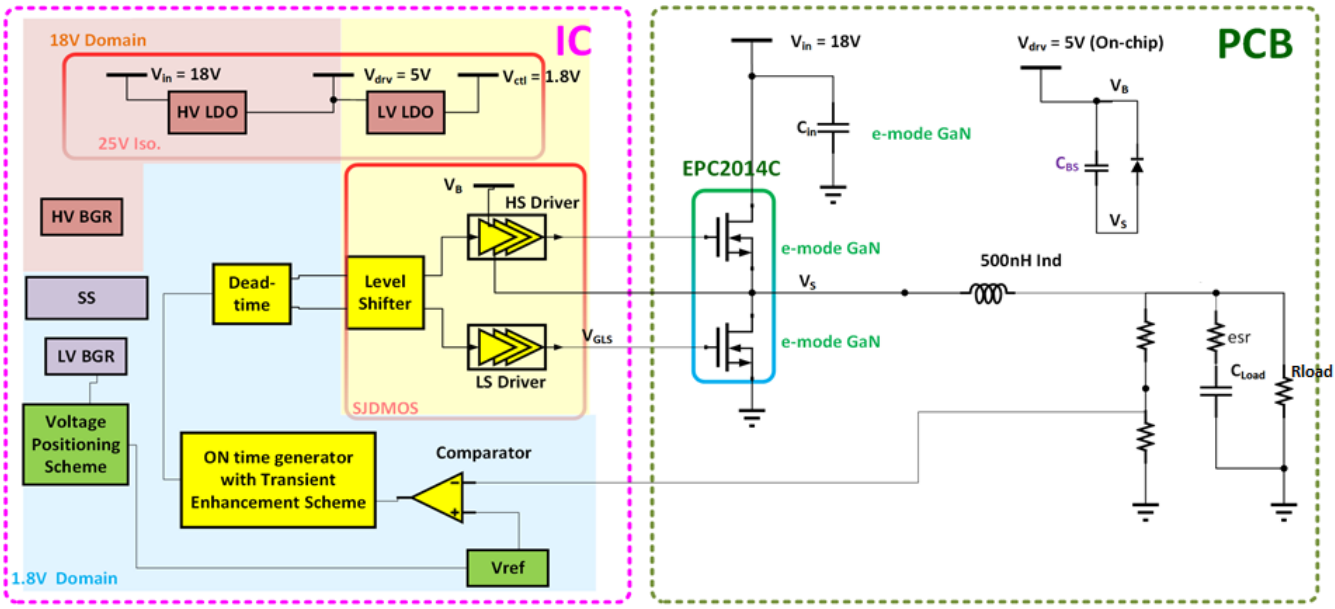

Fig. 9. Block diagram of a radiation-hardened buck converter leveraging the process and circuit techniques discussed in this article to operate with a TID of 200 Mrad.

The hybrid 180-nm CMOS SOI/GaN architecture enables operation with high load current and a switching frequency up to 1 MHz. The use of a constant-on-time (COT) topology assures wide dynamic input range, as a higher conversion ratio is achieved by a small on-time and by the use of GaN power devices that exhibit low parasitic gate capacitance. The controller circuit uses internal ripple generation which reduces reliance on the equivalent series resistance (ESR) of the output cap for loop stability and facilitates ripple reduction at the output.

The COT topology has additional advantages such as a single control loop, minimum number of off-chip components, fast transient response, good noise margin, better line and load transients, and high stability. The GaN power switches enable very high efficiency with a smaller output LC filter. Superjunction devices with their high drain-source blocking voltage, simplify the complex driver design and enable high-frequency operation. Finally, the air core inductor enables operation in a radiation-prone environment that also has a high magnetic field.

Conclusions

The design of electronic components for the space industry poses unique challenges. Such devices are subjected to a harsh environment, particularly their exposure to high radiation bombardment from space. Similarly, other applications such as particle accelerators expose equipment to high radiation levels. Standard commercial electronic circuits and processes fail in these environments.

In this article, we reviewed the main challenges coming from these environments and the means of neutralizing them by ruggedizing existing processes and components using established methods. The application of these processes and techniques was exemplified with the design of a 10-A, 8-V to 18-V input, 1-V to 1.5-V output dc-dc converter comprised of a GaN power stage IC and a CMOS SOI controller/driver IC with high-voltage superjunction transistors for the driver section.

About The Author

Nazzareno (Reno) Rossetti is an analog and power management expert at Alphacore where he helps deliver innovative analog, mixed-signal, and power-management solutions for radiation-tolerant applications. He is a published author and holds several patents in the field. Reno has a doctorate in electrical engineering from Politecnico di Torino, Italy. He can be reached at Reno.rossetti@alphacoreinc.com.

For more on rad hard power components and power converters, see How2Power's special section on Space Power.