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Improving Solar Inverter Reliability: Techniques For Protecting Output Power Switches

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Ac power inverter reliability is a concern in a variety of fields ranging from utility to industrial power systems. However, this article focuses on another inverter application area—inverters used in off-grid and grid-tied, photovoltaic systems for residential rather than commercial use. The power range for such inverters ranges from several hundred watts to about 20 kW. These products are commonly referred to as solar inverters.

Much of what has been published on the subject of inverter reliability relates to the testing performed to establish inverter reliability. Because of the concern over failure rates, there have also been efforts to make inverter failure predictable. For example, an innovative method of predictive monitoring of inverters, albeit primarily industrial and utility inverters, is being pioneered by InfiniRel to provide a more efficient method of managing inverter reliability. This technology has the potential to benefit any class of inverters. But such methods only manage or mitigate problems with inverter reliability, rather than actually improving the actual reliability of the inverter design.

As far as addressing the reliability of the inverter design, most of what's been discussed in the literature has involved such things as electrolytic capacitors. Very little has been written regarding the most stressed devices in the inverter—that is, the output power switches and associated circuitry. Inverter output switch design is a key area that needs attention to achieve improvements in inverter failure rates.

Another consideration in inverter reliability is the choice of transformer-based or transformerless design. The transformerless inverters (commonly referred to as "high frequency" inverters) have a failure mode that can damage loads with dc outputs, whereas inverters with transformer output (commonly referred to as "low frequency" inverters) prove more robust and safer in many regards.

This article begins by discussing the key differences between inverters with transformer outputs and those that are transformerless. After briefly reviewing the vulnerability of the power MOSFETs used as power switches in inverters, the article discusses the benefits of foldback current limiting techniques in protecting the MOSFETs. These techniques have been around a long time, but have not typically been implemented in solar inverter designs. The article then explores the greater stress that's placed on the power MOSFETs in transformerless inverters.

The next sections discuss the improvements made possible in MOSFET protection by TI's UCC5870 isolated MOSFET driver, and some of the limitations designers face in implementing the chip's full set of MOSFET protection features. Finally, a drawback of the inverter with transformerless output—its ability to deliver high levels of dc in certain failure modes—is explained along with a circuit solution to guard against this problem.

Inverter Reliability And Current Designs

There is a major division in inverter technology between transformer and transformerless inverter designs. An initial comparison of the advantages of each architecture is provided in the table.

A basic block diagram of an inverter power stage is shown in Fig. 1. The full-bridge output stage is a universal configuration that may or may not be used with a transformer. Both versions are depicted in the figure.

In the jargon of the solar world they often refer to low-frequency and high-frequency inverters, which is a woefully inadequate nomenclature, especially when you consider "modified sine wave" and "sine wave" inverters. However, high-frequency" inverter terminology has come to be associated with transformerless inverters. The high-voltage internal power supply of a transformerless inverter is generated by *high frequency* dc-dc converters (typically multiple converters).

Table. Comparing advantages of transformer-based versus transformerless inverters.

Transformer output	Transformerless
Safety (If an output device fails, the inverter cannot output dc to the ac power line)	Cost
Ruggedness	Efficiency
Isolation	Weight
Excellent surge capability	--
Low switch voltage has an SOA advantage (avoids second breakdown regions)	--

Transformer-inverter output stages run directly from the battery and are referred to as *low frequency* despite the fact that sine wave inverters use pulse-width-modulation at high frequencies. The lower supply voltage of the transformer inverters eases safe operating area (SOA) considerations as will be discussed in the section on transformer-output inverters. Furthermore, the transformerless architecture can output high levels of dc that can damage loads when the output devices fail (or if the controller fails).

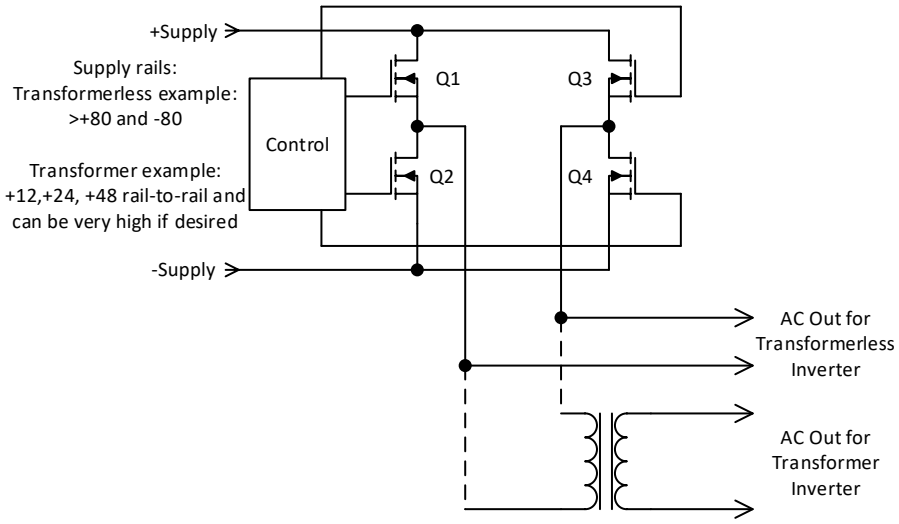

Fig. 1. Basic block diagram of inverter depicts examples of both transformer and transformerless output stages. Transformerless inverters use internal dc-dc converters to step the low-voltage dc input up to the required rail voltages shown in the figure.

Considerations For Power Switching With MOSFETs

All inverters operate their output devices in a switched mode. Proper discipline in the use of MOSFETs in particular dictates that the MOSFET gate driver always provide the highest possible gate-drive voltage. This ensures that the MOSFET operates in the region where $R_{DS(ON)}$ dominates and exhibits a positive temperature coefficient ($R_{DS(ON)}$ increases with temperature), which in turn ensures current sharing. When we discuss current limiting in MOSFETs, at first glance it seems as if we violate this rule. However the MOSFET becomes part of a small current-regulating circuit preventing runaway.[1]

Protection Methods

A good point to begin discussion of how to protect power output devices is to examine techniques used in linear power amplifier circuits, particularly IC-based circuits. The techniques to be described have proven themselves for many years in critical applications and these techniques serve as models for the direction of inverter design. Techniques such as these seem to have been forgotten in an age of code and processors dominating designs.

A variety of power transistor technologies are available for modern inverter design including bipolar, IGBT, MOSFET, and newer varieties of MOSFETs such as silicon carbide (SiC) and gallium nitride (GaN) types. At this time the most popular choices are IGBT and MOSFET but the techniques described can be applied to any device.

Current Limiting

Current limiting is a fundamental form of protection for any power semiconductor. A classic circuit which has been around since the 1970s is unequivocally the best current-limit circuit of all time, shown in Fig. 2. This circuit provides closed-loop current control as well as the fastest possible solution for current limiting. This circuit is widely used in analog and digital power amplifiers as well as monolithic and hybrid power amplifiers.

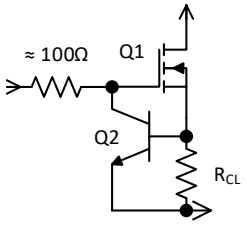

Fig. 2. Simply the best closed-loop current limiter for a power device of any type (MOSFET, bipolar, etc.). Nothing is faster. Current is determined by the choice of R_{CL}, with most general-purpose bipolar transistors (e.g. 2N3904) the current limit value is $0.7/_{RCL}$. The 0.7 in the equation decreases at approximately 2.2 mV/°C which can also be an advantage as generally, current handling ability decreases with temperature.

Regrettably, the circuit of Fig. 2 is not widely used in inverters. The datasheet of a popular inverter driver IC, the EGmicro EG8010 depicts a typical schematic of how current limiting is implemented and the relevant parameters, as shown in Fig. 3. The specified 600-ms delay along with no current limiting at the power device forces conditions that can exceed the SOA of any available power semiconductors. So relying on the current limiting implemented in the selected controller IC, we cannot have 100% confidence that this inverter will not fail under short circuit conditions. But just adding the basic current clamp of Fig. 2 could greatly enhance the reliability of inverters built using this controller IC and by extension other, similar controllers.

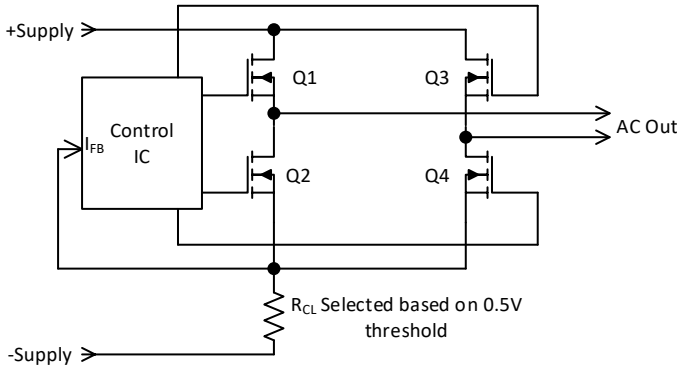

Fig. 3. Implementation of current limiting in a popular inverter control IC. If >0.5 V is observed on R_{CL} then the inverter will shut down. But according to the data sheet "overcurrent detection time is 600 ms" and no power device could be found that has an SOA to support the limit current (e.g. 50 A for a 4-kW at 120-V inverter) for such duration.

SOA Protection

The difficulty with MOSFET protection is best illustrated by examining an SOA plot. Fig. 4 depicts an SOA plot for an onsemi FQA30N40-D MOSFET rated at 400 V and 30 A. These are typical values useful in the output of a transformerless inverter (although even this device may be used in multiples in parallel). Note how rapidly the safe current level drops with increasing voltage stress.

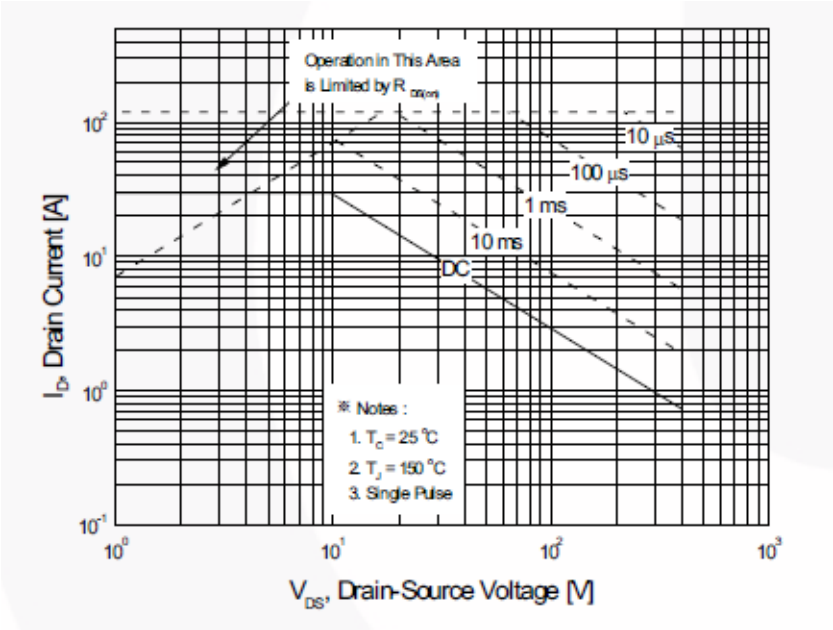

Fig. 4. SOA plot for a 400-V, 30-A MOSFET.

To improve confidence in the inverter's ability to tolerate a short circuit, foldback current limiting can be added to the basic current limit of Fig. 2 to stay closer to or within SOA limits as the voltage across the MOSFET increases. What's more, adding two resistors to the current limit circuit of Fig. 2 provides dynamic response to the output voltage swing. This enhanced closed-loop current limiter is shown in Fig. 5. As the drain-to-source voltage increases, the divider begins to increase the base voltage on Q2 effectively reducing the threshold value for current limiting.

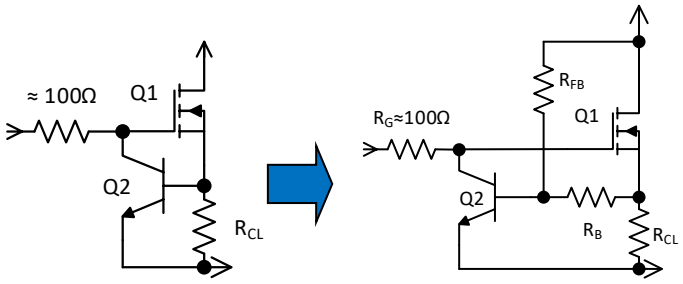

Fig. 5. The original foldback current limiting circuit from Fig. 2 (repeated here on the left) can be enhanced with the addition of a feedback resistor (as shown in the circuit on the right) to shape current limiting for closer conformance to the SOA of the power MOSFETs.

R_B should be set to a low value such as 100 Ω. Considering R_{CL} is typically three orders of magnitude below R_B, it is reasonable to ignore R_{CL} and say R_B and R_{FB} form a voltage divider between the MOSFET source and drain. With R_{FB} typically being a couple orders of magnitude larger than R_B, the divider adds a portion of the drain-to-source voltage in series with the base of Q2.

At low drain-to-source voltages R_{CL} alone determines the current limit. At higher voltages the combined effect of the divider reduces the current limit (avoid very low, or less than zero values as latching could occur). Values can be determined using the following equations:

$$I_{CL} = \frac{0.7 - V_{DS} \times (\frac{R_B}{R_{FB} + R_B})}{R_{CL}}$$

$$R_{CL} = \frac{0.7 - V_{DS} \times (\frac{R_B}{R_{FB} + R_B})}{I_{CL}}$$

The current limiting does not need to consider continuous operation. For example, combining this analog current limiting with the control provided by the IC requires the analog current limit to be active for only 600 ms until shutdown. And it contributes to the possibility of creating a truly "bulletproof" inverter output stage.

Parallel MOSFETs And Current Limiting

Most inverters parallel some number of MOSFETs in their output stages. With parallel MOSFETs each MOSFET is required to have its own current limit circuit as shown in Fig. 6. While a single "master" current limit could be added to this circuit (on the MOSFET source side) the closed loop control of each MOSFET enforces sharing between devices.[2]

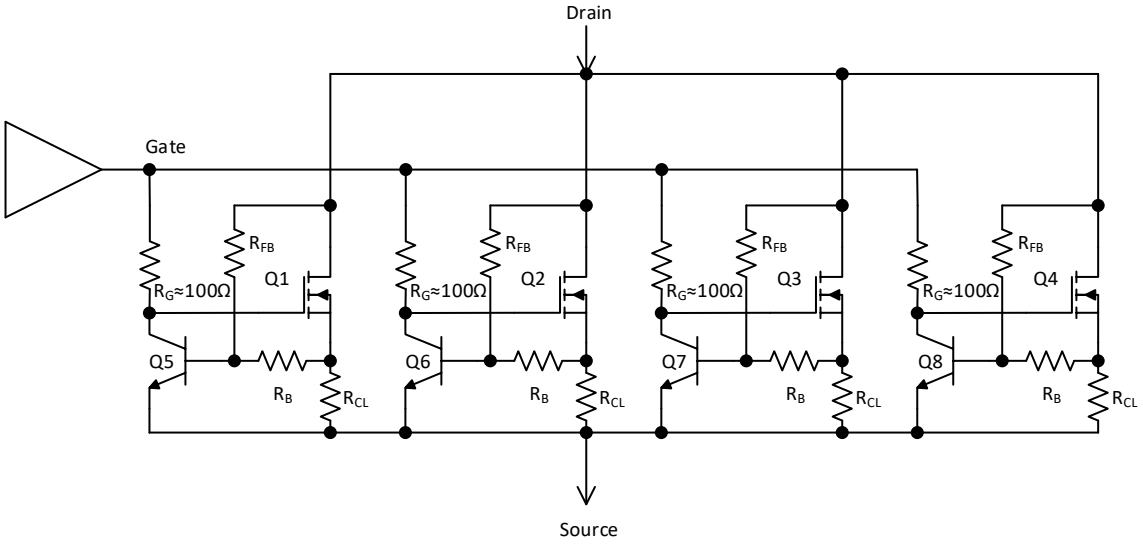

Fig. 6. When paralleling MOSFETs each individual MOSFET should have its own current limit circuit to prevent "current hogging".

Transformer- Vs. Transformerless-Output Inverters

Systems such as typical off-grid inverters are used where the highest typical dc input is 48 V (and for transient ruggedness the devices and inverter should withstand >60 V). (Note that in the vast majority of PV systems, the arrays feed chargers and batteries that control the voltage seen by the inverter. Some grid-tie micro inverter systems connect the array directly to the inverter connections but such systems are not the focus here.)

Transformerless off-grid inverters first convert the dc input up to voltage levels required by the bridge to deliver either 120 Vac, 240 Vac, or both. However, transformerless off-grid inverter designs are handicapped at the outset from the standpoint of protection by the need to operate the output switches at high voltage. In contrast, a transformer-output design has a significant advantage related to ruggedness and reliability by allowing the output switch designs to operate at much lower voltages with the transformer providing the stepup to the required ac line voltage. (Industrial and utility inverters have high-voltage dc inputs, IGBTs, and significantly different requirements than those discussed in this article).

A limitation caused by the high-voltage of transformerless inverters is the previously discussed reduction in SOA apparent in many MOSFETs at high voltages. This behavior is well documented elsewhere and is related to the degradation in current sharing among the individual cells on the MOSFET die. This phenomenon is often referred to as the Spirito effect and is similar to second breakdown in bipolar power transistors.

Fig. 7 is the dc SOA for an onsemi NTH4L015N065SC1-D MOSFET plotted along with a constant power line. This clearly shows that the SOA is at an advantage at lower voltages. An advantage of a transformer-output inverter is that it can operate the MOSFETs (or whatever power switch technology is selected) at much lower voltage with significant improvement in available SOA.

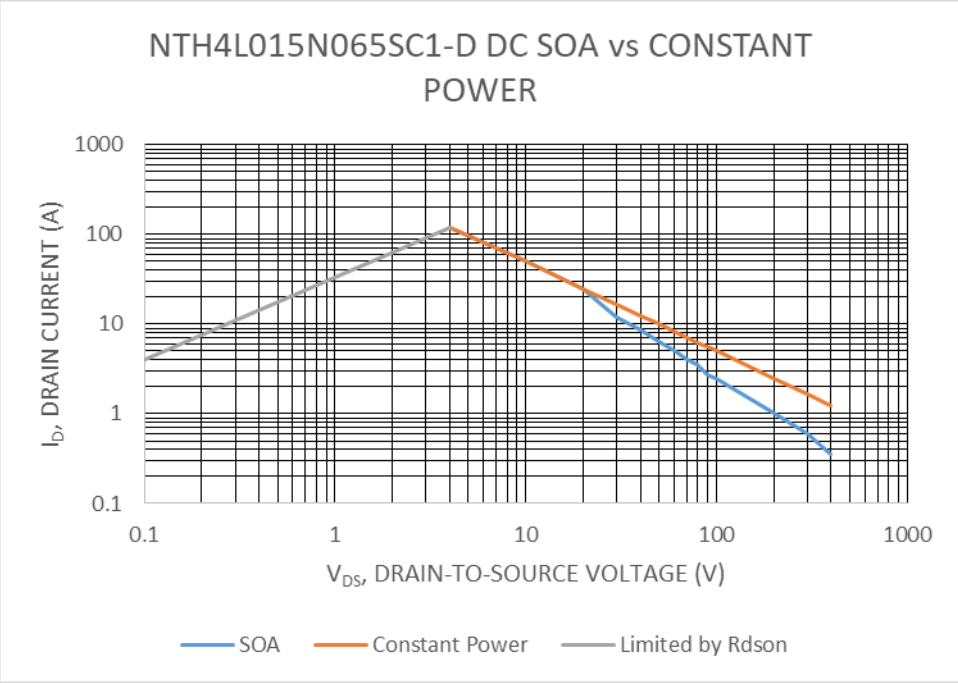

Fig. 7. The SOA of the NTH4L015N065SC1-D power MOSFET is plotted along with a constant power line depicting the reduction in SOA at higher voltages.

MOSFET Driver Developments

A recent development in MOSFET drivers is the TI UCC5870 isolated MOSFET driver which is notable for its provision for current limiting, which is in line with the type of current limiting that this article recommends. While this article proposes a completely analog solution, which is still the fastest and the best, the TI device feeds the current signal back through internal logic which creates a delay, although according to the data sheet much less delay (it's specified in hundreds of nanoseconds) than the inverter control IC mentioned previously. Furthermore the current-sensing architecture of this IC makes possible the addition of resistors at the MOSFET and current limit pins to implement foldback current limiting as shown in Fig. 8.

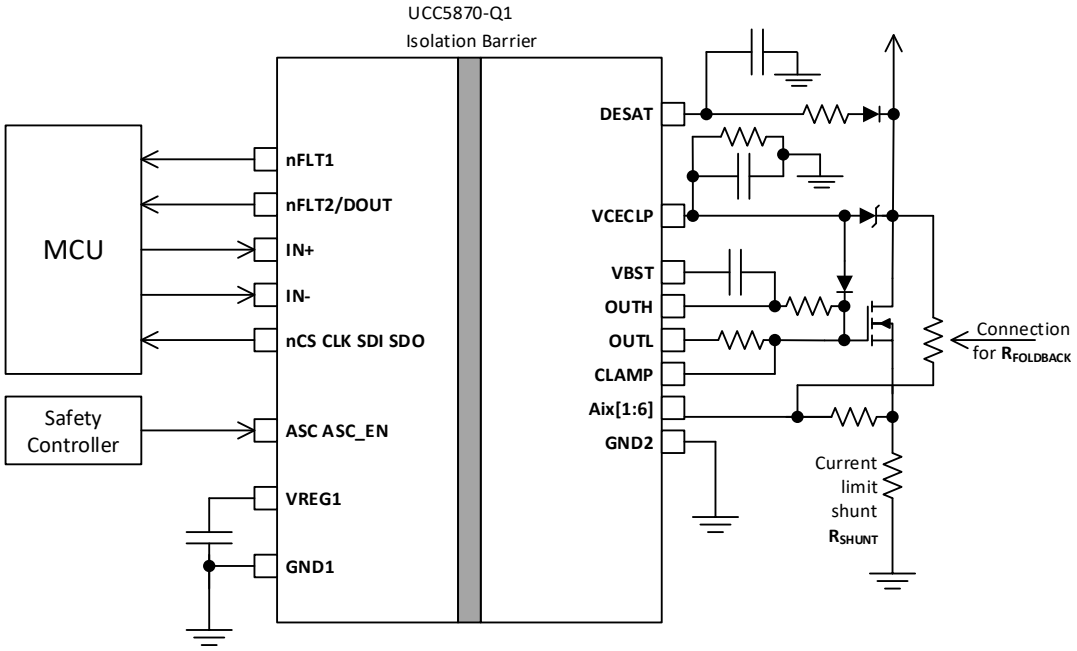

Fig. 8. Partial schematic of TI's UCC5870 showing MOSFET current limiting and how foldback limiting could be implemented.

Current-Sense And Temp-Sense MOSFETs, And Thermal Shutdown

The TI UCC5870 offers curious features that at first glance could be very valuable—if the additional components required to implement them were widely available. In other words, the following UCC5870 features would be good to have if it were actually possible to implement them:

- Using current-sensing MOSFETs for current sensing.
- Using MOSFETs with on-chip temperature sensing for MOSFET temperature protection. Quoting the UCC5870 data sheet, "The temperature protection is intended for power transistors with integrated temperature sensing diodes."

Current-sensing MOSFETs are very familiar to many power designers who have been in the business for a while. They seemed to be widely available in the early 90s but the offerings have been greatly reduced over the years. While an entire article can be written about current-sensing MOSFETs, the method has many advantages and some disadvantages that clever design can often overcome.

Similarly, MOSFETs with on-chip temperature sensing diodes appeared in the early 2000s. In fact, at that time this author researched the devices to see if the diodes behave according the familiar kT/Q equations that extrapolate to zero at absolute zero temperature. If so, it would have made it possible to use these diodes as temperature sensors with minimal or no calibration. But characterization and studies of those diodes, which were polysilicon diodes, did not support such a method. Individual calibration would be required.

As with the current-sensing MOSFETs, there appear to be very few offerings for temperature-sensing MOSFETs at this time. On-chip thermal shutdown of MOSFETs is the ultimate MOSFET protection, demonstrated by the many integrated "smart" load switch ICs on the market and demonstrated by Apex Microtechnology many years ago for linear power amplifiers (although that device included foldback current limiting also).

An interesting product would be something like a "stripped down" smart load switch (remove the smart) with thermal protection for a device that otherwise looks like a MOSFET. Such an IC would not be required to provide the charge pump for gate drive (this device would be intended to be an alternative to a "naked" MOSFET).

Discrete implementation is made difficult, as an internal on-chip thermal shutdown is intrinsic to the MOSFET itself. Any attempt to approximate this in discrete circuitry is outside the package and subject to whatever thermal path is between the MOSFET and the sensor. Nonetheless workable thermal protection can and has been done.

Inspection of many inverters does reveal the use of thermal sensors on heat sinks, representing a reach of desperation on the part of designers seeking some kind of thermal protection. The closest approach possible has been demonstrated by the attachment of a thermistor to the center, or drain lead of a MOSFET package such as a TO3-PI as shown in Fig. 9.

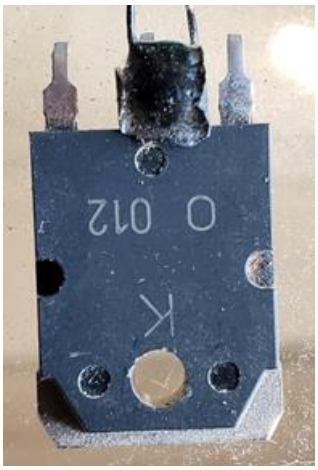

Fig. 9. A thermistor attached to the drain pin of a TO-3PI package represents about the closest thermal coupling you can get with a discrete approach to thermal sensing.

Protecting Loads

While the transformerless inverter offers a number of advantages it suffers from one troubling failure mode: If an output device fails shorted, or a controller fails in such a way as to turn on a device or combination of devices, the inverter can deliver dc, or ac superimposed with high values of dc. This happens, and has happened (including two times for the author, one time I smelled the problem before I realized what happened).

The solution is simple. A transformerless inverter should have a mechanical relay or contactor in its output circuit, normally open. A "dc detector" should then drive this relay such that the relay is enabled only when no dc is detected on the inverter output. This could certainly be a defining feature for high-end transformerless inverters. Obviously transformer-output inverters are immune to this problem.

Summary

The inverter industry is showing that there is a need for reliability improvements, and certainly the ruggedness of output stages is an area where improvements can be made. In particular, transformerless inverters show great promise when failure modes are addressed.

Acknowledgements

A special thanks to Bert Wank of Infinirel for his contributions to and review of this article.

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2. "Techniques For Safely Paralleling MOSFETs In Linear Circuits" by Jerry Steele, How2Power Today, June 2021.

3. "Improving Reliability of Low-Cost Power-Source Inverters" by Dennis Feucht, How2Power Today, October 2020.

4. "Designing an Open-Source Power Inverter (Part 1): Goals and Specifications" by Dennis Feucht, How2Power Today, May 2021.

5. **"**Designing an Open-Source Power Inverter (Part 2): Waveshape Selection" by Dennis Feucht, How2Power Today, September 2021.

The following are general references on inverter reliability for all types (off-grid, consumer, utility and industrial):

6. "Photovoltaic Inverter Reliability Assessment" by Adarsh Nagarajan, Ramanathan Thiagarajan, Ingrid Repins, and Peter Hacke, National Renewable Energy Laboratory, October 2019. This report showcases and describes an approach to help assess and predict the reliability of PV inverters. It focuses heavily on thermal issues and thermal modeling of inverter power stages.

7. "Performance and Reliability of PV Inverter Component and Systems due to Advanced Inverter Functionality" by Jack Flicker and Sigifredo Gonzalez, Sandia National Laboratories, Albuquerque, NM. The results of advanced functionality operation indicated increased thermal and electrical stress on components, which will have a negative effect on inverter reliability as these functionalities are exercised more frequently in the future.

8. The following statements from the Solar Plant Operators page of the InfiniRel website characterize inverter reliability issues:

- "Increasing inverter operation and maintenance costs, which can be as high as 500% of what was budgeted, are driving up solar plant O&M costs."
- "Aging Fleet of Inverters: In 2017 Power-Technology reported that 176-GW of Global inverter capacity was 5-yrs of age. That number continues to increase."
- "Fail Without Warning: Failures can occur within thousandths of a second without any discernible warning signs."

9. Also taken from the Solar Plant Operators page of the InfiniRel website, the following are proposed solutions to inverter reliability problems:

- "Predictive Maintenance: Measures electronic signatures with highly sensitized equipment that can detect potential problems before they occur," Solar Plant Operators page, InfiniRel website.
- "Timely Analytics: Provides real-time guidance that is as simple as a stoplight and as convenient as an App."

About The Author

Jerry Steele has a long association with power management products from his early days at Burr-Brown, Apex Microtechnology, National Semiconductor and Maxim, and at Texas Instruments as a senior member of technical staff. His experience has covered a variety of products including precision analog and mixed-signal devices dedicated to temperature, current, and power measurement to system management and protection devices including devices such as eFuses and hot swap controllers. Jerry has authored a

considerable number of analog and mixed-signal articles over the years, and co-authored five patents.

For further reading on inverter design, see the How2Power Design Guide, locate the Design Area category and select "DC-AC Inverters". For more on power protection in power converters, see the Design Area category and select "Power Protection."