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Source-Down Power MOSFET Package Now Available For More Devices

Infineon Technologies' new generation of OptiMOS Source-Down (SD) power MOSFETs offers devices in a 3.3-mm x 3.3-mm PQFN package and a wide voltage class ranging from 25 V up to 100 V. According to the vendor, this package sets a new standard in power MOSFET performance, offering higher efficiency, higher power density, superior thermal management and low bill-of-materials (BOM). The PQFN addresses multiple applications including motor drives, SMPSs for server and telecom, OR-ing and battery management systems.

Compared to the standard drain-down concept, the latest source-down package technology enables a larger silicon die in the same package outline. In addition, the losses contributed by the package, which limit the overall performance of the device, can be reduced. This enables a reduction in $R_{DS(ON)}$ by up to 30% compared to the state-of-the-art drain-down package, says Infineon.

The benefit at the system level is a shrink in the form factor with the possibility to move from a SuperSO8 5-mm x 6-mm footprint to a PQFN 3.3-mm x 3.3-mm package with a space reduction of about 65%. This allows for the available space to be used more effectively, enhancing the power density and system efficiency in the end system.

Additionally, in the source-down concept, the heat is dissipated directly into the PCB through a thermal pad instead of over the bond wire or the copper clip. This improves the thermal resistance $R_{\theta JC}$ by more than 20%, from 1.8 K/W down to 1.4 K/W, thus enabling simplified thermal management.

Infineon offers two different footprint versions and layout options: the SD Standard-Gate and the SD Center-Gate. The Standard-Gate layout simplifies the drop-in replacement of drain-down packages, while the Center-Gate layout enables optimized and easier paralleling of devices. These two options can bring optimal device arrangement on the PCB, optimized PCB parasitics and ease of use. For more information see the Source-Down PQFN package page.

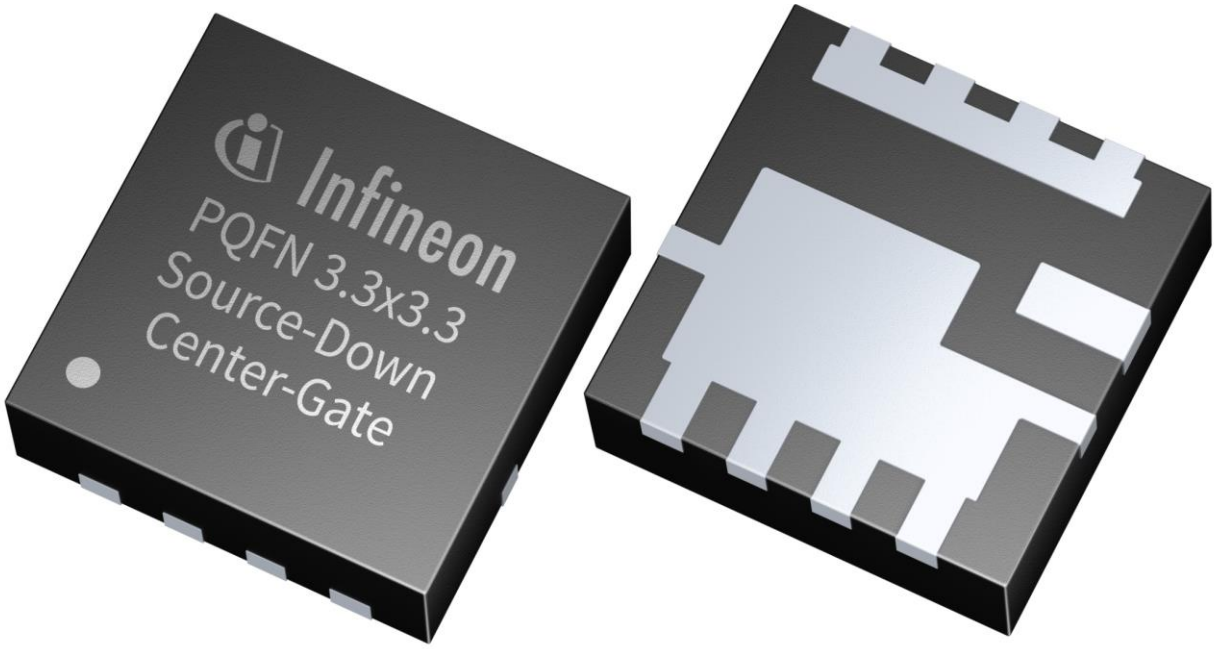

Figure. Infineon has broadened its portfolio of OptiMOS Source-Down (SD) Power MOSFETs, adding voltage options (25 V to 100 V), FOM options and two different footprint versions, allowing designs across more applications. Source-down packaging also permits larger silicon die in the same surface area as traditional drain-down devices while reducing losses contributed by the package. Application benefits include higher power density and efficiency, as well as improved thermal management and reduced bill-of-materials.