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Developing A 25-kW SiC-Based Fast DC Charger (Part 8): Thermal Management

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In parts 1 through 7 of this series,[1-7] we describe the development of a 25-kW fast dc EV charger using a wide portfolio of silicon carbide (SiC) power modules and power components from onsemi. In this part, we are going to focus on thermal management of the overall design to improve efficiency, reliability and prevent premature failures in the system.

First, we will go over the various advantages of SiC MOSFET modules versus discrete SiC MOSFETs from the perspective of switching losses and thermal assembly. Second, we will describe thermal management techniques and calculations used to design the cooling fan assembly and control system, and how we leveraged the internal NTC feature of the SiC power module to automatically control fan cooling in the PFC and dc-dc stages. The design of the PWM-to-voltage converter that is used to regulate fan RPM is discussed at length, with simulations presented to demonstrate key aspects of its operation and the design of its compensator.

Discrete Versus Module

Switching Losses

SiC MOSFET modules typically provide higher efficiency when compared to discrete SiC MOSFETs due to their reduced parasitics. For example, the table below compares a discrete 20-mΩ/1200-V SiC MOSFET with Kelvin source in a TO247-4 leaded package (the NTH4L020N120SC1[8]) and a SiC MOSFET module (the NXH020F120MNF1PTG[9]).

Table 1. Comparing switching losses of a discrete SiC MOSFET versus a SiC MOSFET module.

NTH4L020N120SC1 (discrete SiC)		NXH020F120MNF1PTG (SiC module)	
E_{ON}	E_{OFF}	E_{ON}	E_{OFF}
0.49 mJ	0.39 mJ	0.24 mJ	0.24 mJ

The specs in Table 1 are taken from the datasheets of the products and they show that the module has lower switching losses. This is due to the lower parasitic inductance in the package, which allows higher power capability. As a result, SiC modules can operate at a higher switching frequency than discrete MOSFETs for the same output in the system. Higher switching frequency operation helps in reducing passive component size, and overall design size.

Thermal Assembly

Package assembly plays an important role in thermal management. Discrete MOSFETs and modules do not have the same thermal assembly. In a discrete MOSFET package, the die is usually attached to a copper pad (or a "tab"). This copper pad is molded and visible externally as a heat tab comes in contact with air or an external heatsink. However, a thermal interface material (TIM) or thermal compound is used between the MOSFET and the heatsink. The thermal pad is used for two reasons:

- To improve heat conduction from the MOSFET heat tab to a heatsink
- To electrically isolate the heat tab from the heatsink.

This assembly is shown in Fig. 1 below.

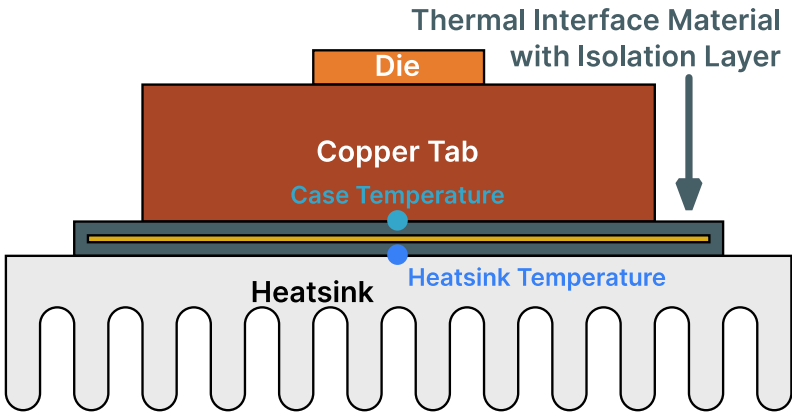

Fig. 1. Thermal assembly of a discrete FET. The locations used for temperature measurement are identified.

The NTH4L020N120SC1 discrete SiC FET has a junction-to-case thermal impedance of 0.3°C/W. If a TIM with a thermal impedance of 3°C/W is used between the MOSFET and a heatsink, Fig. 1 can be represented with thermal impedance values as shown in Fig. 3 (and table 2) and the total thermal impedance between the MOSFET and the heatsink would be 3.3°C/W.

A power module's thermal assembly differs significantly when compared to a discrete MOSFET's. Since the module uses a DBC (direct bonded copper) to attach the MOSFET die, the junction-to-case thermal impedance already includes the isolation layer.

We have also selected a module in Table 1 with pre-applied phase change thermal material. Phase change material is excellent to fill the void between DBC and the heatsink. As it maximizes the contact surface between the two pieces, it reduces the thermal impedance of the total assembly. Fig. 2 below shows this assembly.

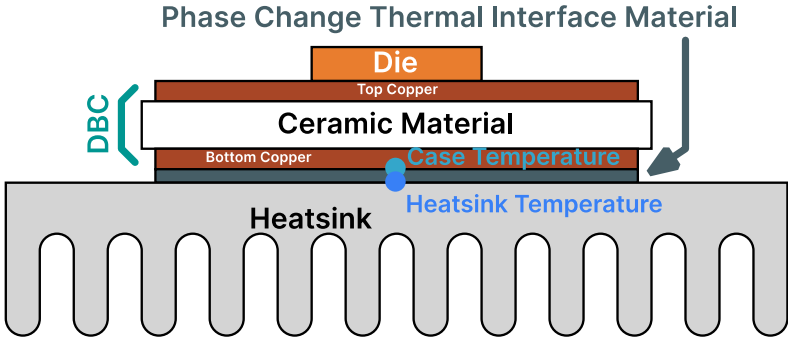

Fig. 2. Module package thermal assembly with case and heatsink temperature measurement points identified.

The 20-mΩ, 1200-V SiC MOSFET module (NXH020F120MNF1PTG) data sheet[9] provides thermal impedances for both junction-to-case and junction-to-heatsink, specifying their values as 0.45°C/W and 0.80°C/W, respectively. Table 2 summarize those values.

Table 2. Comparison of thermal impedance for discrete versus modular packages.

NTH4L020N120SC1		NXH020F120MNF1PTG	
R_{thJC}	R_{thJH}	R_{thJC}	R_{thJH}
0.3°C/W	Min 1°C/W 3.3°C/W with 5-kV isolation	0.45°C/W	0.80°C/W with 5-kV isolation

While the junction-to-case R_{th} is lower for a discrete package, the full thermal assembly will show a higher thermal impedance than the module's thermal assembly. Also, modules provide better heat transfer capability than discrete packages. Modules will allow higher power flow capability for the same die value (a 20-mΩ, 1200-V SiC MOSFET die in this example).

Fig. 3 below shows the thermal equivalent drawings for each thermal assembly (discrete and module). The 25-kW fast dc charger uses SiC MOSFET modules for their higher thermal performance.

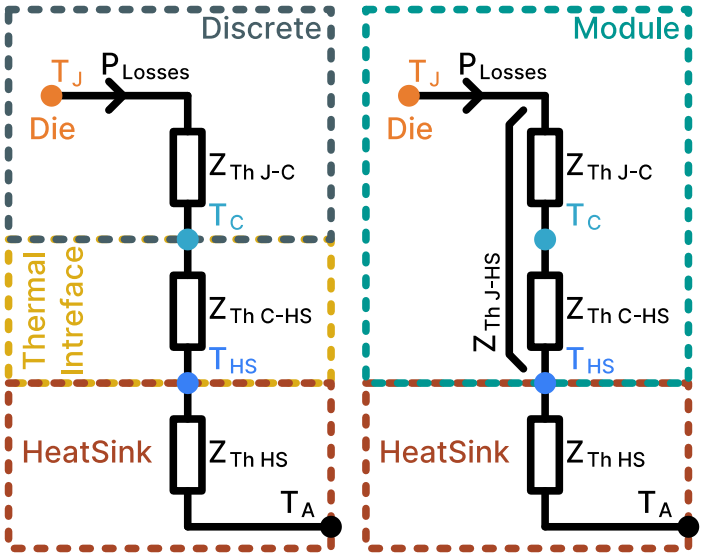

Fig. 3. Electro-thermal equivalent schematics for both assemblies (discrete and module).

Thermal Solutions For PFC And DC-DC Stages

This section describes the thermal solutions designed for the PFC and dc-dc stages. To create a compact dc charging module, we decided to use cooling fan assemblies with low thermal resistance and small form factor. As mentioned in the previous section, SiC modules exhibit a low thermal resistance and in this case they have integrated NTCs.

A PWM-to-voltage converter is used to control the cooling fan assemblies and cooling is regulated automatically based on the SiC PIM's (NXH010P120MNF1) internal temperature, measured by the integrated NTC (see Fig. 4). This approach lowers the extensive noise from the cooling mechanism when the charging module is running at low output power levels.

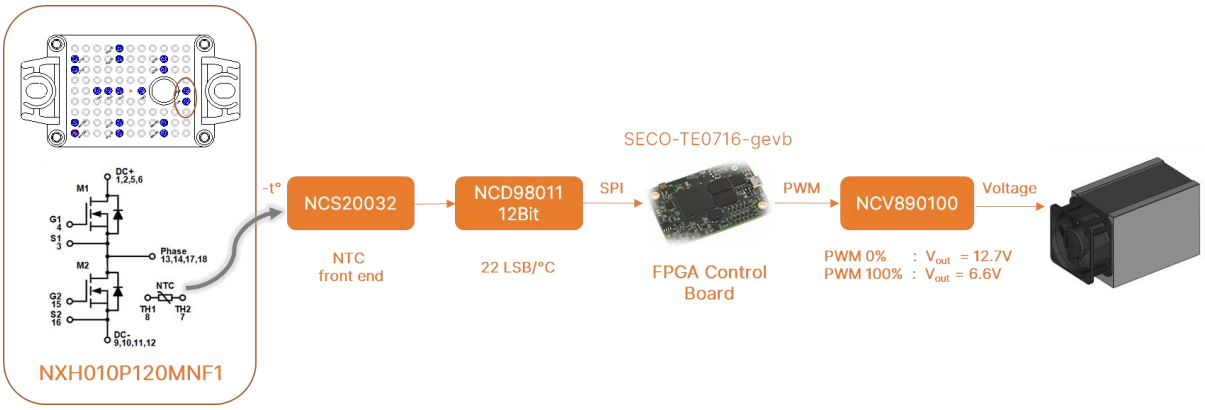

Fig. 4. Block diagram of the fan cooling control loop.

A sketch of the mechanical and cooling concept with cooling fan assemblies and PIM modules is shown below in Fig. 5.

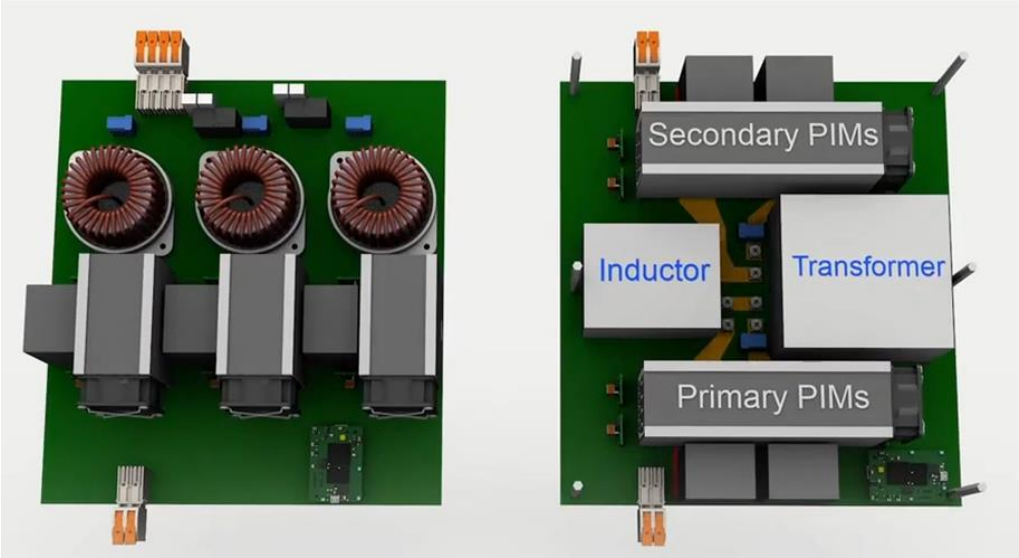

Fig. 5. Mechanical sketch and cooling concept with heatsinks and fans. On the left is the PFC stage with fan assemblies attached to PIMs and blowing towards PFC chokes. On the right is the dc-dc converter stage with fan assemblies attached to primary and secondary PIMs.

The assumed ambient temperature is 30°C (maximum) since there is no housing in the design. The scope of the PFC and dc-dc stage thermal design is not to perform accurate CAD tool simulations with thermal models of certain components, but to use a simple design using power losses of critical components from a thermal management point of view and to choose a cooling concept based on off-the-shelf heatsink design (not custom).

PFC Stage Thermal Design

The critical components for thermal management in the PFC stage are three SiC half-bridge power modules and three PFC power chokes. The power losses of the components must be analytically evaluated prior to the heatsink selection and design. The thermal performance of the PFC chokes was evaluated with expected losses (~27 W/choke) simulated using a dc current flowing in the winding. The PFC choke manufacturer supported us by performing fan tests. When a fan with 3 m^3/s of airflow was applied, the temperature rise was less than 30°C. This test result was used in fan selection.

Results from the SPICE simulation were used to evaluate expected power losses in the SiC modules, (from part 3[3]). The overall peak power loss in the PIM modules reaches ~240 W at low line which is the worst-case scenario as shown in Fig. 6, which is approximately 80 W/PIM module.

Based on these results, a cooling fan assembly with a thermal impedance Z_{th} of 0.2°C/W was selected. With a power loss of 80 W, the rise in temperature should be approximately 16°C (80 W x 0.2°C/W). Since the maximum room temperature is assumed to be 30°C, the temperature of the cooling system should be at around 46°C.

As demonstrated by our magnetics evaluation, fan cooling keeps the PFC chokes' temperature rise under 30°C. PFC floor planning with SiC PIM module cooling fan assemblies blowing the air directly towards the PFC chokes assures stable thermal performance of the whole PFC stage.

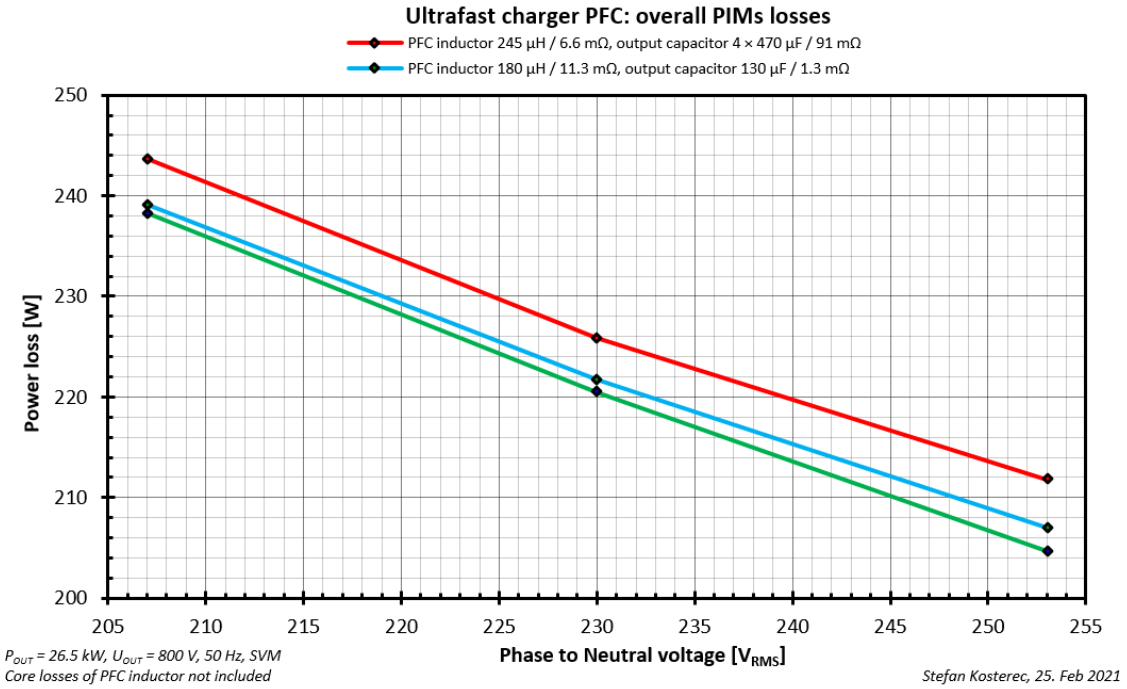

Fig. 6. Overall power loss of PFC stage PIM modules as a function of input phase-to-neutral voltage for three PFC inductors values.

Dual Active Bridge (DAB) DC-DC Stage Thermal Design

The critical components for thermal management in the DAB dc-dc stage are four SiC PIM half-bridge power modules, a dc-dc transformer, and a resonant choke. We assume the same approach to thermal design as in the PFC stage design.

The DAB dc-dc transformer and resonant inductor are designed with a maximum temperature rise of 70°C without cooling. Assuming an ambient temperature of 30°C, the magnetics will then reach a temperature of 100°C. Since this is a high temperature, we decided to use one fan dedicated to cooling down the magnetics. Results from SPICE simulations (from part 4[4]) are used to evaluate expected power losses in the PIM SiC modules. In the DAB dc-dc topology, we use a transformer with a turns ratio of 1.2:1 (red curve in Fig. 7).

From Fig. 7, the combined peak power loss of the primary PIM modules is 300 W and from Fig. 8, the combined peak power loss of the secondary PIM modules is 150 W. In the DAB dc-dc stage we decided to use one cooling fan assembly for primary PIMs and one for secondary PIMs. We choose cooling fan assemblies with a thermal impedance Z_{th} of 0.15°C/W.

With the chosen assemblies and assuming a 30°C ambient temperature, the peak temperature of the primary cooling system reaches 75°C and the peak of the secondary cooling system reaches 52.5°C. The fan speed is controlled by a PWM based on input from the PIMs' NTC temperatures as well.

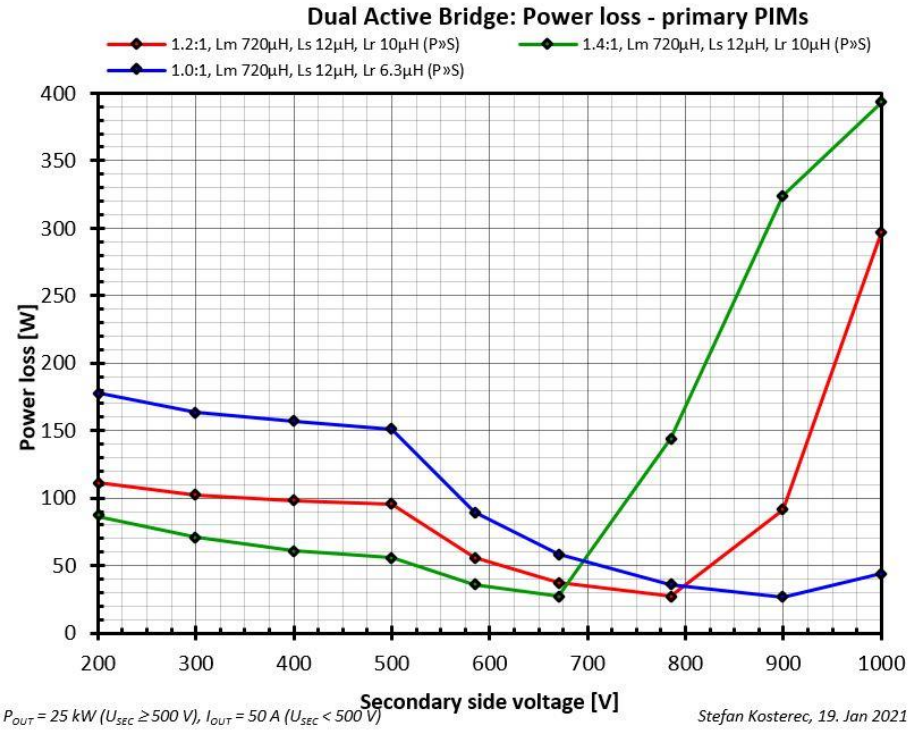

Fig. 7. Overall power loss of DAB dc-dc stage's primary PIM modules as a function of dc-dc secondary voltage for three DAB transformer turns ratios. (Red curve assumed in the design).

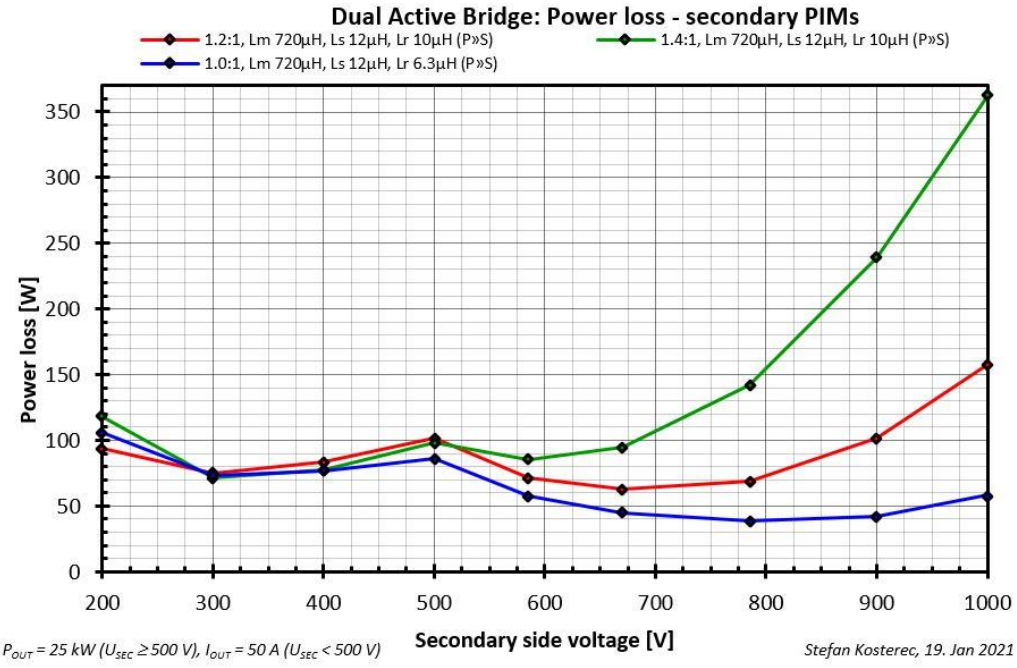

Fig. 8. Overall power loss of the DAB dc-dc stage secondary PIM modules as a function of the dc-dc secondary voltage for three DAB transformer turns ratios. (Red curve assumed in the design).

Negative Thermal Coefficient (NTC) Thermistor Front End Circuitry

The NXH010P120MNF1 SiC half-bridge PIM module features an internal 5-kΩ NTC thermistor, which allows us to measure the internal die temperature. The NTC is critical to design an automatic cooling system for an attached heatsink. Internal PIM module temperature is measured with ADCs present on the UCB.

From the PIM datasheet we list the following NTC parameters in Table 3.

Table 3. Thermistor characteristics.

Nominal resistance	T= 25°C	R_{25}	—	5	—	kΩ
Nominal resistance	T= 100°C	R_{100}	—	457	—	Ω
Deviation of R25		ΔR/R	-3	—	3	%
Power dissipation		P_D	—	50	—	mW
Power dissipation constant			—	5	—	W/K
B-value*	B(25/50), tolerance ±3%		—	3375	—	K
B-value*	B(25/100), tolerance ±3%		—	3455	—	K

*Note: The B-value describes the shape of the slope of the resistive curve over temperature (R/T). In this case, the B-value defines the thermistor's material constant between the range of T1 (25°C) and T2 (50°C or 100°C).

The NTC thermistor's temperature sensitivity (its change in resistance based on temperature) is important to design a suitable NTC front end circuit. Using a nominal resistance of 5 kΩ at 25°C and the B25/100 constant we can use the equation for resistance calculation at a given temperature. Calculations can be simplified by simulation to get the NTC resistance sensitivity to temperature. The value of the B25/100 constant used in simulation is 3455°K, and a simulated characteristic is shown in the Fig. 9, red curve. The blue curve shows the impact of the B25/100+3% tolerance, which we used to assess the possible impact of the tolerance on the NTC resistance. In the NTC front end circuitry design, we decided not to take into account the B-value ±3% tolerance.

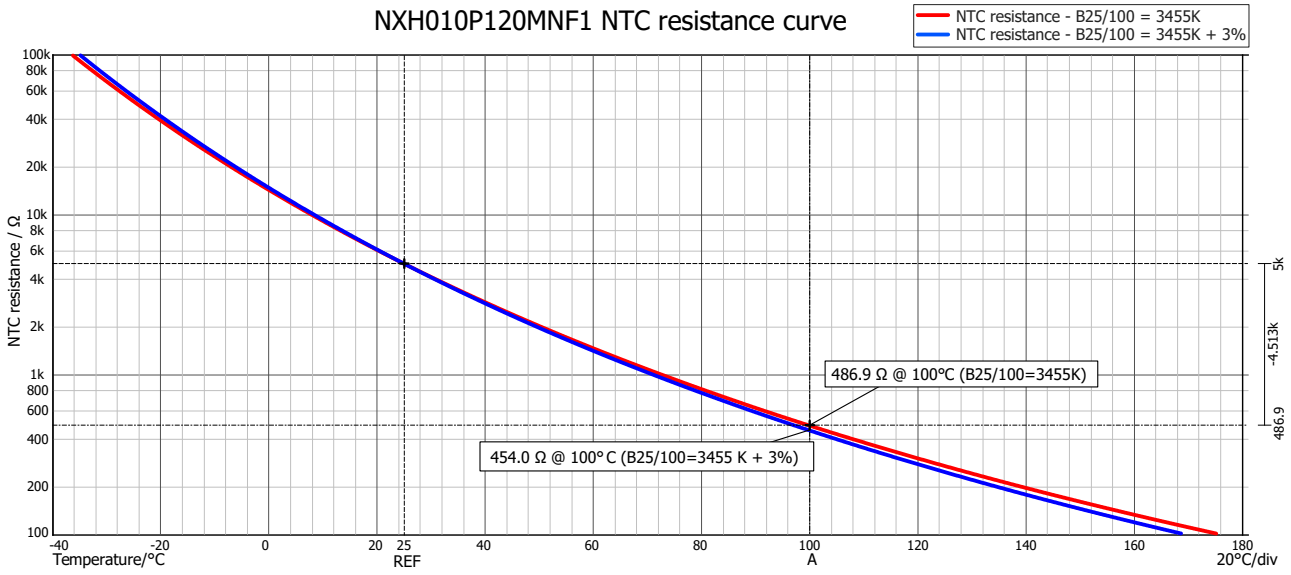

Fig. 9. Simulated dependence of the PIM NXH010P120MNF1's integrated NTC resistance (Ω) on temperature (°C).

Measuring the resistance vs. temperature characteristic on a logarithmic scale provides low resolution at high temperatures, whereas the resistance changes little at low temperatures (just ~Ω/~°C). Therefore, we decide to use a simple method based on partial linearization. An additional resistor is connected in parallel to the NTC

and this parallel connection is powered through a resistor connected to a fixed Vcc. Simulation circuitry is shown in Fig. 10.

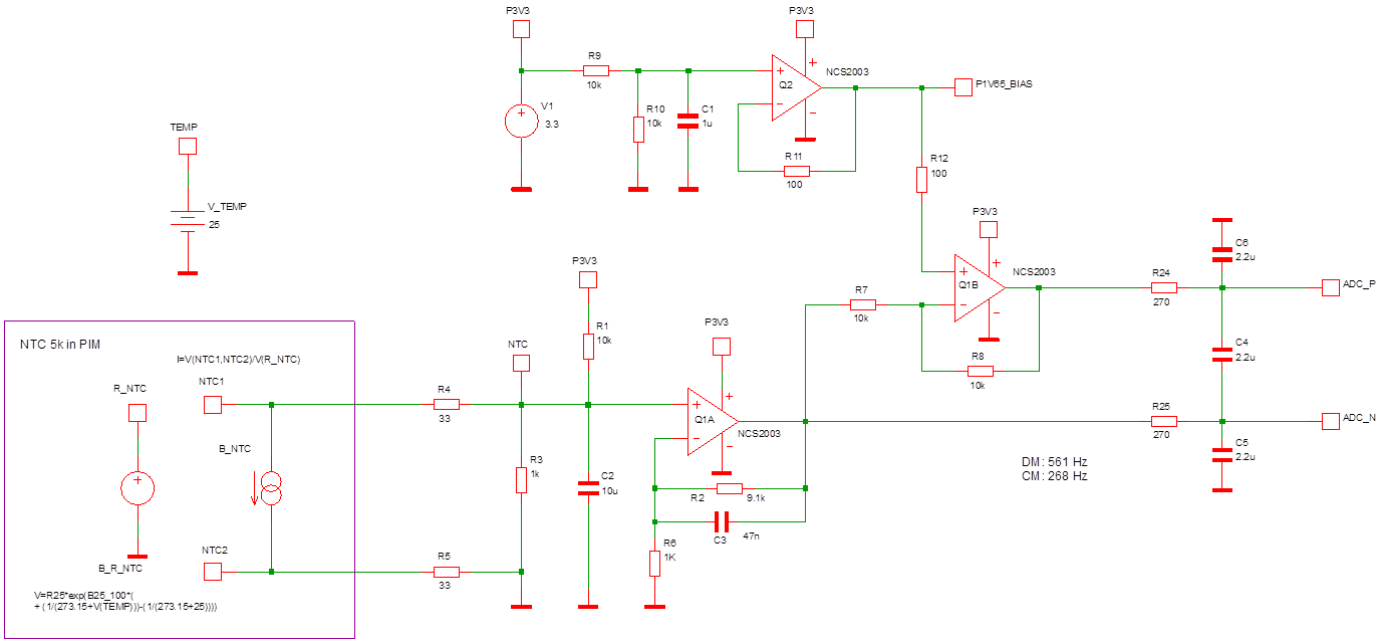

Fig. 10. SPICE model of NTC front end circuitry.

Selecting a suitable resistor R3 to parallel with the NTC and powering resistor R1 can be achieved through linearization. R4 and R5 are decoupling resistors in the PCB layout as it's important to keep the ADC as close as possible to the NTC circuitry. Connection to the NTC should be routed differentially for CMM noise immunity of the temperature measurement circuit.

Op-amp Q1A amplifies voltage from the NTC with the gain set to 10.1. Op-amp Q1B is then used to create a complementary ADC_P signal to create a differential input to the NCD98011 ADC. It's important to note that a complementary signal to the ADC_P signal isn't typically generated; however this is done intentionally to change the negative temperature dependence of the NTC to a positive value. The higher the temperature, the higher the voltage, which is measured by the ADC for post processing in control firmware.

In the next figure, Fig. 11, we show the voltage and current flowing through the integrated NTC in the PIM.

In these simulations, the current reaches values less than 300 µA with the typical current flowing through an NTC being approximately 100 µA. But since the integrated NTC in the PIM module is on the internal substrate, the heat generated by the current through NTC doesn't influence the module temperature. The higher current provides better linearization in the NTC measurement circuitry.

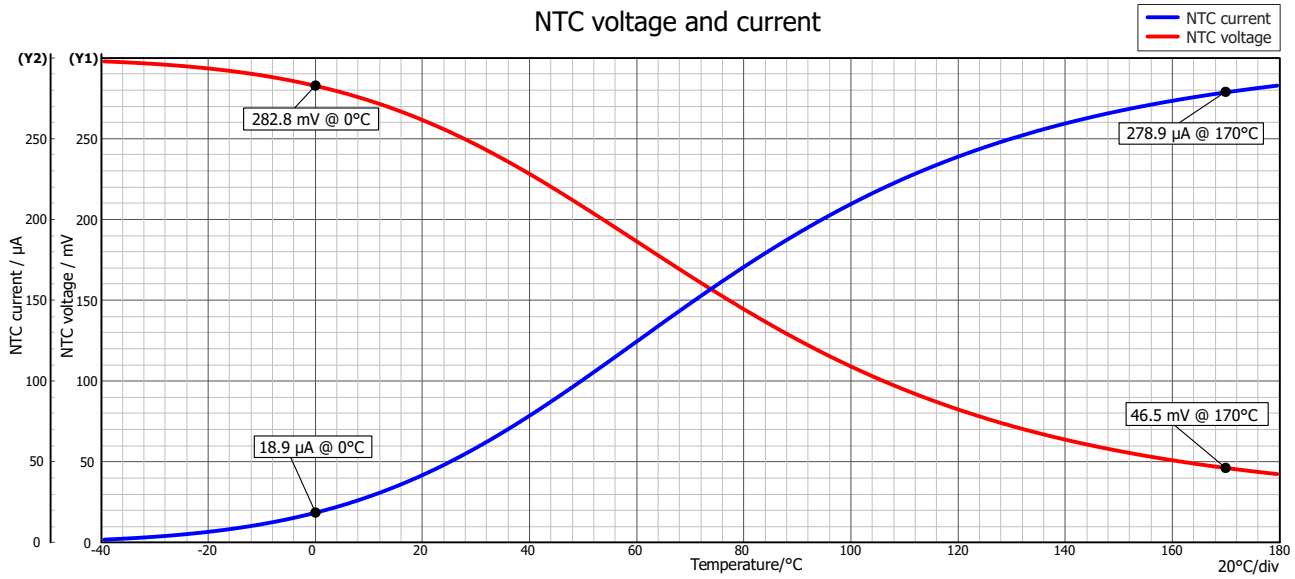

Fig. 11. Simulated voltage and current flowing through the integrated NTC.

Fig. 12 shows the temperature measurement range of the designed circuit, which can be used to measure temperature from -40°C to 180°C. As shown in the figure, the full ±3.3-V voltage range of the ADC is not utilized. However, with the current measurement circuitry reaching a resolution of 0.05°C/LSB, which is 22 LSB/°C, we have fully covered the requirements of temperature measurement in our 25-kW dc charging module design with PIM modules.

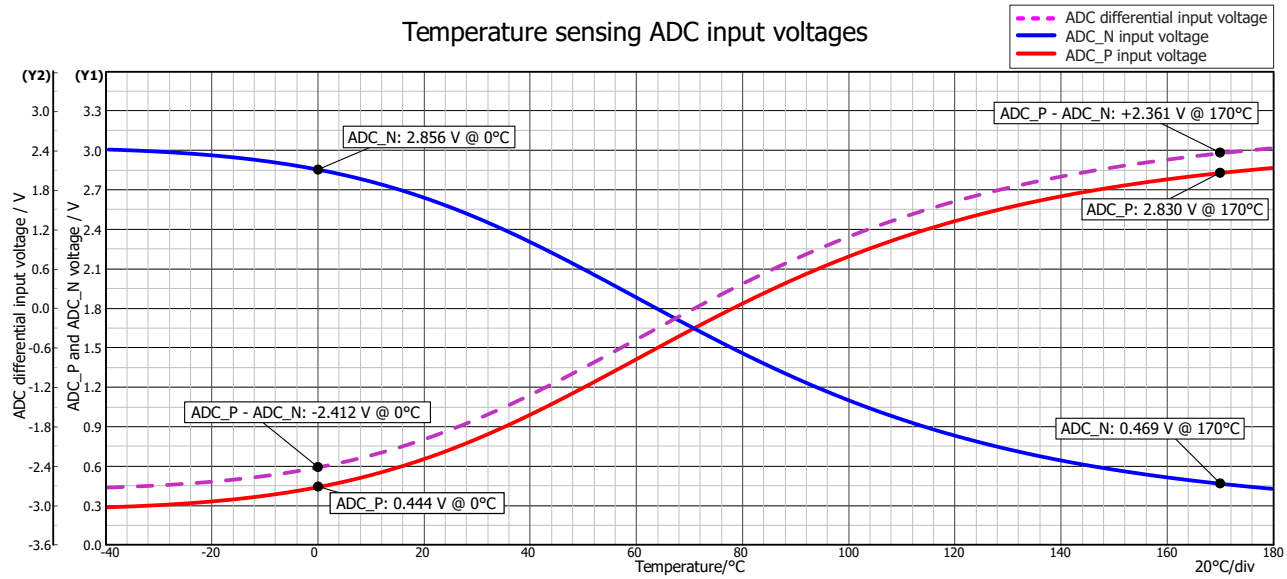

Fig. 12. Temperature measurement range of the designed NTC front end circuitry.

The bandwidth of the NTC measurement circuitry is set to 77.6 Hz, and the simulated attenuation at the PFC switching frequency of 70 kHz is approximately -126.6 dB. This assures that the measured temperature is not disturbed by the main noise source in the PFC stage as well as that in the DAB dc-dc stage where the switching frequency is 100 kHz (see Fig. 13).

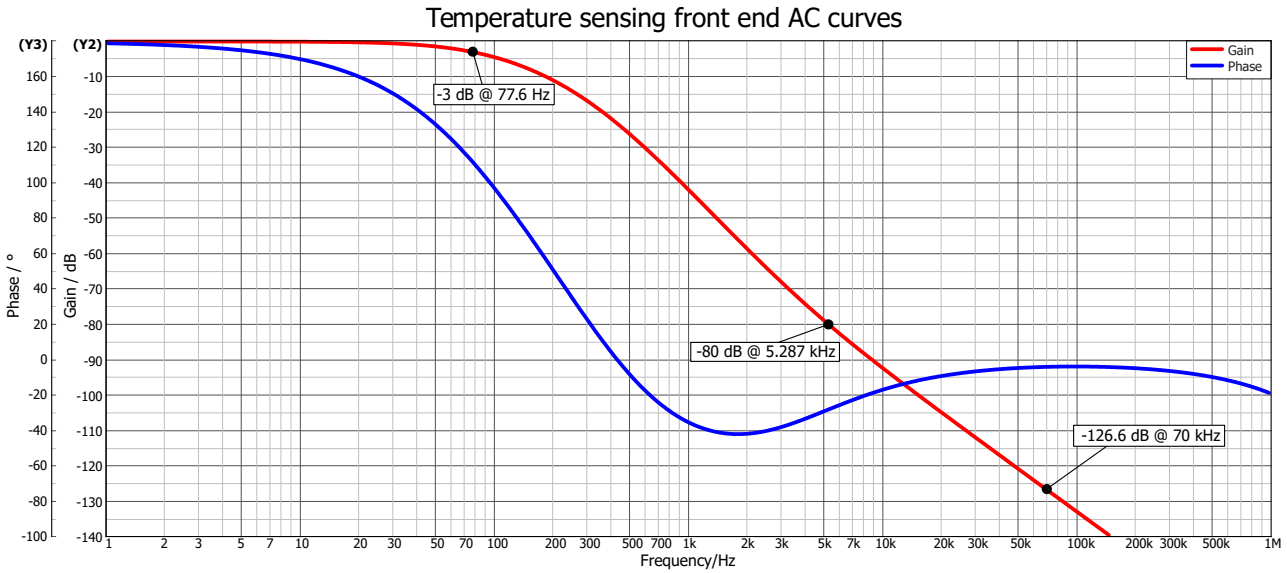

Fig. 13. Frequency characteristic of the NTC measurement circuitry.

Even with the designed linearization, the implementation of temperature measurement in control firmware in the digital domain will require further linearization. A look-up table is normally used as shown in the generated look-up table below

Table 4. Conversion look-up table. ADC output values recorded at different NTC temperature measurements.

Temperature (°C)	ADCdiffin (V)	Nadc (at 3.3 V ADCVref.)
-40	-2.719	-1688
-30	-2.686	-1667
-20	-2.630	-1632
-10	-2.542	-1578
0	-2.412	-1497
10	-2.228	-1383
20	-1.983	-1231
30	-1.675	-1039
40	-1.309	- 812
50	-0.899	- 558
60	-0.466	- 289
70	-0.033	- 20
80	+0.381	+ 236
90	+0.759	+ 471
100	+1.095	+ 680
110	+1.385	+ 860
120	+1.631	+1012
130	+1.837	+1140
140	+2.008	+1246
150	+2.149	+1333
160	+2.265	+1405
170	+2.361	+1465
180	+2.440	+1514

PWM-To-Voltage Converter To Regulate Fan RPM

Since cooling assemblies used in the system are equipped with a fan without an automatic RPM control, we use an onsemi buck switching regulator, the NCV890100, as a PWM-to-voltage converter. Using an ac average model of the NCV890100 (downloadable from onsemi website), we were able to run the simulation model of the PWM-to-voltage controller used for the fan supply. The measured voltage-ampere characteristic of fans used in the cooling fan assemblies was used to design the fan SPICE model, and the fan worked reliably between 6 V and 12 V dc.

In the simulation of the circuit in Fig. 14, it is shown that the OUT dc bias voltage depends on output capacitor capacitance COUT. Since X7S capacitors exhibit high voltage dependence, the output capacitance was modelled with voltage dependence, which has a substantial impact on the ac characteristic of the PWM-to-voltage converter. PWM control from the UCB was modelled as well.

Fig. 14 shows the designed SPICE simulation circuitry with a dc bias for PWM set to 100%. The output voltage is 6.64 V which meets our design considerations. Fig. 15 shows the designed SPICE simulation circuitry with dc bias for PWM set to 0%. The output voltage is 12.7 V which meets our design consideration. Output capacitance is decreased from 9.88 µF to 5.09 µF (two 10-µF capacitors in parallel).

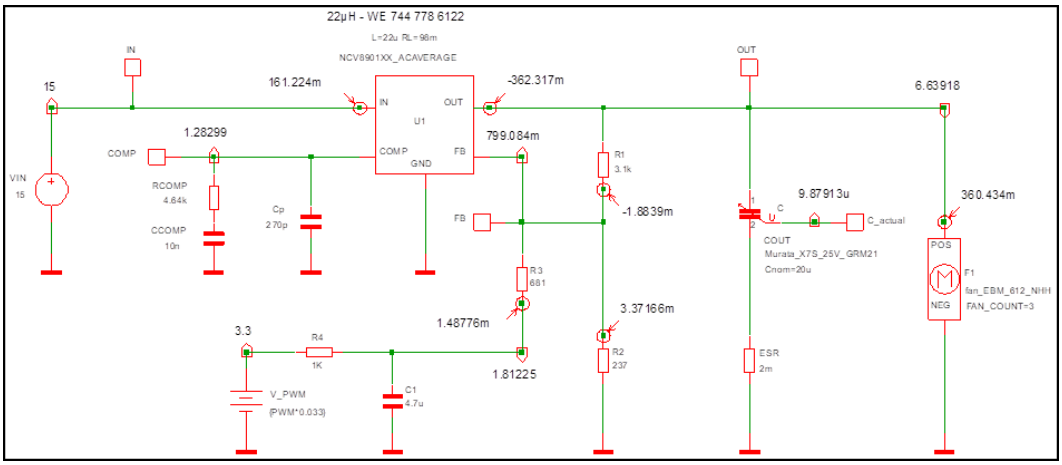

Fig. 14. SPICE model of the designed PWM-to-voltage circuitry with dc bias for PWM set to 100%. The output voltage is 6.6 V.

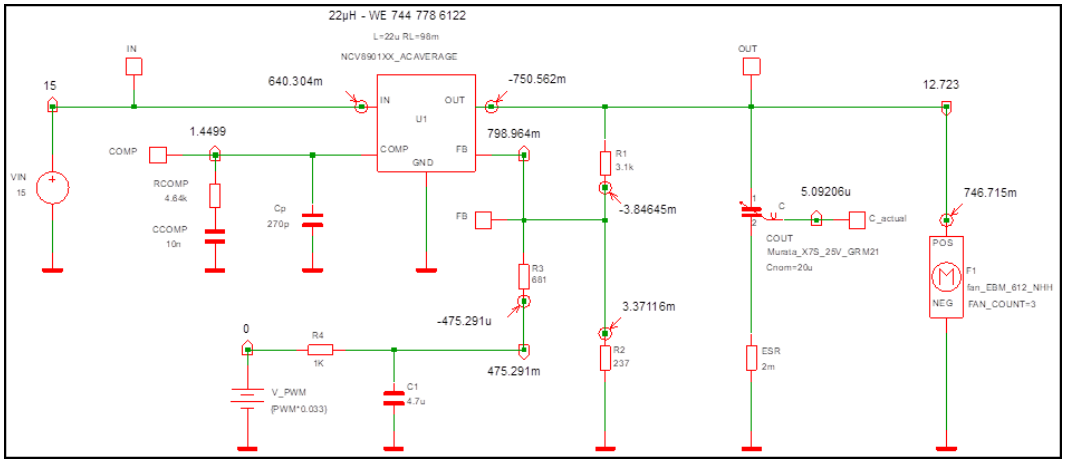

Fig. 15. SPICE model of the designed PWM-to-voltage circuitry with dc bias for PWM set to 0%. The output voltage is 12.7 V.

Fig. 16 shows the PWM-to-voltage converter's analysis and output dependence on the duty cycle.

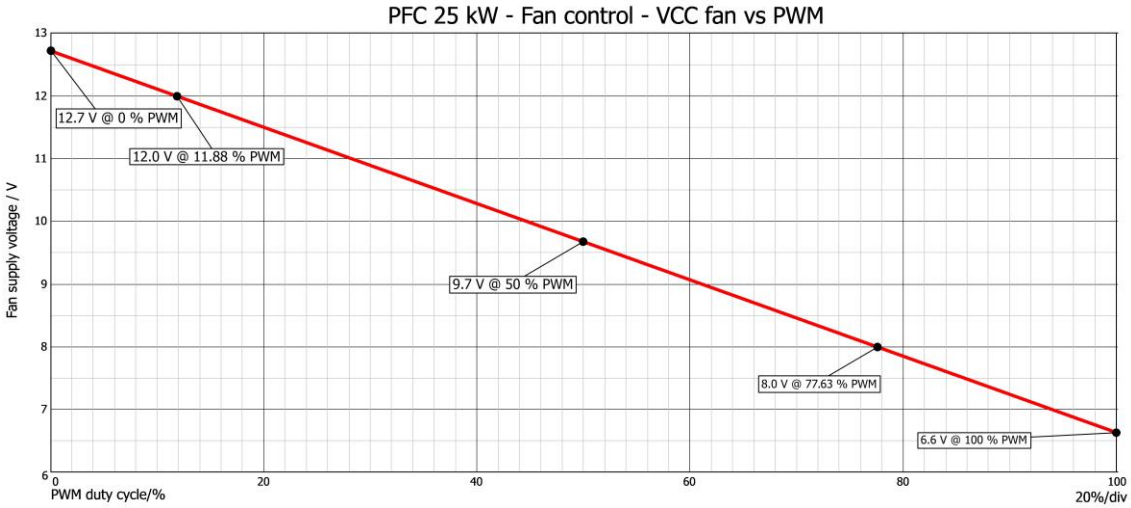

Fig. 16. Output voltage of PWM-to-voltage converter as a function of PWM duty cycle.

The ac characteristics of the control loop were simulated to verify the stability of the PWM-to-voltage converter. To start, the following values were used for the first step of the simulation: Ccomp = 470 pF, Rcomp = 10 kΩ, Cp = 100 pF, R1 = 3.1 kΩ and R2 = 237 Ω.

In the simulation sweep we can observe the moving gain (red) and phase (blue) characteristics of the PWM-to-voltage converter as shown in Fig. 17. The variations in the gain and phase of the converter are shown with the dashed and dotted-dashed lines. The crossover frequency ranges from 32.9 kHz to 51.8 kHz; phase margin, from 26.6° to 31.9°; and gain margin, from 16.5 to 20.5 dB which are not sufficient for stable operation across the whole operating range of the converter.

While most power converters are typically designed to obtain a phase margin of at least 45° to ensure stability, we have targeted a phase margin of 70° for a robust design and therefore the results are not acceptable for a stable circuit.

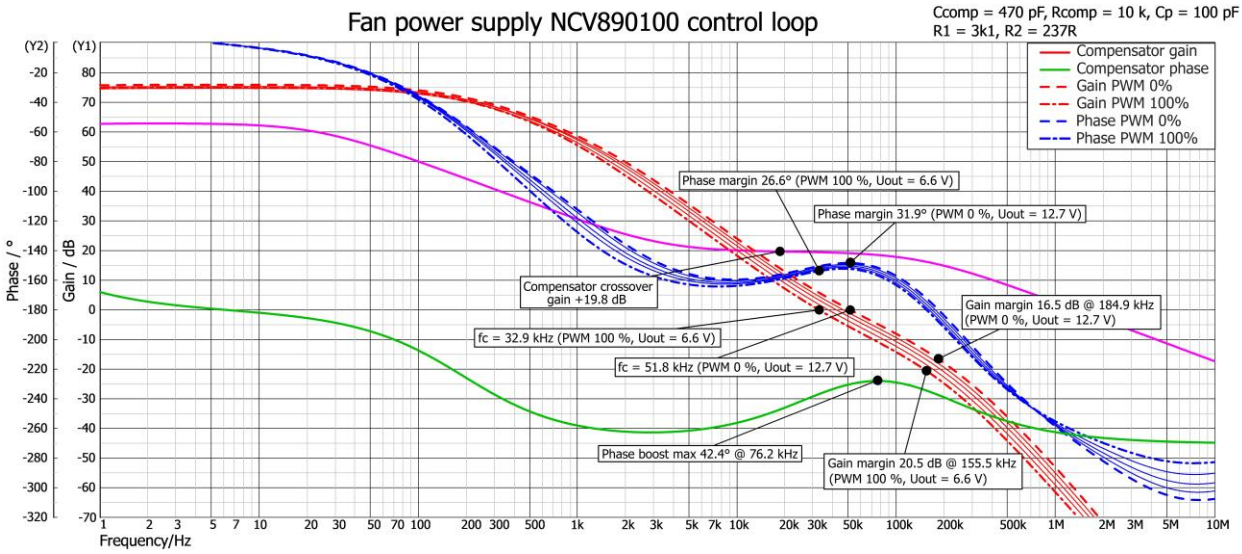

Fig. 17. Simulated control loop ac characteristics of the PWM-to-voltage converter and compensator with starting design values of Ccomp = 470 pF, Rcomp = 10 kΩ, Cp = 100 pF, R1 = 3.1 kΩ and R2 = 237 Ω.

To improve the stability of the PWM-to-voltage circuitry, the compensator was re-designed for three fans connected to the output of converter. Three fan cooling systems are used in the PFC stage and two are used in the dc-dc stage, (plus one extra fan that is reserved for DAB transformer cooling). The compensator was tuned with crossover frequency in the range from 13.5 kHz to 25.3 kHz, which yields a phase margin of 72.2° and a gain margin in the range from 23.6 dB to 27.7 dB for the PWM-to-voltage converter. The compensator is tuned with a maximum phase boost of 71.2° which is in the crossover area. Phase does not decrease significantly below the crossover area.

The final component values for the compensator were set to Ccomp = 10 nF, Rcomp = 4.64 kΩ, Cp = 270 pF, R1 = 3.1 kΩ and R2 = 237 Ω. The simulated control loop characteristics of the PWM-to-voltage converter are shown in Fig. 18.

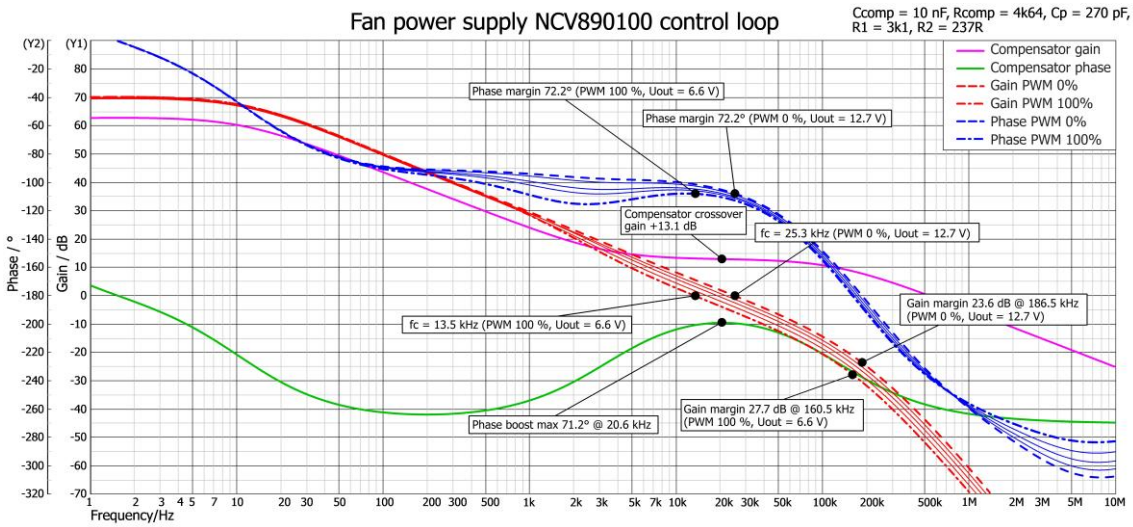

Fig. 18. Simulated control loop ac characteristics of the PWM-to-voltage converter and compensator with final values of Ccomp = 10 nF, Rcomp = 4.64 k Ω, Cp = 270 pF, R1 = 3.1 kΩ and R2 = 237 Ω.

The final schematic of the PWM-to-voltage converter using the NCV890100 buck switching regulator is shown below in Fig. 19.

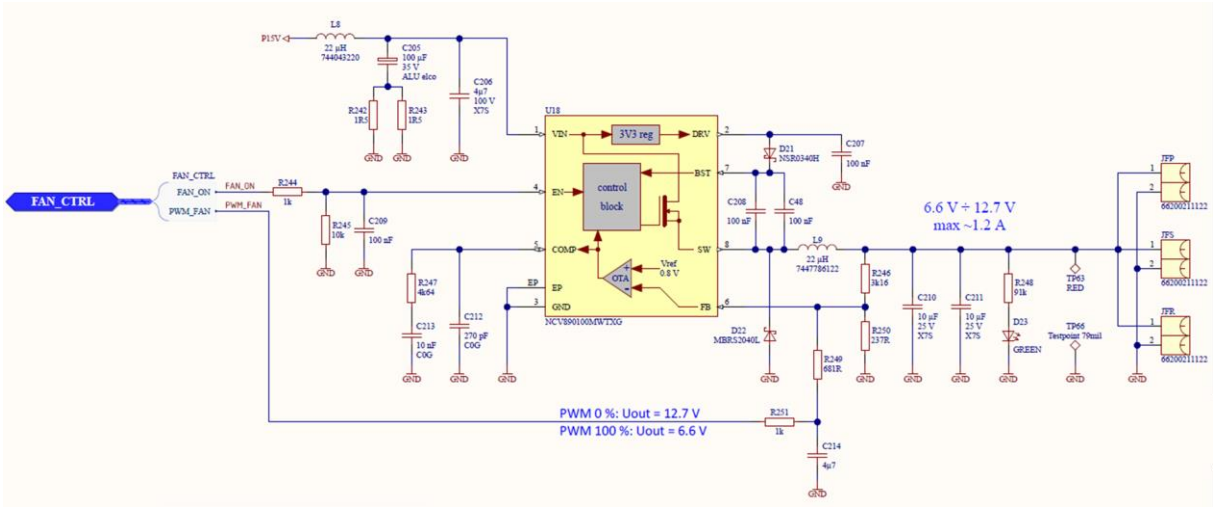

Fig. 19. Final schematic of the PWM-to-voltage converter using the NCV890100 buck switching regulator.

Conclusion

In this article we discussed the thermal assembly advantages of SiC PIM modules versus discrete SiC FETs. With SiC PIM modules we can achieve higher switching frequency operation to help reduce passive component size and provide better heat transfer capability than discrete packages. Modules allow higher power flow capability for the same die value, and improve overall design size. In addition we discussed the advantage of the integrated NTC in PIM modules used in the digitally controlled cooling concept to lower the extensive noise from the cooling mechanism when the charging module is running at low output power levels.

We also discussed the design process and considerations in the development process to achieve three digitally controlled cooling fans in the PFC stage and two cooling fans in the dc-dc stage with an additional one for the DAB transformer. The team is planning to release two additional parts in this article series to discuss lab performance data and design recommendations based on lessons learned when testing the hardware at full 25-kW power.

References

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About The Authors

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For further reading on designing EV chargers, see the How2Power Design Guide, locate the Application category and select "Automotive".