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APEC 2022: GaN Power Devices And Advanced Topologies Are Put To Work In Latest Adapter Designs

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The USB PD Revision 3.1, which was announced last year, pushed the limit on USB power delivery from the previous 100 W maximum up to 240 W of power delivery over a full featured USB Type-C cable and connector. This new power limit, which is referred to as the Extended Power Range, permits use of this popular power standard for charging or powering higher-power applications such as gaming laptops, desktops, work stations, and numerous non-computer products such as power tools, e-bikes and e-scooters. Meanwhile, there are still many products for which the 100-W limit, now dubbed the Standard Power range, is still adequate.

At the recent APEC 2022, the efforts of power semiconductor companies to address these power supply applications were prominently on display as numerous exhibitors showed demos and reference designs of adapters for USB-PD applications. These designs are leveraging GaN power devices—from a growing pool of vendors—together with new topologies and new controllers to create complete solutions for power adapters with higher efficiency and higher power density. For the higher power adapters, GaN is being applied in more of the design including the PFC stage and on the secondary side for synchronous rectification.

Meanwhile, semiconductor companies are not just developing reference designs and demos of smaller and higher-power, single-output adapters, they are also developing multi-output designs for multi-port adapters and wall outlets. This article highlights some of the USB-PD reference designs and demos I saw on display, or heard discussed at APEC. For many of these designs, simplified schematics and photos of demo boards are shown here with key components identified, and efficiency and power density specs highlighted.

65-W Adapters Continue To Evolve

Among adapter designs addressing the USB-PD Standard Power Range, 65-W remains a popular power level as this addresses many smartphone and laptop charger applications. At APEC, **Infineon** showed a demo of a 65-W dual USB type C charger reference design. It was built around three Infineon chips, the PAG1P USB-C power delivery primary start-up controller, the PAG1S USB-C power delivery secondary-side controller (an integrated QR flyback controller for chargers/adapters), and the CCG7D dual-port USB-PD controller along with Infineon CoolMOS high-voltage and OptiMOS low-voltage MOSFETs (Fig. 1).

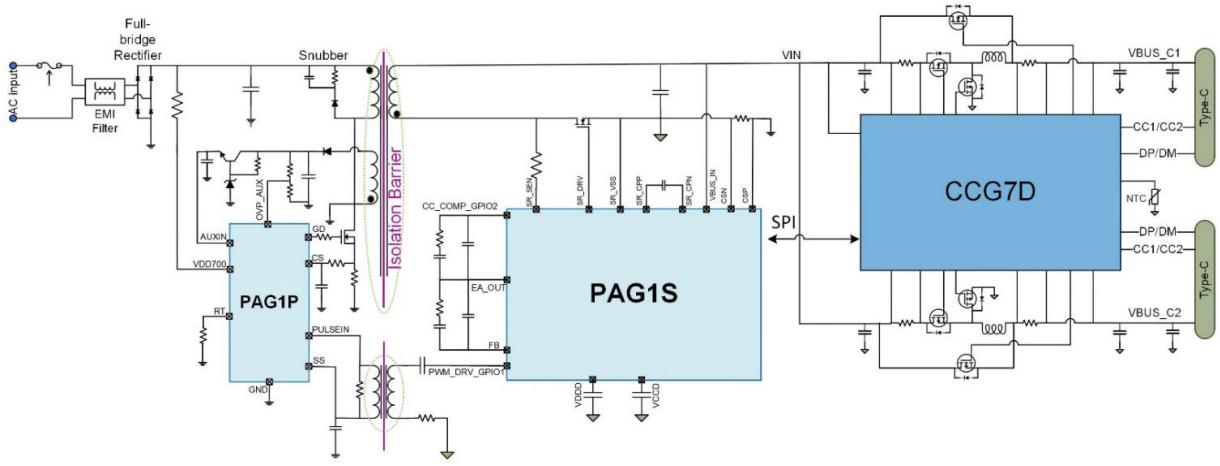
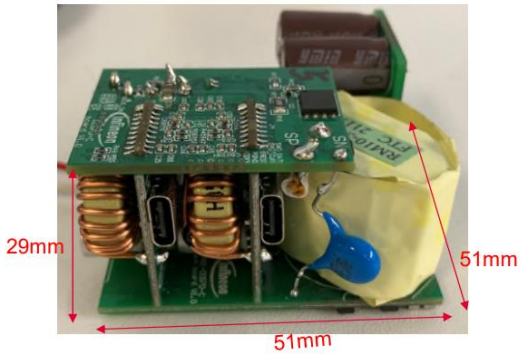


Fig. 1. Schematic for Infineon's 65-W dual type-C PD adapter reference design.

The CCG7D is a dual-port USB-PD controller. So instead of using two controllers in parallel, a single device can be used. This reference design achieves a power density of 14 W/in.^{3} (uncased) and peak efficiency exceeds 90% at high line and 20-V output (Fig. 2).



Featured specs:

Total Power = 65W, Port Power = 65W
Power Density: 14.12 W/in^3
Input Range: 90Vac – 264Vac
Feature: Dynamic load-sharing, Temperature throttling
PWM switching frequency: 20kHz - 150kHz, QR
Meets DoE VI (multi voltage output) standard with 1-2% margin

Infineon Components:

Primary PWM Controller: PAG1P x1
Primary HV Switch: IPL65R195C7 x1
SR Controller and Flyback regulation: PAG1S x1
SR MV Switch: BSC042NS x1
PD Controller + Buck Converter: CCG7D x1
Buck converter LV switch: BSZ063N04LS6 x4
VBUS LV Switch: BSZ0902NS x2
ESD Components: ESD245 x8, ESD239 x2

Fig. 2. Like many of the adapter demo boards, the one for Infineon's 65-W dual USB type C charger reference design actually combines multiple boards to achieve the high density called out here in the featured specs. Infineon's components are also identified here.

Nihit Bajaj, Infineon's Sr. applications marketing manager, noted that the addition of the buck converter in the dual-port adapter design adds a third stage of power conversion versus the two stages required in a single-port design. So that necessarily reduces efficiency versus single-port designs. He also observed that the tricky part of designing multiport adapters is implementing dynamic current sharing between the different ports, a distinctive feature of the CCG7D.

For the 65-W dual USB type C charger reference design a complete evaluation board is available for order. It offers passing EMI specs and meets the DoE level VI (multi-voltage output) standard for efficiency with 1% to 2% margin (Fig. 3). This reference design follows in the footsteps of the company's 45-W dual-port design for use in adapters and wall outlets.

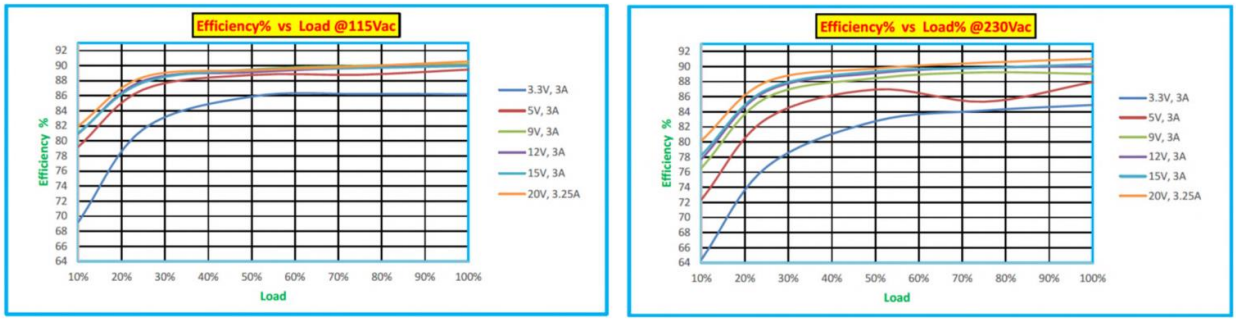


Fig. 3. Most adapter designs feature universal input range. Efficiency of Infineon's 65-W dual type-C PD adapter reference design is shown here for 115 Vac (left) and 230 Vac (right) input.

Testing The Limits Of GaN And Different Topologies

Meanwhile, **Infineon** also showed a 240-W design that represents a technology demonstrator rather than a finished reference design. It was intended to push the limits of the company's technology by applying new topologies. This is a dual-port design with up to 48-V output for USB PD and operation from a universal input voltage range. The design is flexible in terms of current sharing.

It achieves a power density of 42 W/in.^{3} uncased and 24 W/in.^{3} cased. It features an all-GaN design in terms of the power switches except for the CoolMOS MOSFETs in the low-frequency leg of the totem-pole PFC, employs a dc transformer, and ZVS in all stages including the totem-pole PFC. The PFC switches at 400 kHz, using essentially CCM control.

According to Infineon's Sr. staff engineer of Power Electronic Systems Innovation, Jon Azurza, the company looked at different topologies and system partitioning to develop this design. The biggest challenge was in handling the wide voltage ranges on both the input and output, said Azurza. The input operates from the universal input range of 90 to 265 Vac while the output must operate over the USB PD range of 5 to 48 V. The next step for Infineon will be to develop a complete reference design based on this technology demonstrator. Applications for this power supply design include power tools and e-bikes.

Among its demos, **Innoscience Technology** showed two all-GaN adapter designs featuring the company's own high-voltage and low-voltage GaN devices. One was a 140-W USB-PD 3.1 adapter consisting of a CRM totem-pole PFC and an asymmetrical half bridge (AHB), which switches at 300 kHz. This design is all GaN except for the diodes used in the line frequency leg of the PFC (Fig. 4).

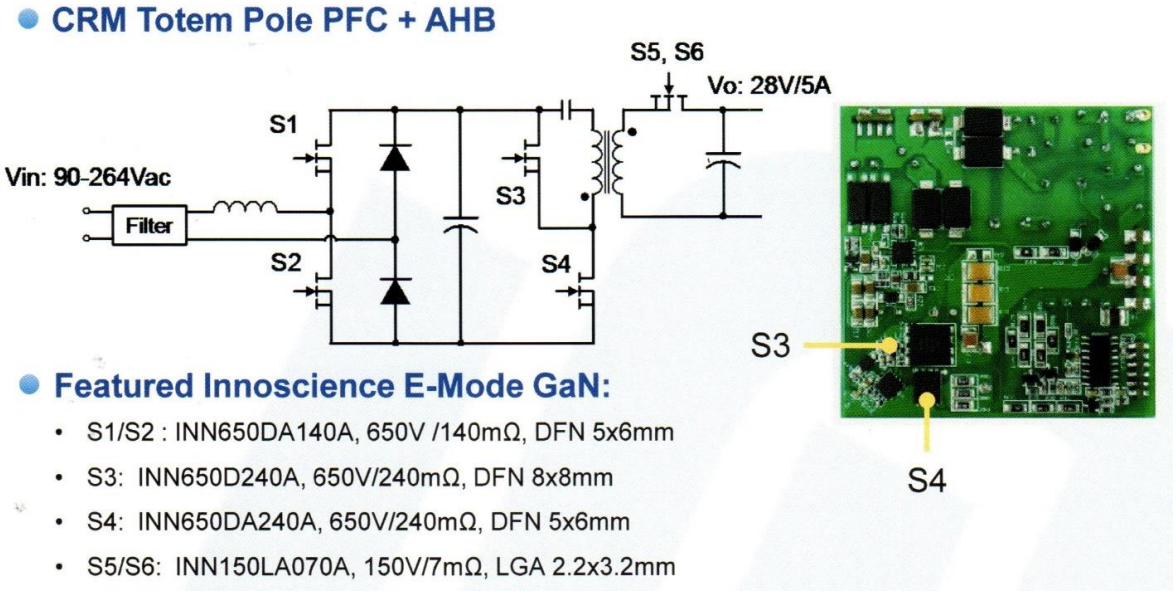


Fig. 4. Innoscience's 140-W USB-PD 3.1 adapter switching at 300 kHz. The power stages are identified in the simplified schematic with the GaN device part numbers identified below.

This is a complete reference design that has passed EMI requirements. It achieves 95.2% efficiency at high-line (230 Vac) input and 28-V out, which is said to be 2% higher than an equivalent silicon design (Fig. 5). According to Innoscience, with its 29 W/in.^{3} power density (uncased), this 140-W reference design provides a 30% size reduction when compared to the adapter currently used to power the Apple MacBook Pro. That adapter is said to switch at a lower frequency and use only a partially GaN design.

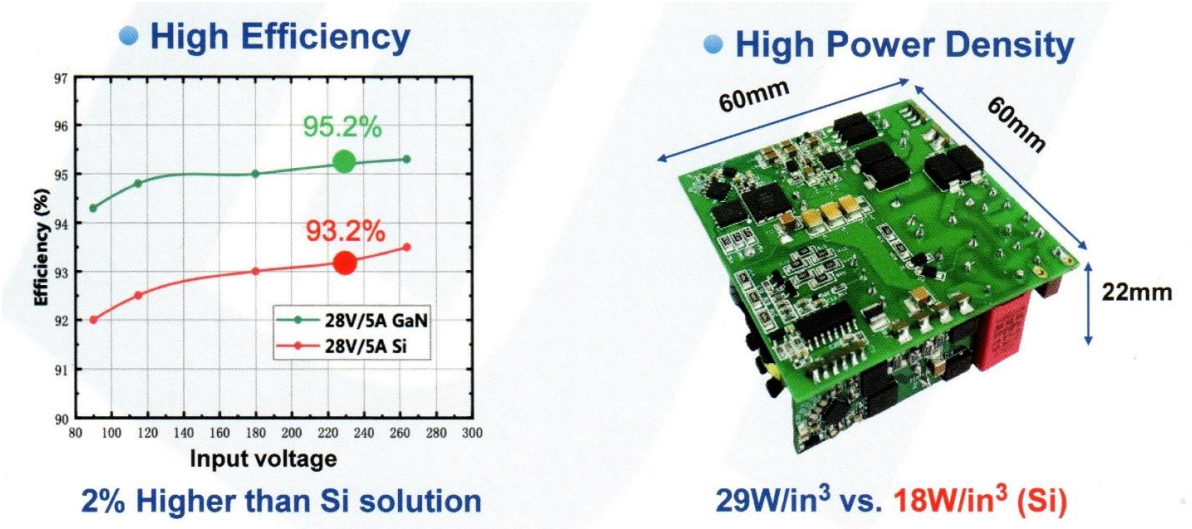


Fig. 5. Innoscience's 140-W USB-PD 3.1 adapter's measured efficiency (left) and demo board (right).

Another Innoscience demo was a 240-W 350-KHz ac-dc adapter based on a CRM totem-pole PFC and LLC half-bridge converter. Operating from a universal input, this design produces a 48-V 5-A output. This reference design differs from the 140-W version in a couple of ways. First, the PFC stages uses all GaN power switches even in the line-frequency leg. Secondly, the dc-dc stage is an LLC half bridge (Fig. 6).

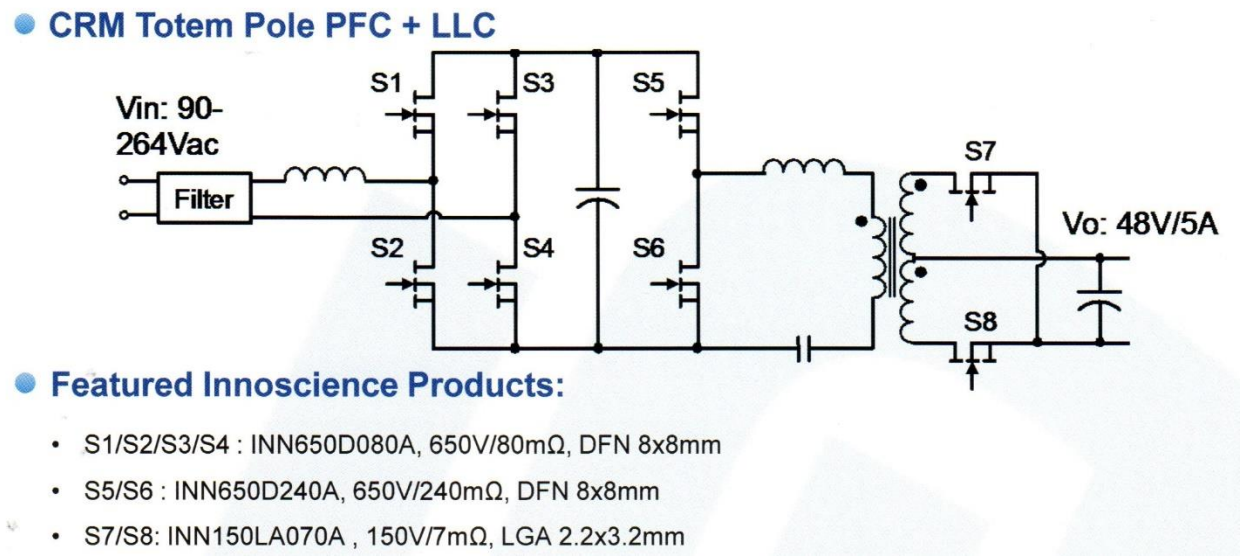


Fig. 6. Innoscience's All-GaN 240-W 350-kHz ac-dc adapter simplified schematic.

According to the company, this design achieves a 96.7% efficiency at nominal high-line input, which is said to be 2% higher than an equivalent silicon-based solution. With an uncased implementation measuring 85 mm x 58 mm x 20.5 mm, this all GaN 240-W adapter design achieves a power density of 38.5 W/in.^{3} versus 11 W/in.^{3} for an equivalent silicon design, according to the company (Fig. 7).

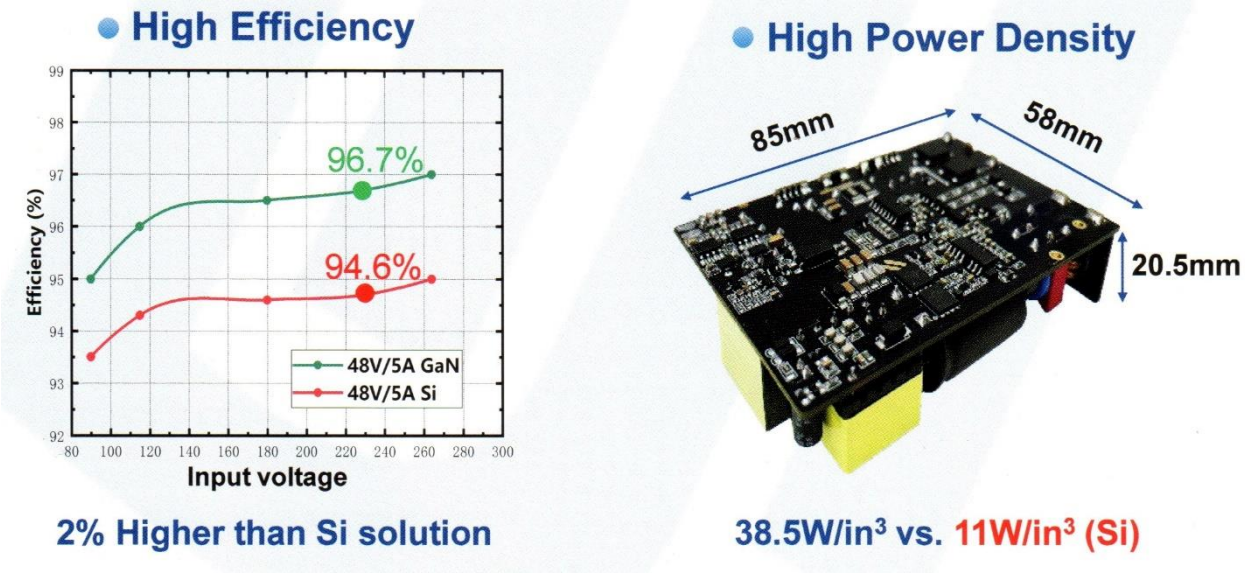


Fig. 7. Innoscience's All-GaN 240-W 350-kHz ac-dc adapter's measured efficiency (left) and demo board (right) with power density highlighted.

At its booth, **Efficient Power Conversion (EPC)** announced and demo'd another all-GaN 240-W USB-PD 3.1 fast charger reference design. This design combines low-voltage GaN FETs from EPC, with high-voltage GaN power stages from Navitas.

The evaluation board converts a universal ac input to an adjustable dc output voltage from 15 V to 48 V. It achieves a power density of about 1.3 W/cm^3 (uncased) (or 21.6 W/in.^{3}) by employing GaN power switches operating at high switching frequencies in both the primary and secondary circuits (Fig. 8).

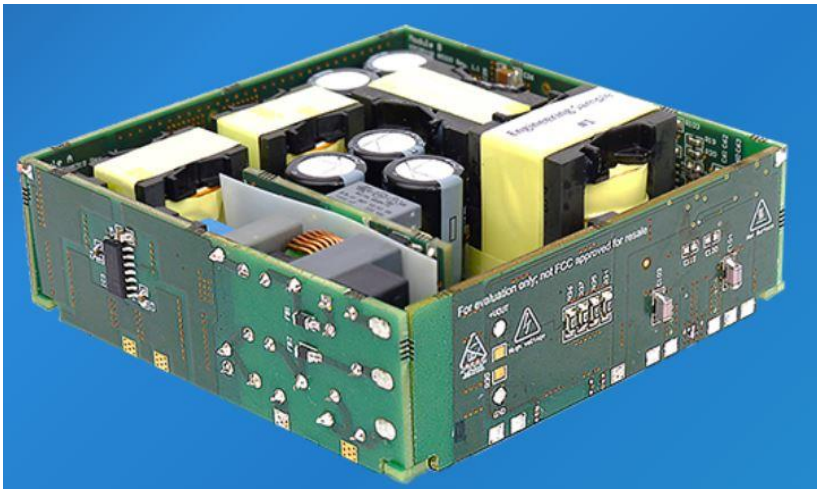


Fig. 8. The EPC9171 kit is a 240-W USB-PD 3.1 ac-dc adapter reference design board employing GaN power switches in both the primary and secondary circuits. Measuring, 83.7 x 83.7 x 26 mm (3.30 x 3.30 x 1.02 in.), it achieves a power density of 21.6 W/in.^{3} or 1.3 W/cm^3 (uncased).

The EPC9171 design consists of a two-phase interleaving boost converter power factor correction (PFC) stage and an isolated LCC resonant power stage. Unlike the well-known LLC resonant power stages, which suffer from limited output voltage range, the LCC resonant converters are well suited for wide-output-voltage-range multi-point applications. This solution provides a higher power density than a conventional, three stage design typically consisting of active PFC, LLC and buck power stages, according to EPC.

For the PFC stage in the EPC9171, GaN power switches operate well above 200 kHz (using critical conduction mode (CrCM)) allowing physically small PFC inductors. The LCC resonant converter, which also uses GaN power switches, operates in the frequency range of 350 to 580 kHz, which helps to reduce the size of the power transformer as well as that of the other passive components in the resonant circuit.

The synchronous rectifier stage employs a pair of 100-V-rated, 3.2-mΩ EPC2218 GaN FETs on the secondary side of the LCC stage. The GaN FETs are driven by fast synchronous rectifier controllers to minimize the losses over the whole output voltage and current range and allow a simple yet effective thermal design. Meanwhile, a pair of 650-V NV6128 GaNFast power stages from Navitas are used in the primary circuit of the LCC resonant converter, and a pair of the same devices are used in the PFC stage. Fig. 9 charts efficiency under low-line and high-line conditions at various output voltages.

With 240 W of power, this solution can be adopted not only for ultra-fast USB charging for laptops, notebooks, and smartphones, but can extend USB charging to other applications requiring 240 W, such as gaming PCs, eBikes, and eScooters. As the cost for 48-V batteries continues to decrease, additional applications for ac-dc charger applications are emerging.

The EPC9171 evaluation board is priced at $1,440 each and is available for immediate delivery from Digi-Key.

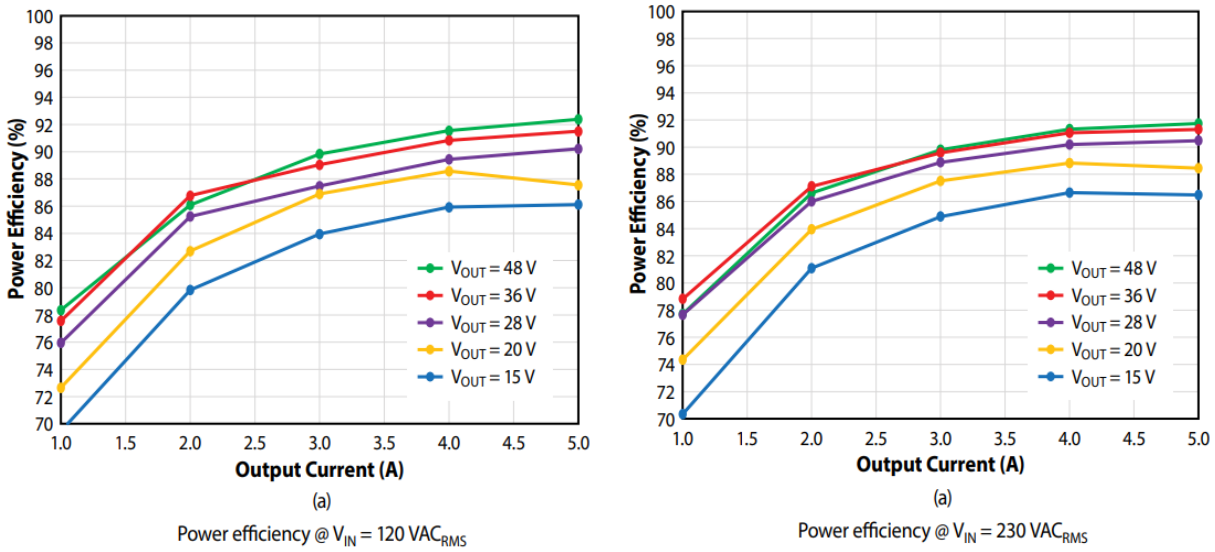


Fig. 9. Typical efficiency of the EPC9171 240-W USB-PD 3.1 ac-dc adapter reference design at various output voltages with Vin = 120 Vac (left) and Vin = 230 Vac (right).

A Proprietary AC-DC Architecture

Eggtronic introduced SmartEgg, the latest member of its EcoVoltas family of high-efficiency ac-dc architectures. SmartEgg is a zero voltage switching (ZVS) solution for power applications in the 75- to 1-kW range that need both output voltage regulation and power factor correction (PFC). According to the vendor it enables much higher no-load-to-full-load efficiency and a 50% smaller bill of materials (BOM) than conventional converters, while significantly increasing the power density and reliability of ac-dc converter designs. It is also said to be one of the first platforms to support the new USB PD Revision 3.1 specification delivering up to 240 W of power over full featured USB Type-C cables and connectors.

Traditional medium-power ac-dc PFC architectures employ a boost PFC input stage and an LLC stage that controls the output voltage. SmartEgg halves the number of MOSFET and magnetic components required by replacing these two stages with a single-stage converter capable of controlling both input current and output voltage (Fig. 10).

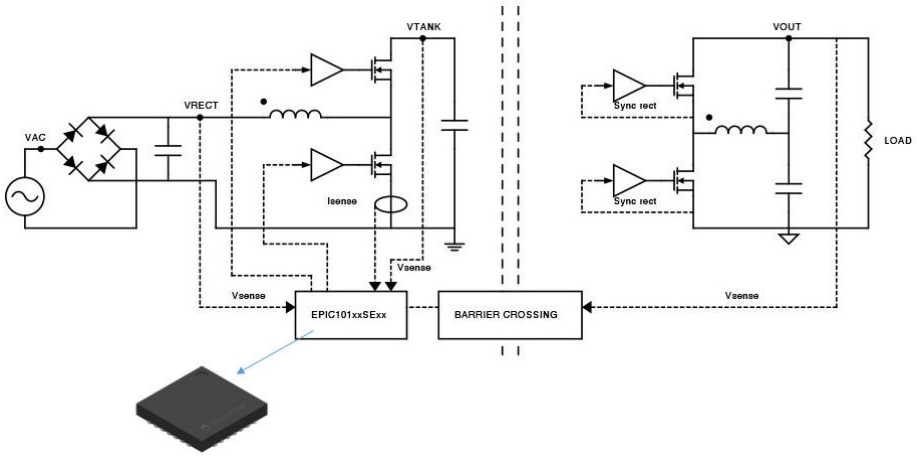


Fig. 10. The SmartEgg ac-dc architecture performs power factor correction and isolated voltage regulation in a single stage. By forcing ZVS under all conditions, it achieves very high efficiency across the load range, very high power density and a reduced bill of materials. Implementation of this architecture depends on a proprietary controller, the EPIC101AGSE01 32-bit controller.

SmartEgg consists of an input rectifier (Eggtronic offers solutions based on either an input bridge or bridgeless rectifier), two primary FETs, two secondary FET rectifiers, a single magnetic component and a few capacitors. The main controller manages PFC and output voltage regulation, ZVS and frequency control.

Forced ZVS under every load condition delivers efficiencies of up to 95% at full load and 92% at light load. Its magnetic component is a custom device with a high amount of leakage inductance. Because little energy is stored in this component (the converter can be modeled as a forward converter), the transformer can be small. Fig. 11 depicts a 150-W implementation of the SmartEgg architecture. However, the demo shown at APEC was a 230-W version with a single fixed output.

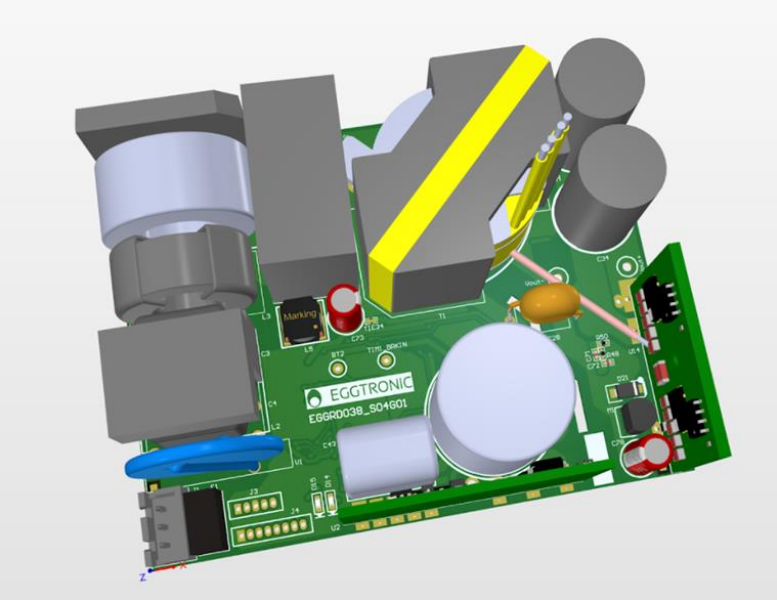


Fig. 11. A 150-W implementation of the SmartEgg ac-dc architecture is depicted here. It measures 80 x 62 x 28.2 mm (uncased) which equates to a power density of 17.6 W/in.^{3}. It passes EMI worldwide.

Eggtronic engineers can create custom designs based on the new SmartEgg architecture or they can provide the reference design together with the required IC controller. Output options are fixed-voltage, CC/CV battery charger, and USB PD 3.1. The first fixed-voltage reference design is available now, with a multi-port USB-PD-3.1-compliant version coming in May.

Silanna Semiconductor, which did not have a booth at APEC, did discuss their APEC-timed announcement of the company's first multi-port fast charger reference design, the AnyPort RD-5, at the conference along with some reference designs that were being shown by partner companies. In the case of the RD-5, this all-silicon design combines the company's CO_2 Smart Power families of ACF controllers and high-frequency dc-dc converters to create a high-power-density, ultra-efficient, production-ready solution for multi-port 65-W USB-PD applications (Fig. 12).

Fig.12. Silanna Semiconductor's AnyPort RD-5 multi-port fast charger reference design is pictured here.

The design provides a cased power density of 11.4 W/in.^{3} and operates with an end-to-end peak efficiency in excess of 91.5%. It also achieves >6 dB conducted and radiated EMI margins. For more information, see https://powerdensity.com/reference-design/.

According to Mark Drucker, CEO, the company is also working with two GaN partners, GaN Systems and Transphorm, to develop higher-power multi-port fast charger reference designs with both type A and type C ports.

These include the RD-16 100-W 2C1A multi-port USB-PD reference design using GaN Systems' GaN FET and the RD-25 118-W 1C1A multi-port USB-PD reference design using Transphorm's GaN FET. These reference designs were displayed at GaN Systems' and Transphorm's APEC booths, respectively.

Unlike their 65-W RD-5 reference design, which is a two-stage design, the RD-16 and RD-25 are three-stage designs due to the requirement for PFC above 75 W. (See Figs. 13 and 14 for more on RD-16.) They include Silanna Semiconductor's active-clamp flyback ac-dc controller (SZ1131) and high-frequency buck converters (SZPL3102 and SZDL3105) and use GaN devices in both the PFC and ACF stages for delivering best-in-class efficiency and power density, according to the vendor.

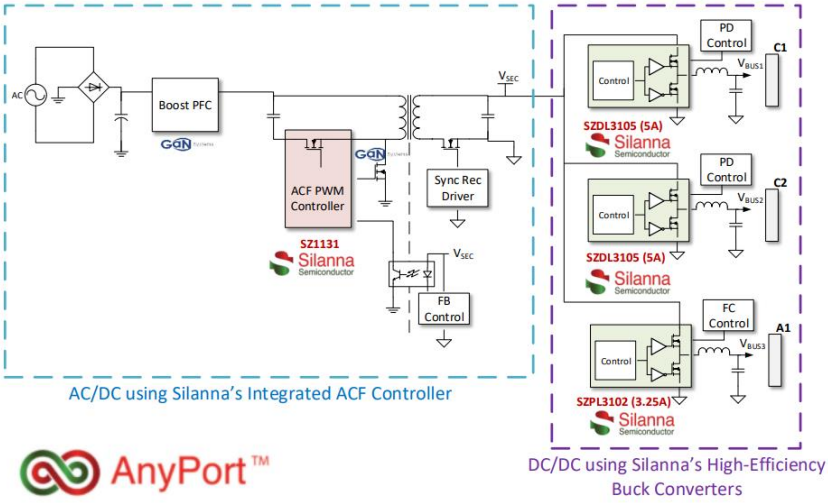


Fig. 13. Simplified schematic for Silanna's RD-16 100-W 2C1A multi-port USB-PD reference design using the company's ACF controller and buck converters in combination with GaN Systems' GaN FET. (See https://powerdensity.com/wp-content/uploads/2022/03/RD-16-v2.pdf).

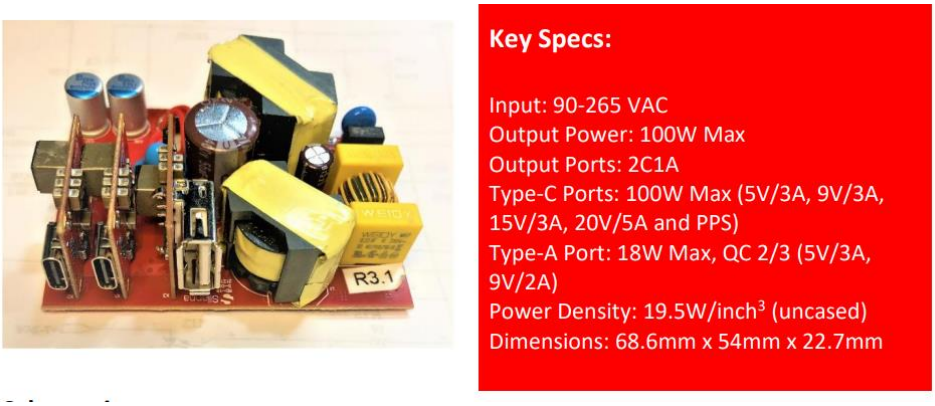


Fig. 14. A demo board for Silanna's RD-16 100-W 2C1A multi-port USB-PD reference design is shown here along with some key specs.

Silanna reports that it is currently optimizing these designs before releasing them in the coming weeks with full test reports. Efficiency and power density numbers will be announced through the PR and test reports at that time.

Although not a multi-port design, during the APEC timeframe, Silanna in combination with smart socket outlet specialist Smarter Living announced what they describe as the world's smallest 65-W in-wall GaN fast charger. Measuring just 42 mm x 42 mm x 30 mm, the 3510PDFE charger is built around Silanna's SZ1131 ACF controller and is the first in a series of small-form-factor wall sockets that Smarter Living will be providing for global markets.

Smarter Living's 3510PDFE 65-W charger provides a single USB output, delivers power delivery (PD) voltage outputs of 5 V, 9 V, 12 V, 15 V and 20 V and supports Programmable Power Supply (PPS) charging. It features 93.5% peak efficiency and <20-mW no-load power. Note that this adapter is designed to accommodate just the European mains range of 220 to 250 Vac, though the SZ1131 ACF controller itself works over a universal input range. For more information, see the press release.

Novel Control Chips With GaN

In its press conference at APEC, **Power Integrations** introduced new PFC chips and secondary-side converter and controller chips that can be combined to build adapter designs that deliver up to 220 W continuous without heatsinks. These new devices include a family of high-efficiency quasi-resonant PFC ICs with a 750-V GaN switch, the HiperPFS-5. With efficiency of up to 98.3%, the HiperPFS-5 ICs deliver up to 240 W without a heat sink and can achieve a power factor of better than 0.98.

The company also announced the HiperLCS-2 chipset, an IC family that simplifies the design and manufacture of LLC resonant power converters. The new dual-chip solution features an isolation device with a high-bandwidth LLC controller, synchronous rectification driver and FluxLink isolated control link, alongside a separate half-bridge power device utilizing Power Integrations' 600-V FREDFETs with lossless current sensing and high- and low-side drivers.

The HiperLCS-2 devices operate at high efficiency across the load range with dissipation so low that direct heat transfer through the FR4 PCB is sufficient, eliminating heatsinks in adapter designs up to 220 W continuous output with up to 170% peak power capability.

Although a USB-PD 3.1 reference design was not specifically called out or shown in their presentation, in their materials they noted that HiperPFS-5 ICs are well suited for use in high-power USB PD adapters as well as TVs, game consoles, all-in-one computers and appliances (Fig. 15).

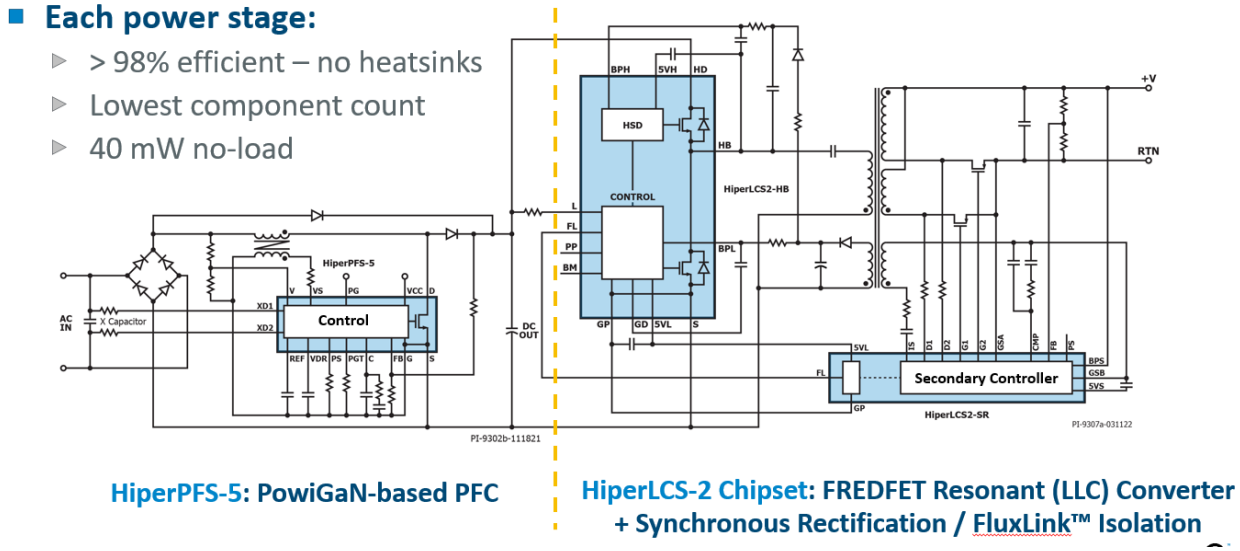


Fig. 15. With the introduction of its HiperPFS-5 PFC chip with built-in GaN switch and its HiperLCS-2 chipset combining a FREDFET resonant (LLC) converter and a synchronous rectifier with in-package isolation, Power Integrations enables design of compact, low-parts-count power supplies with single power outputs exceeding 200 W with no heatsinks.

As Edward Ong, senior product marketing manager at Power Integrations, observed, a HiperPFS-5 PFC IC can be paired with the HiperLCS 2 chipset, or the company's InnoSwitch4-CZ active-clamp flyback ICs, to build power supplies that "can easily beat even the most aggressive efficiency regulations while cutting the bill of materials by half and achieving extremely attractive form factors for ultra-fast chargers." (See Fig. 15 again and Fig. 16).

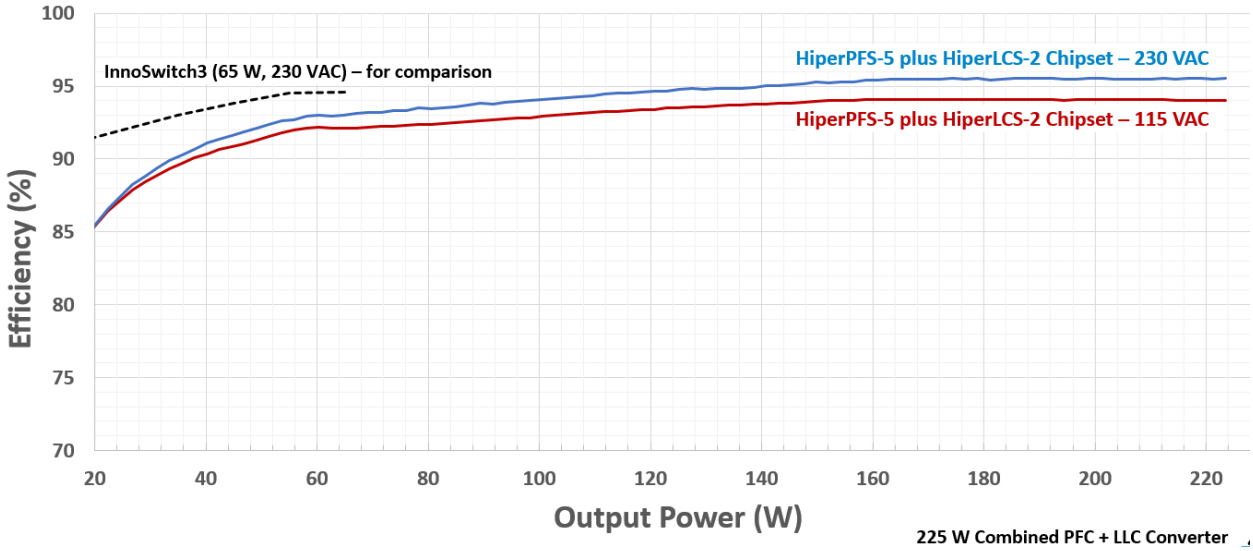


Fig. 16. A combined 225-W PFC plus LLC converter based on the HiperPFS-5 PFC chip and HiperLCS-2 LLC converter and synchronous rectification/isolation chipset achieves in excess of 95% efficiency at high-line input and an output voltage of 24 V.

(For more on the HiperPFS-5 and HiperLCS-2 devices, see the articles "Quasi-Resonant PFC Chips With GaN Switch Shrink PFC Stage For Adapters" and "Chipset Boosts LLC Converter Efficiency, Slashes Component Count," which also appear in this issue of the newsletter.)

While the adapter design proposed using the HiperPFS-5 and HiperLCS-2 ICs shows a single-output design, in the weeks following APEC, Power Integrations announced a reference design for a "Multi-Port USB-C Wall Outlet Without Buck Converters". This design is based on the company's InnoSwitch3-Pro ICs.

The DER-916 design example from Power Integrations describes a 65-W wall outlet featuring current sharing between two USB type-C ports, connected to dual InnoSwitch3-Pro flyback switcher ICs. The PowiGaN-based devices result in a compact design that requires no heatsinks or dc-dc converters and achieves 92% end-to-end efficiency (Fig. 17). For more information see the DER-916 design example report.

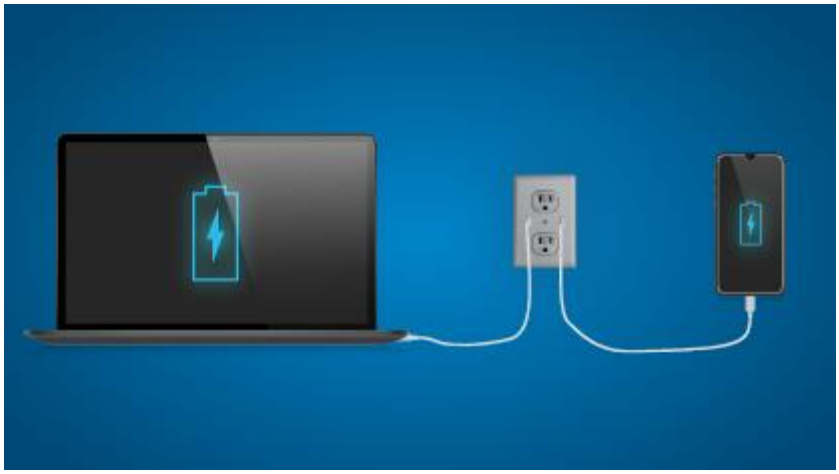


Fig. 17. Two InnoSwitch3-Pro ICs connect through a low-pin-count USB-PD controller and dynamically adjust output voltage and current. For example, when a laptop is plugged into either of the two ports, it can be charged at 65 W. When a mobile phone is then plugged into the other port, it can be charged at 20 W while the laptop is automatically adjusted to 45-W charging.

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