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# Designing An Open-Source Power Inverter (Part 3): Power-Transfer Circuit Options

*by Dennis Feucht, Innovatia Laboratories, Cayo, Belize*

Previous parts of this series discussed system-level goals and specifications[1] for this design and system-level design considerations[2] such as the impact of battery selection, output waveshape, and circuit performance parameters of interest—mainly current form factor. In this part, various candidates for the inverter's converter-stage power-transfer circuit are reviewed, the optimal circuit is chosen, and design equations are developed for it.

However, the discussion ventures a bit broader and deeper than that. Although this Volksinverter design assumes a two-stage scheme consisting of a battery converter (a stepup dc-dc converter) and an inverter (a PWM'd H-bridge), we will explore other possible alternatives to this scheme.

For example, this discussion begins by considering some alternatives involving the inverter stage, which can eliminate a storage capacitor on the battery converter output in one case (the waveform generator option), or replaces the H bridge with another converter, offering the possibility of a more streamlined and efficient design for the complete power inverter (the differential waveform generator).

From there, the push-pull, boost push-pull, and SEPIC topologies are considered as options for the battery converter stage, leading to a more-detailed comparison of push-pull versus SEPIC. Limitations of the boost push-pull as a waveform generator are then explored.

While an *optimal* power-transfer circuit is identified as such fairly early in the discussion, the analysis of power-transfer circuit options does not end there for two reasons. One is that detailed comparisons of the different circuit options (topologies) is needed for designers to have confidence in the selected circuit. (It's important to understand the benefits and limitations of options not chosen).

Secondly, this discussion is meant as a general tutorial on how to evaluate power transfer circuits for power inverter applications, not just for the Volksinverter. Beyond those rationales for the broader discussion, the analysis lays the foundation for possible adjustments in the Volksinverter design in later parts of this series in order to achieve a more-optimum design.

## Conventional Two-Stage Converter-Inverter

The power-transfer circuit scheme of the Volksinverter is shown in Fig. 1.[1]

A two-stage system minimizes the input-current form factor, $\kappa_g$, which was discussed in part 2,[2] by charging a storage capacitor between converter and inverter stages. The inverter stage is of H-bridge design and can be PWMed to generate the output waveform.

The two-stage scheme is typical of low-cost commercial inverters that output bipolar square-waves. Their inverter stage is not PWMed to produce a sine waveshape but is switched on and off each half-cycle by a 50-Hz or 60-Hz digital oscillator to produce the correct duty-ratio *D* relative to the square-wave amplitude, as shown in part 2 and repeated here in Fig. 2. An improvement incorporated in this design increases the inverter-stage input voltage to the sine-wave amplitude (peak value) and the H-bridge is PWMed (using two-quadrant PWM drive) to produce a sine waveform.

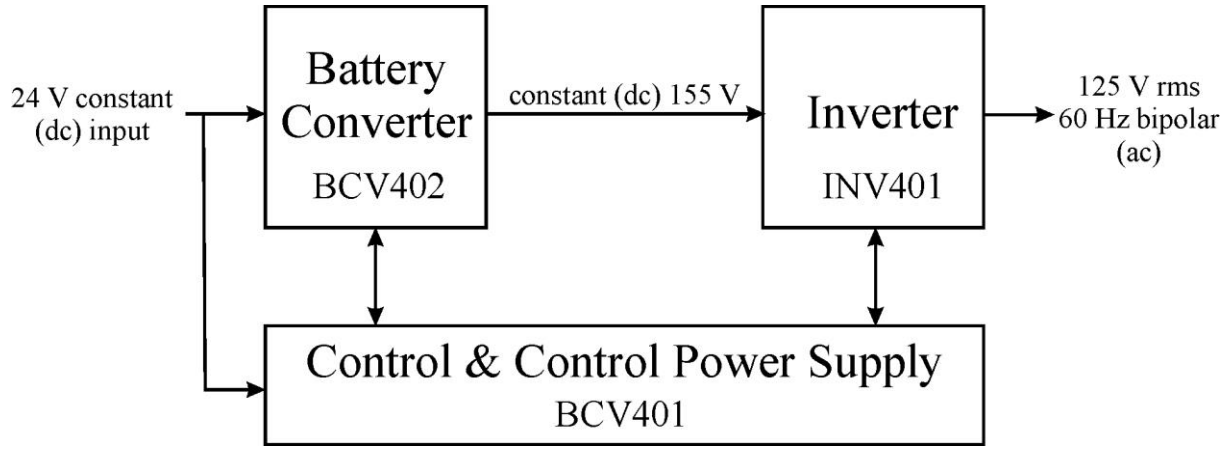


*Fig. 1. Two-stage power transfer inverter design. Three subsystems are the battery converter power-transfer circuit that raises the battery voltage to the peak output voltage of 155 V, the power-transfer inverter circuit that generates by PWM the bipolar third-harmonic sine-wave (3HSW) output waveform of 125 V rms, and the power-transfer control and protection circuits with their own low-voltage power supply. The three Volksinverter subsystems have been implemented in modular fashion as circuit-boards, with module designations (BCV402, INV401, and BCV401) shown in the blocks.*

An advantage of the two-stage scheme is that it can be optimized to minimize input current ripple. The lowest-$\kappa_g$ input circuit is used to charge the interstage storage capacitor. The inverter stage then exhibits the degraded $\kappa$ in generating the output waveform. The storage capacitor isolates the peak currents of the inverter stage from the input, thereby reducing the input-current ripple requirement.

Storage capacitance $C_o$ must be large enough to keep the converter from following the output current waveform, thereby defeating the interstage-storage advantage. It must be large enough to supply current over more than one cycle of output so that the feedback-loop bandwidth of the converter does not respond appreciably to cyclic changes. A large $C_o$ requires space and cost, and conflicts with sourcing sine-squared current from $V_g$; a tradeoff is created in choosing the $C_o$ value.

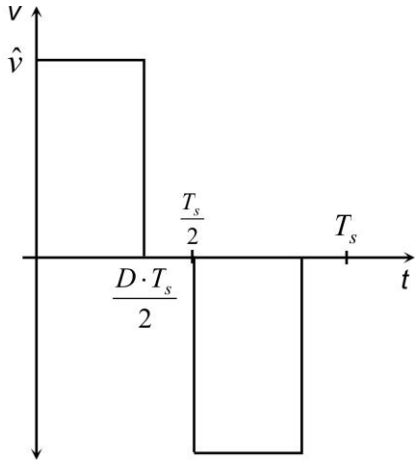


*Fig. 2. One cycle of a symmetric bipolar square-wave, misnamed a "modified sine wave" in commercial literature. It is not a modification of a sine wave but is more easily and cheaply generated than a sine wave.*

### *Two-Stage Alternative: Waveform Generator And H-Bridge*

Because the converter (i.e. the battery converter shown as the first stage in Fig. 1) is PWMed for control, it can be PWMed to produce the waveshape of the output waveform, and $C_O$ eliminated. In a functionally modified two-stage scheme, the converter PWM controller generates a sine-magnitude (rectified sine wave) output. It is input to the inverter H-bridge that switches in synchronism with its zero-crossings.

This scheme PWMs the converter to produce a unipolar (magnitude) output waveform of the desired waveshape. It lacks the low $\kappa_g$ of the two-stage scheme described in the previous section in that sine-squared current is input. If the input current is not a design constraint, its advantage is a simplified inverter stage—an H-bridge that need only switch polarity in synchronism with the zero-crossings of the output waveform. This single zero-crossing waveform can be easily isolated from the battery-side ground and no additional control circuitry is required on the output side.

### *Another Alternative: Differential Waveform Generator*

If the inverter stage is traded for a second converter operating differentially with the first, and without storage capacitors, the converters become power amplifiers driven by PWM waveforms. A MOSFET switch to ground at the output of each converter is required for bipolar operation. Output sine-magnitude waveforms are synchronously sunk by the other converter during each half-cycle of waveform generation, as shown in Fig. 3.

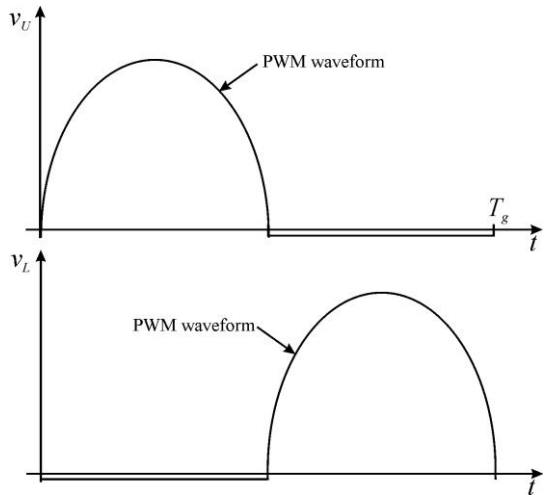


*Fig. 3. Outputs of a differential PWMed waveform generator. The opposing sides of the differential circuit are push-pull converters without output capacitors, having instead a switch conducting to ground while the other side generates a PWM waveform. The power-line output terminals float relative to circuit ground, as in H-bridge inverters.*

No additional H-bridge inverter stage is required and the output switches are ground-referenced and have simple gate drivers. This H-bridge-less inverter power-transfer scheme has the disadvantage when compared with the previously described two-stage converter-inverter scheme—of drawing a sine-squared input current if generating a sine-wave output. Its advantages are fewer components and greater potential efficiency. This scheme might be the optimal inverter scheme in simplicity, and possibly also in reliability.

### *Battery Converter Options: Push-Pull And Boost Push-Pull Power-Transfer Circuits*

A key design challenge for low input-voltage inverters is the low converter input resistance. The constraining variable is the input current. For an inverter design with a full-scale (fs) input power, $\overline{P}_g$ = 1200 W and a minimum input operating voltage of 20 V, then the maximum average input current is 60 A. An inverter loss of 36 W at full output power results in efficiency, $\eta$ = 97 %. A constant times an average is average power;

$$\overline{P} = V \cdot \overline{i} = \overline{v} \cdot I$$

At 60 A, not only must the wiring be substantial, fuses must be large or paralleled, MOSFETs must have low $r_{on}$ and board traces must be thick, usually covered with a layer of solder. A low-resistance converter power-transfer circuit is needed to minimize losses. Topologies better suited for high-resistance inputs, such as full-bridge, half-bridge, or series-forward converters, have excessive series resistance. A single power switch in the high-current loop is desired.

The converter topology commonly found in battery-input inverters is the push-pull circuit, a differential circuit with waveforms shown in Fig. 4. A PWM-switch CP (buck) circuit has an output inductor and is not optimal because the conducting primary winding has the input voltage, $V_g$ across it and requires a turns ratio, $n = N_p/N_s$ that is smaller to achieve the required output on-time voltage of $V_s$ which is then reduced across the inductor. A smaller $n$ for the same transformer power rating results in less output current. The primary-winding series switches alternate each switching cycle in conducting while the other remains off with $2 \cdot V_g$ across it.

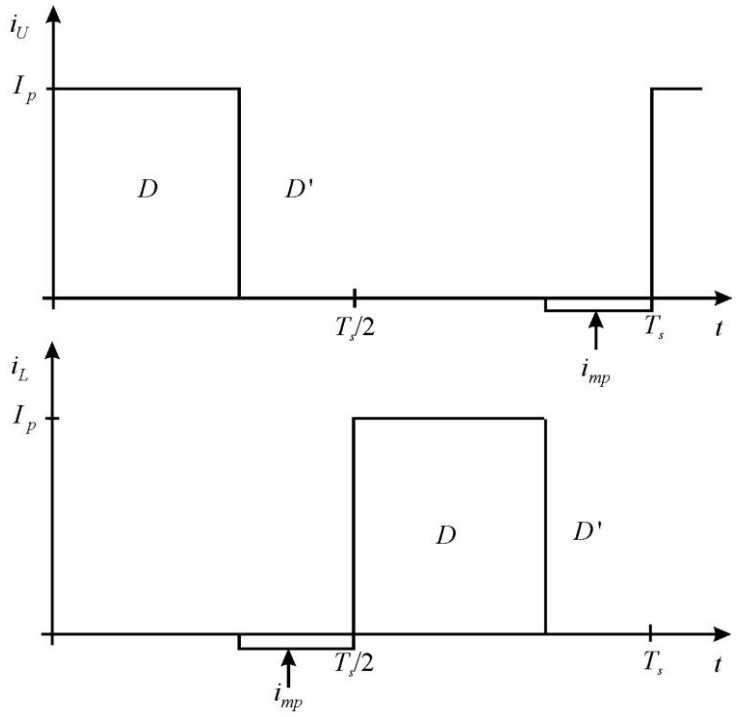


*Fig. 4. Push-pull switch currents. During off-time, $D' \cdot T_S$ magnetizing current, $i_{mp}$ from the conducting switch that shuts off transfers to the non-conducting switch and flows in reverse through its body-drain diode.*

Without $L$, the resulting circuit is a *chopper*, and output current demand is propagated immediately back to the input circuit. Chopper currents are only limited by parasitic series inductance and resistance which are generally wide in tolerance and not an easily controllable aspect of the design. Good design practice is to not have circuit behavior depend on parasitic elements.

The optimal choice for power transfer is the *boost push-pull* (BPP) transfer circuit shown in Fig. 5. Like the push-pull circuit, it has two parallel input loops, one for each half-cycle of the magnetic cycle, with one MOSFET in each loop. Like the push-pull, the transformer operates over the full (bipolar) magnetic-flux ripple range ($\pm \hat{B}_{\sim}$), and the transformer secondary circuit has a fast-recovery diode (FRD) full-wave bridge for rectification.

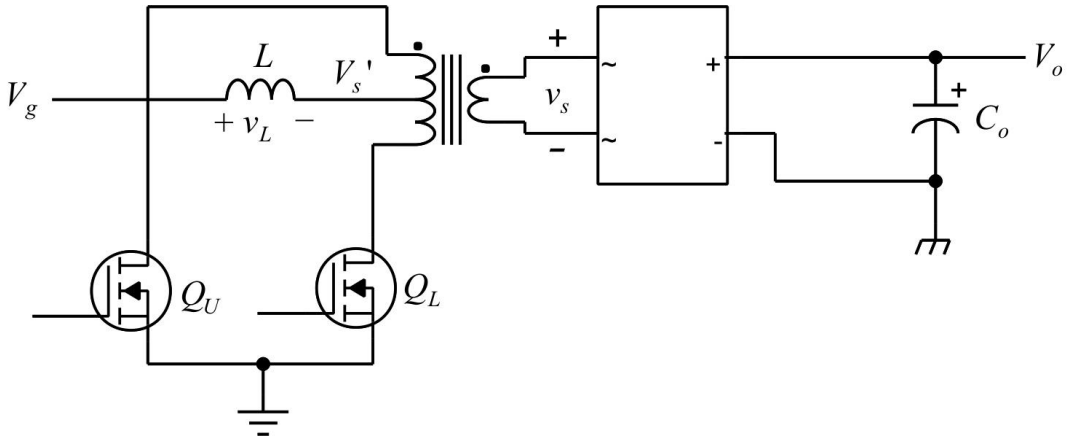


*Fig. 5. A boost (common-active) push-pull power-transfer circuit has an input inductor and transformer. The high input current is routed through the inductor and one MOSFET switch during off-time, and through both switches during on-time, thereby minimizing power loss from series switch resistance.*

Unlike the push-pull chopper circuit (PP), it is a boost converter. At the primary center-tap during off-time, it has $V_s' = n \cdot V_s > V_g$. It is during off-time, not on-time as in the PP, that power is transferred, and with $V_s' > V_g$, $n$ is larger, as is secondary current, $I_s$.

Primary RMS current is also smaller for the same power transfer than the PP. It is a circuit with a higher output voltage. By designing $V_s'$ to be a safety margin above $V_g$, the transformer power rating must be slightly larger than the rated transfer power, but the inductor power rating is reduced significantly as we will see when the magnetic components are designed. It is the added inductor that distinguishes the BPP from a PP chopper.

Another difference between the PP and BPP circuits is the switch sequencing. During on-time, both BPP switches are on, shorting the transformer primary windings to ground, with $V_s'$ on the transformer side of the input inductor. On alternating switching cycles (or magnetic half-cycles) of the BPP, one MOSFET switch stays on and conducts all inductor input current, $I_g$.

During off-time time, the other transistor is off, with a voltage of $2 \cdot V_s'$ across it. The magnetizing current in the primary winding, $i_{mp}$ transfers to the off-side primary winding as it does in the PP, shown in Fig. 4. The body-drain diode of the off MOSFET conducts. When the next cycle begins, the MOSFET that is already conducting in the reverse direction switches on with zero switching loss.

A reliability problem with push-pull primary circuits is flux imbalance. By omitting current sensing (as is done in the flimsiest units), there is no good way to correct for runaway magnetizing current. Any flux imbalance between the two half-cycles from differing MOSFET or winding on-resistance and hence winding voltage results in a change in magnetizing current during one half-cycle not exactly equal to the opposite change during the opposing half-cycle. The current increases in magnitude slightly each cycle until a component (usually a MOSFET) fails from overcurrent.

A method of correction is to make the circuit resistance high enough that voltage drop from the extra current compensates, but this increases power loss. Push-pull voltage drive is inherently unstable. The solution is to operate push-pull circuits with current control. The BPP input inductor reduces flux imbalance but does not prevent it.

The common-active (boost) PWM-switch configuration has a voltage transfer ratio,

$$\frac{V_o}{V_g} = \frac{1}{n} \cdot \frac{1}{1-D} = \frac{1}{n} \cdot \frac{1}{D'}, \; n = \frac{N_p}{N_s}$$

where $n$ is the turns ratio of the transformer and $N_p$ is the number of turns of each half-winding (or each of the two center-connected windings) on the primary side.

The secondary circuit is that of a peak-charging rectifier with essentially uncontrolled current pulses through the output capacitor, $C_o$ that stores and supplies output current when the rectifier diodes are off. The diodes conduct during the switching-cycle off-time at secondary winding voltage, $v_s$, which exceeds two diode drops plus the output voltage, $V_o$ across $C_o$.

The conduction time is $D' \cdot T_s$ of the cycle. The charge of the average current is supplied during this time. By reducing $C_o$ in value, diode conduction time is increased for a given average output current and the peak current amplitude is reduced at the expense of larger voltage ripple. Unlike for sine-waves, however, square-wave peaks have a relatively long duration, allowing diode bridge conduction for a larger fraction of the cycle, thereby reducing peak converter current.

## A Battery Converter Alternative: SEPIC Converter

An alternative power-transfer circuit for low-resistance inputs is a common-inductor (boost-buck) PWM-switch configuration with current steering—a *Ćuk-switch* circuit. It has a single transistor in series with the input winding, and can be optimized for near-zero current ripple from the input source. The SEPIC converter, which is shown in Fig. 6, is in the class of Ćuk-derived circuits, all of which can be modeled by configurations of the four-terminal Ćuk-switch. Ćuk-switch transfer circuits are PWM-switch common-inductor (CL) configurations.

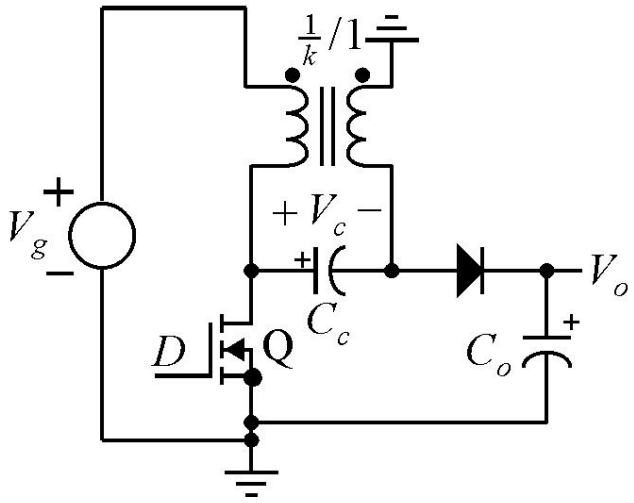


*Fig. 6. Ćuk-switch (SEPIC) transfer circuit. Both output and the passive-side windings are grounded.*

In this circuit, the transductor—a term that refers to both transformers and inductors—operates at the boundary between transformer and coupled-inductor behavior. During on-time, the active MOSFET switch, Q is on and $V_g$ is applied to the left-side primary winding. With a turns ratio of $n \approx 1$, $V_g$ also appears across the secondary winding, causing the voltage at the diode-capacitor node to be $-V_g$. The output diode is off during the on-time.

The coupling capacitor, $C_c$, charges to an average voltage of $V_g$ with the polarity indicated. During the off-time it has been charged to $V_g$. Then its voltage, $v_c$ is applied through Q across the secondary winding with a polarity that opposes the primary drive voltage. Both are close to $V_g$, but by setting the turns ratio to slightly more than one (actually, $1/k$, where $k$ is the coupling coefficient), $v_c$ drives the transductor mutual inductance so that the magnetizing current is sourced by $C_c$ from the secondary winding. Then no magnetizing current ripple appears in the primary winding and it is constant. This has the advantage of reducing power loss and EMI from the battery cables.

Q conducts not only the primary current, $i_p$ but also the current of the secondary winding, through $C_c$, or $i_c$. Over a switching cycle, $T_s$ the average MOSFET current, $\bar{i}_Q = \bar{i}_p$. When Q shuts off, the polarity across both windings reverses and $i_c$ reverses. The winding polarity causes the output diode to conduct, clamping the secondary winding to the voltage, $V_s = V_o + V_D$ where $V_D$ is the diode on-voltage. Then $V_s$ is induced in the primary winding.

For the complete cycle, $v_c$ averages to $V_g$, but during the off-time, it is recharged by $i_p$ flowing through it to the output. Both Q and the diode conduct $i_p + i_s$ and must be rated accordingly. For high primary current, this increases the already demanding switch current requirements.

The transductor has a net flux per cycle for steady-state operation of zero. The circuit-referred flux is

$$\lambda = v \cdot t$$

The average on-time flux is $V_g \cdot D \cdot T_s$. The average off-time flux is $V_s \cdot D' \cdot T_s$. The two flux magnitudes must be equal or $i_p$ will increase without bound over multiple cycles. When equated, the voltage transfer ratio is

$$\frac{V_s}{V_g} = \frac{\bar{v}_s}{\bar{v}_g} = \frac{\tilde{v}_s}{\tilde{v}_g} = \frac{D}{D'}$$

Charge balance on $C_c$ must also be maintained over $T_s$. The charge is

$$q = i \cdot t$$

For the on-time, the average charge is $I_s \cdot D \cdot T_s$ and for the off-time, $I_p \cdot D' \cdot T_s$. Equating and solving for the current transfer function,

$$\frac{I_p}{I_s} = \frac{\bar{i}_p}{\bar{i}_s} = \frac{\tilde{i}_p}{\tilde{i}_s} = \frac{D}{D'}$$

The primary and secondary currents are assumed to have a negligible ripple component. Consequently, current amplitudes equal average and RMS current values. Multiplying the two transfer functions and solving, we find that the input power equals the output power, as it must for the lossless power-transfer circuit.

The average input current is

$$\bar{i}_g = \frac{\bar{P}_g}{V_g}$$

The active-switch average current,

$$\bar{i}_Q = (I_p + I_s) \cdot D = \left( I_p + \frac{D'}{D} \cdot I_p \right) \cdot D = I_p = \bar{i}_p$$

where $I_p$ and $I_s$ are the conduction-time amplitudes of the primary and secondary currents.

Similarly, both winding currents also divert to the diode during the off-time, and

$$\bar{i}_o = \bar{i}_D = (I_p + I_s) \cdot D' = \left( \frac{D}{D'} \cdot I_s + I_s \right) \cdot D' = I_s = \bar{i}_s$$

The transistor and diode switch currents are discontinuous, and their RMS values vary with $D$;

$$\tilde{i}_Q = \sqrt{D}\cdot\sqrt{\left(\frac{I_p}{D}\right)^2} = \frac{\bar{i}_g}{\sqrt{D}}; \tilde{i}_D = \sqrt{D'}\cdot\sqrt{\left(\frac{I_s}{D'}\right)^2} = \frac{\bar{i}_o}{\sqrt{D'}}$$

The capacitor current is an average of near-constant $i_s$ during $D$ and $i_p$ during $D'$. The RMS value of a bipolar square-wave is, in general,

$$\tilde{x} = \sqrt{D\cdot X_+^2 + D'\cdot X_-^2} \Rightarrow \tilde{i}_c = \sqrt{D\cdot I_s^2 + D'\cdot I_p^2}$$

Magnetizing current, $i_m$ is assumed negligible. Substituting for either winding current, and finally both,

$$\tilde{i}_c = \sqrt{\frac{D'}{D}}\cdot I_p = \sqrt{\frac{D}{D'}}\cdot I_s = \sqrt{I_p\cdot I_s}$$

The capacitor RMS current is the geometric mean of the primary and secondary current amplitudes.

The form factors of transfer-circuit currents are

$$\kappa_g = \kappa_p = \kappa_s = 1;\ \kappa_Q = \frac{1}{\sqrt{D}}; \kappa_D = \kappa_o = \frac{1}{\sqrt{D'}}$$

### *Push-Pull And SEPIC Compared*

The decision as to which topology is superior for the battery converter stage cannot be reduced easily to a single scalar numerical comparison. However, some additional insight can be achieved by confining a comparison to the parameters where the design is most constrained. For low-$R_g$ (low voltage, high current) converters, active (primary-side transistor) switch and transductor primary current losses are a driving design consideration. The passive (secondary-side diode) switch loss is included in an overall switch figure of demerit: the product of the switch form factors or switch *form-factor product*

$$\kappa_{QD} = \kappa_Q\cdot\kappa_D$$

For both push-pull and SEPIC converters, $\Delta i_m$ can be reduced by increasing transductor inductance. In optimizing design, power loss from the ripple component of the currents (ignored in the above formulas) is traded off against the size and cost of the transductor, both of which increase with inductance. Consequently, the small-ripple approximation applies, and $i_m$ is not a significant consideration in assessing the relative merits of alternative power-transfer circuits.

The plots in Fig. 7 show push-pull and SEPIC active-switch and passive-switch losses with comparable average currents. The SEPIC form factors are symmetric with $D$ and $D'$ interchanged. The push-pull circuit has the lowest loss at high duty-ratio, with a minimum $\kappa_{QD} = \sqrt{2} \approx 1.414$ at $D = 1$; the SEPIC minimum $\kappa_{QD} = 2$. This is the main PP advantage over the SEPIC. PP diode and transistor loss both decrease as $D$ increases.

By equating push-pull and SEPIC switch form-factor products and solving for the crossover $D$, the SEPIC has an efficiency advantage over push-pull below $D = ⅔ \approx 0.67$. To be superior in switch efficiency, the push-pull must be designed to operate at $D > ⅔$.

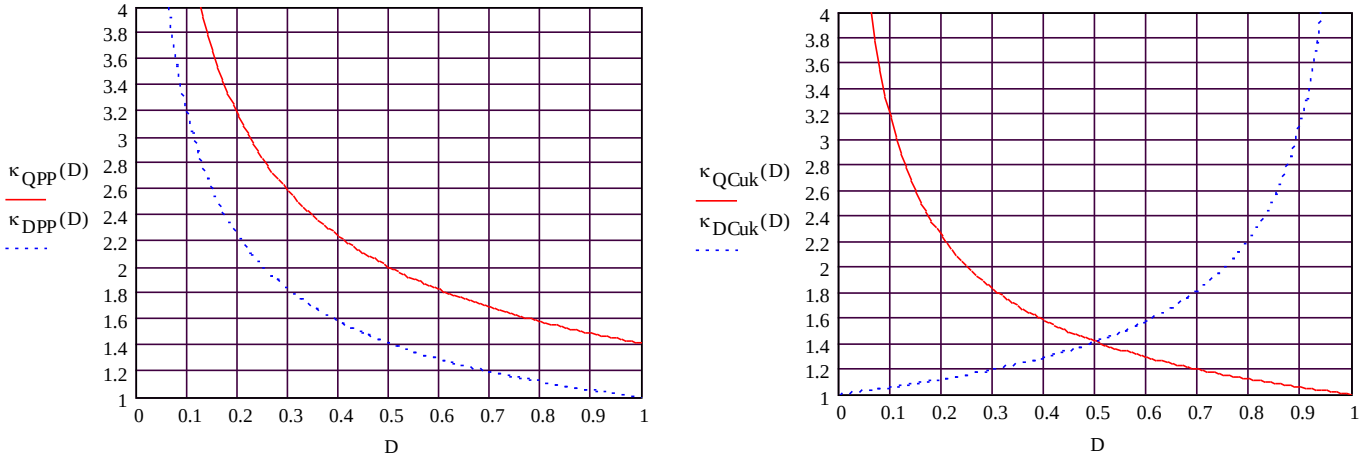


*Fig. 7. Plots of active (Q) and passive (D) switch current form factors, κ for push-pull (left) and SEPIC (right) circuits with duty-ratio D. The form-factor product has a minimum of* $\sqrt{2} \approx 1.414$ *for push-pull and 2 for SEPIC circuits.*

The SEPIC has a transductor advantage in that the ripple component of its winding currents is essentially zero. This allows use of iron-powder instead of ferrite cores. Not only are they lower in cost, but they also have significantly higher saturation-current values. Winding loss is also reduced because the input current is constant.

Yet the SEPIC has some disadvantages. One is the $C_c$ isolation versus transformer isolation of the push-pull scheme. (Low-cost commercial inverters usually are not isolated.) Another of the disadvantages of the Ćuk-switch converters is that the currents of both transductor windings flow through both the active (transistor) and passive (diode) switches. For low-resistance circuits, this increases an already difficult maximum current requirement for the circuit components.

The push-pull form factors for both primary and secondary vary together with $D$. By maximizing $D$, both $\kappa_p$ and $\kappa_s$ are minimized. For the SEPIC, the primary and secondary $\kappa$ conflict. The best that can be achieved is a compromise optimum at $D$ = ½.

An additional disadvantage of the SEPIC power-transfer circuits is that a large fraction of the input current must be conducted through the coupling capacitor, an RMS amount equal to the geometric mean of the two transductor winding currents. Minimum RMS capacitor current at $D$ = ½ is still that of the equal currents of the windings. A way around these obstacles is to tap the winding(s), which make Ćuk-derived circuits more of a competing alternative for high input currents. Tapping, however, also increases current ripple.

In comparison of the push-pull and SEPIC from a control standpoint, it is evident that push-pull losses are minimized for both primary and secondary circuits by maximizing $D$. The optimal push-pull control scheme that emerges from this is one of fixing $D$ at the maximum realizable value (perhaps around 0.95 for most PWM ICs) and regulating with cycle skipping. This scheme avoids the need to stabilize a feedback loop that controls $D$ along with the additional components that compensation entails.

Feedback-loop stability margins of the push-pull buck circuit are less difficult to achieve over the range of operation because of its linear transfer function. The $D/D'$ transfer function of the SEPIC is nonlinear, but it also has in its $i_o/d$ transfer function (where $d$ is the incremental $D$) a complex RHP zero-pair. The push-pull scheme is derived from the common-passive (buck) configuration and has a real LHP zero. Both have a LHP complex pole-pair.

For SEPIC control optimization, the tradeoff between primary and secondary losses offers additional design freedom as to where the losses can be shifted. For equal switch form factors, $D$ is optimally ½. For waveform

generation, large excursions from 0.5 will drive $\kappa$ on primary or secondary side to high values. For output voltages at the low end of the range, the dominant losses are in the secondary circuit; for high output voltages, losses are higher on the primary side, as the following table shows.

Table. Current form factors versus duty cycle for the SEPIC.

| D | pri κ = $1/\sqrt{D}$ | sec κ = $1/\sqrt{D'}$ |
|---|---|---|
| 0.5 | 1.414 | 1.414 |
| 0.6 | 1.291 | 1.581 |
| 0.685 | 1.208 | 1.782 |
| 0.7 | 1.195 | 1.826 |
| 0.75 | 1.155 | 2.000 |
| 0.8 | 1.118 | 2.236 |
| 0.9 | 1.054 | 3.162 |
| 0.95 | 1.026 | 4.472 |
| 1 | 1 | ∞ |

For values of $D < 0.5$, swap $D$ and $D'$. For instance, the $1/\sqrt{D}$ value for $D = 0.1$ is $1/\sqrt{D'}$ for $D = 0.9$, or 3.162, and $1/\sqrt{D'}$ for $D = 0.1$ is the $1/\sqrt{D}$ value for 0.9, or 1.054. At $D = 0.5$, the SEPIC form factors are $\kappa_Q = \kappa_D = \sqrt{2} \approx 1.414$, comparable to max-$D$ push-pull $\kappa_{QD}$. The SEPIC has the immense disadvantage of recirculating power equal to the transfer power through the transductor windings and its large coupling capacitor.

## Boost Push-Pull Waveform Generation

The suitability of the boost push-pull to the Volksinverter design has been noted, but this is not the end of the discussion. We also need to think further about its limitations and possible ways to address them. The current-driven BPP circuit improves low-$R_g$ efficiency but because $V_s' > V_g$, it is limited as a waveform generator at low output voltages. However if both overlapping and non-overlapping switch conduction is output by the controller then the lower output voltage range can be generated in the non-overlapping mode. The relationship between these modes is accounted for quantitatively by setting $D' > 1$ in the equations. Then $D$ emerges as non-overlapping for the two transistors.

For non-overlapped switching both switches are off some of the time, and the inductor current has nowhere to go. If the inductor is given an additional winding that returns its off-time current either to the input or output through a diode, the augmented converter is a *Weinberg transfer circuit*, shown in Fig. 8. The diode could be returned to $V_g$ with $n = 1$, and with large-sized secondary wire. More efficient is the output-return option shown in Fig. 8. The additional winding has a turns ratio comparable (if not equal) to the transformer. For large $n$ and diode returned to the output, the output winding would not be of large-size wire.

This circuit can generate the full range of the output waveform though commercial PWM controllers do not have the versatility of both switching modes and extra circuitry is required. It can be operated either in CP (buck) mode with non-overlapping switch on-times or in CA (boost) mode with overlap for $V_s' > V_g$. At the crossover voltage for $V_s'$, modes are switched and $D$ changes discontinuously from 1 to 0. In CP mode, from flux balance,

$$(V_g - n \cdot V_s) \cdot D = n_L \cdot V_s \cdot D' \ , \ V_s \approx V_o + V_D$$

where $n_L$ is the turns ratio of the (coupled) inductor. Then the buck transfer function is

$$\frac{V_s}{V_g} = \frac{D}{n \cdot D + n_L \cdot D'}$$

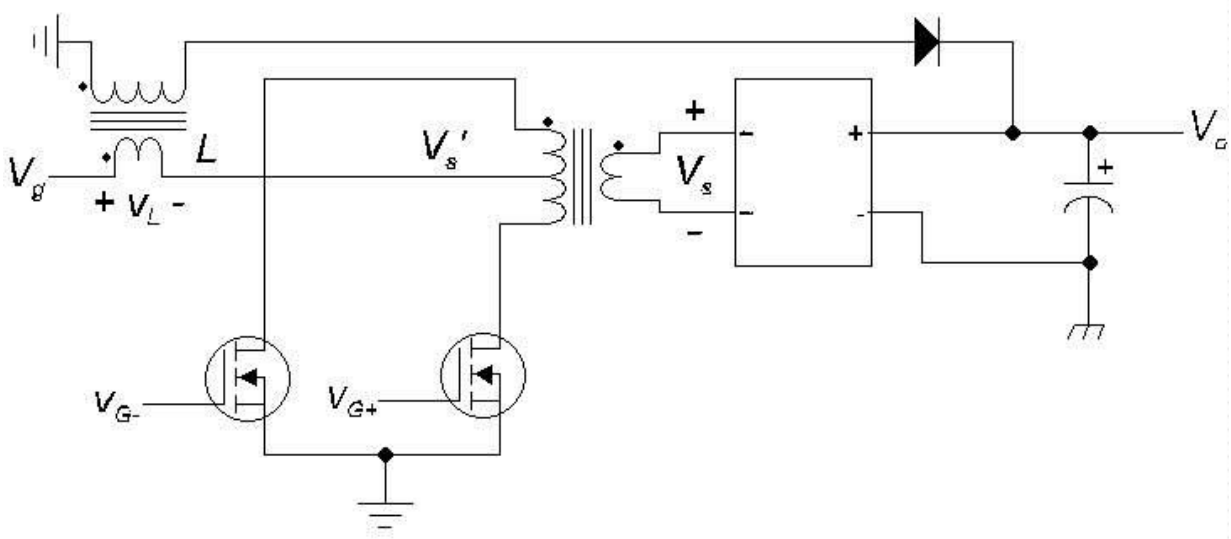


*Fig. 8. A Weinberg circuit is a buck transfer circuit that is operated as a boost push-pull circuit with non-overlapping switch drive and an additional close-coupled winding on the input inductor for returning its energy to the output.*

Whenever the inductor turns ratio is that of the transformer then $n_L = n$ and

$$\frac{V_s}{V_g} = \frac{1}{n} \cdot D \ , \ V_s' < V_g$$

For the CA (non-overlapping) boost mode,

$$V_g \cdot D \ = (n \cdot V_s - V_g) \cdot D' \Rightarrow \frac{V_s}{V_g} = \frac{1}{n} \cdot \frac{1}{D'} \ , \ V_s' > V_g$$

The boost mode does not use the secondary winding of the coupled inductor and $n_L$ consequently does not appear in its equations.

## *Conclusion*

From this survey comparing different inverter circuit design possibilities and with additional comparisons in subsequent parts of this series, the chosen power-transfer circuit is the boost push-pull. The advantages will become more evident as the series progresses, though in some cases alternative circuits have their relative advantages. Yet overall the BPP excels and is the basis for the converter of a two-stage battery converter-inverter scheme for the Volksinverter.

**References**

1. "Designing An Open-Source Power Inverter (Part 1): Goals And Specifications" by Dennis Feucht, How2Power Today, May 2021.
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**About The Author**

*Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.*

*For further reading on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC power inverters."*